`mos_inverter_buffer.sqproj`

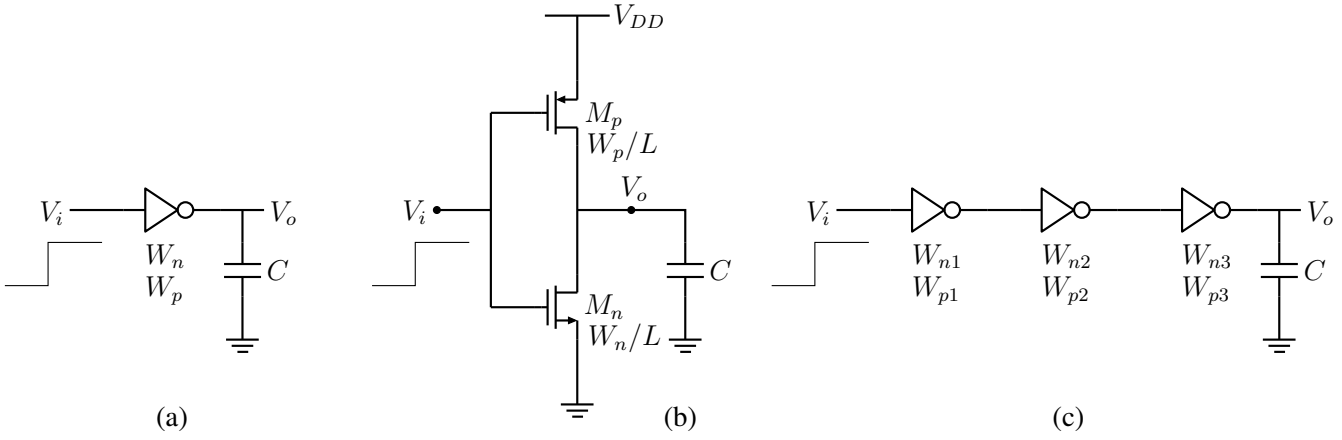

Figure 1: (a) A CMOS inverter driving a capacitive load, (b) Detailed circuit diagram of the inverter, (c) A chain of inverters driving a capacitive load.

Consider a CMOS inverter with a capacitive load as shown in Fig. 1 (a). The circuit diagram of the inverter is shown in Fig. 1 (b). We will assume that all transistors have the same length L (minimum feature size), a typical situation in VLSI circuits. We are interested in the propagation delays (t_{PHL} and t_{PLH}) between the input V_i and output V_o.
When the output goes from V_{DD} to 0 V, C gets discharged through M_n. As an approximation [1], we can replace M_n with an average resistance

$$R_n = \frac{V_{DD}}{\frac{W_n}{L}\frac{K'_n}{2}\left(V_{DD}-V_{Tn}\right)^2} \equiv R'_n\frac{L}{W_n}\,, \quad R'_n = \frac{V_{DD}}{\frac{K'_n}{2}\left(V_{DD}-V_{Tn}\right)^2}\,, \tag{1}$$

where $K'_n = \mu_n C'_{\rm ox}$. The delay t_{PHL} is then given by

$$t_{PHL} = R'_n\frac{L}{W_n}\left(C_{\rm out}+C_{\rm load}\right)\,, \tag{2}$$

where $C_{\rm out} \propto W\,L\,C'_{\rm ox}$ is the "intrinsic" capacitance of the inverter, and $C_{\rm load}$ is the load capacitance. Similarly,

$$t_{PLH} = R'_p\frac{L}{W_p}\left(C_{\rm out}+C_{\rm load}\right)\,. \tag{3}$$

We now compare two cases: (i) single inverter with widths W_n and W_p (Figs. 1 (a), 1 (b)) and (ii) a chain of inverters with W_{n1}, W_{p1} the same as the single inverter case, and progressively

larger widths for the subsequent stages, viz., $W_{n2} = A\,W_{n1}$, $W_{n3} = A\,W_{n2} = A^2\,W_{n1}$ (similarly, for the p-channel transistors). The load capacitance for both of these configurations is the same.

If we take a simplistic view, we will conclude that the delay in the second case will be larger since the total delay is the addition of the delays due to the three inverters. However, the situation is more complex because the delay of a given stage depends on not only its capacitive load but also its current capability. A transistor with larger W can charge a given load capacitance faster. If the factor A is selected carefully, the delay for the chain of inverters can be made much smaller than the single inverter case, particularly when the load capacitance is large. Further details of the calculation can be found in [1].

Exercise Set

1. In the circuit file, we have two situations: (a) a chain of three inverters with transistor widths selected using the above procedure and $C = 20\,\text{pF}$, (b) a single inverter with the same widths as the first inverter in (a) and a much smaller C ($1\,\text{pF}$).

   Run the simulation, and compare the propagation delays in the two cases. Note that the delays in case (a) would be much larger if the capacitance values in (a) and (b) were the same.

2. In the single inverter case, it is possible to reduce the propagation delays by increasing W_n and W_p. Is this desirable?

References

1. R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, Prentice-Hall India, 1998.