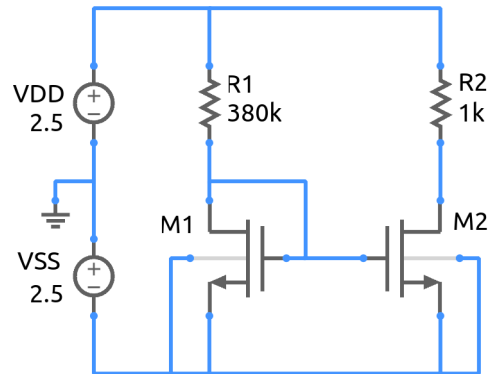


mos_mirror_1.sqproj



Use mos_mirror_iv_1.sqproj to plot I-V of M2.

A basic current mirror is shown in the figure. It has been designed for an output current of $10\ \mu\text{A}$, with transistors M_1 and M_2 having the same W/L ratios and other parameters. The BSIM1 model is used for the transistors, and the parameter values have been taken from [1]. BSIM1 is a complex model in which different parameters affect the device characteristics in a composite manner. It is convenient therefore to use an additional circuit file (`mos_mirror_iv_1.sqproj`) to get an idea of the device characteristics. The threshold voltage of the transistors is found to be about 1 V, and r_{on} at $I_D = 10\ \mu\text{A}$ is about $1\text{V}/0.6\ \mu\text{A}$, i.e., $1.7\ \text{M}\Omega$.

Exercise Set

1. Run the simulation, plot I_1 and I_2 (currents through M_1 and M_2 , respectively) as a function of V_o (voltage at the drain of M_2), and verify that $I_2 \approx I_1 \approx 10\ \mu\text{A}$.
2. Calculate the expected value of V_G for the parameters given in the circuit file and $I_D = 10\ \mu\text{A}$. Verify with simulation.
3. For the circuit to work as a current mirror, M_2 should operate in saturation. Find the value of V_o at which M_2 leaves the saturation region. How will this affect the I_2 versus V_o relationship? Verify with simulation.

4. From the simulation results, calculate the slope dI_2/dV_o , and relate it to the output resistance of M_2 at $I_D \approx 10 \mu\text{A}$.

References

1. R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, Prentice-Hall India, 1998.