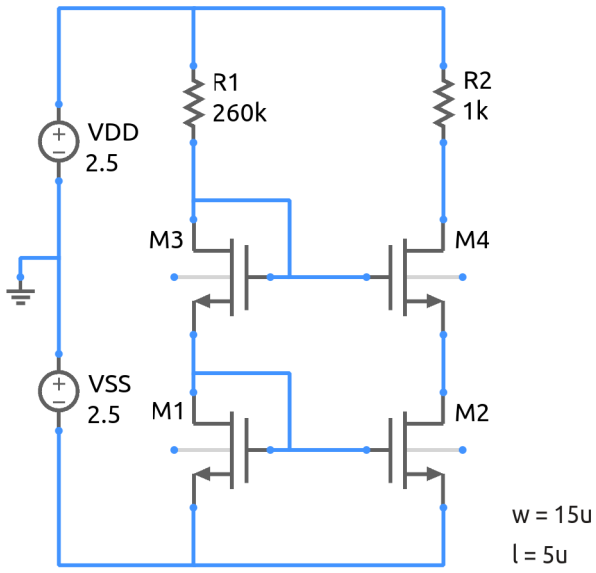
mos_mirror_2.sqproj



A cascode current source, which gives a significantly larger output resistance than the simple current source of `mos_mirror_1.sqproj`, is shown in the figure. It has been designed for an output current of $10\,\mu$A, with transistors M_1, M_2, M_3, M_4 having the same W/L ratios and other parameters.

The BSIM1 model is used for the transistors, and the parameter values have been taken from [1]. BSIM1 is a complex model in which different parameters affect the device characteristics in a composite manner. It is convenient therefore to use an additional circuit file (`mos_mirror_iv_1.sqproj`) to get an idea of the device characteristics. The threshold voltage of the transistors is found to be about 1 V, and r_{on} at $I_D = 10\,\mu$A is about $1\dot{\text{V}}/0.6\,\mu$A, i.e., 1.7 MΩ. The output resistance of the current source is given by $R_o = g_m\, r_o^2$ and is estimated to be (see [1]) 152 MΩ.

Exercise Set

1. Run the simulation, plot I_1 (current through M_1 and M_3) and I_2 (current through M_2 and M_4) as a function of V_o (voltage at the drain of M_4), and verify that the current is close to $10\,\mu$A[1].

[1] Since V_{SB} is not 0 V for M_3, the actual current is somewhat different than the intended value of $10\,\mu$A.

2. Calculate the expected values of V_{G1} and V_{G3} for the parameters given in the circuit file and I_D found in the plot above. Verify with simulation.

3. For the circuit to work as a current mirror, M_4 should operate in saturation. Find the value of V_o at which M_4 leaves the saturation region. How will this affect the I_4 versus V_o relationship? Verify with simulation.

4. From the simulation results, calculate the output resistance $(dI_4/dV_o)^{-1}$.

References

1. R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, Prentice-Hall India, 1998.