

Figure 1: NMOS transmission gate.

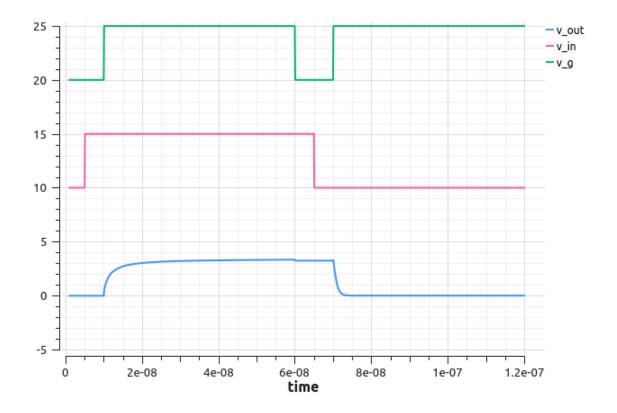


Figure 2: Simulation results for the NMOS transmission gate shown in Fig. 1. Note that the plots are offset by 10, 20 for clarity.

Fig. 1 shows an NMOS transmission gate. The input voltage, the gate voltage, and the output voltage are shown in Fig. 2 as a function of time.

## Exercise Set

- 1. Explain the operation of the transmission gate with the help of the waveforms in Fig. 2.
- 2. Compare the output voltage of the NMOS transmission gate with that of the CMOS transmission gate (mos\_pass\_c.sqproj).

## References

 R. J. Baker, H. W. Li, and D. E. Boyce, CMOS Circuit Design, Layout, and Simulation, Prentice-Hall India, 1998.