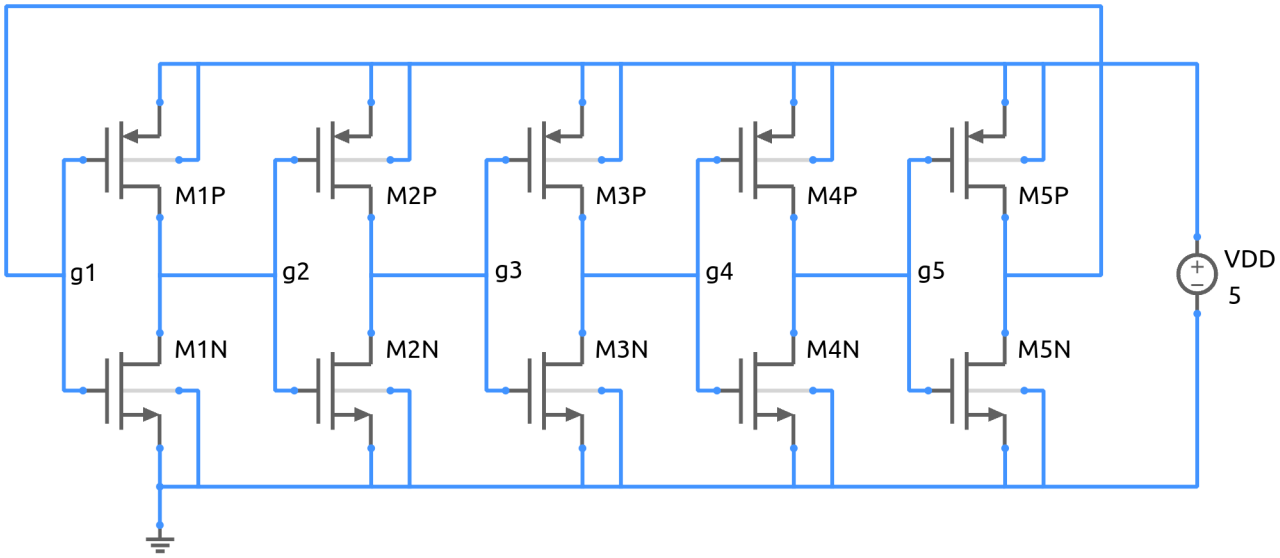
mos_ring_osc.sqproj



A ring oscillator with five CMOS inverters is shown in the figure. The oscillation frequency is given by

$$f_o = \frac{1}{n\,(t_{PHL} + t_{PLH})}\,, \tag{1}$$

where n is the number of inverters, and t_{PHL}, t_{PLH} are the propagation delays of one inverter driving another identical inverter. The delays are determined broadly by two factors: (i) the capacitance seen at the output of the inverter, (ii) the current carrying capability of the transistors. The capacitance seen at the inverter output node is proportional to $W \times L$ (the transistor area), and the current carried by a transistor is proportional to W/L.

Exercise Set

1. Run the simulation, plot the voltages at the five inverter output nodes (together), and explain how they are related. From the plot, calculate the oscillation period and frequency.

2. Make the following changes, run the simulation, plot $V_{G1}(t)$, and compare the oscillation period with the original value. Explain qualitatively your results in each case. (Note that the global parameters `w_n`, `w_p`, `phi_n`, `phi_p` are convenient here, with `phi_n`, `phi_p` controlling the threshold voltages[1] of the n- and p-channel transistors, respectively.)

[1]The circuit file `mos_iv_1.sqproj` may be used to see the effect of `phi` on the I_D-V_G curve.

(a) The length as well as width of each n-channel transistor are doubled.

(b) Width of each n-channel transistor is changed from $5\,\mu$m to $20\,\mu$m.

(c) Width of each p-channel transistor is changed from $5\,\mu$m to $20\,\mu$m.

(d) Width of each transistor is changed from $5\,\mu$m to $20\,\mu$m.

(e) The parameter `phi_n` is decreased by 0.5.

(f) The parameter `phi_p` is decreased by 0.5.

References

1. R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, Prentice-Hall India, 1998.