mos_vco_1a.sqproj

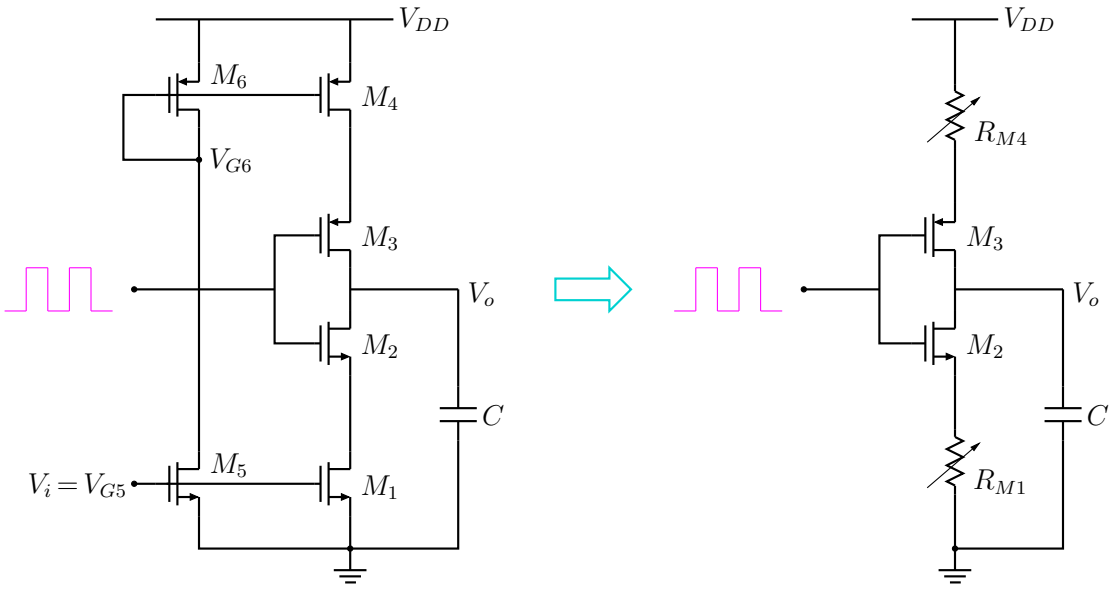

Figure 1: (a) Circuit to illustrate the working principle of the VCO in `mos_vco_1.sqproj`, (b) Simplified circuit.

The purpose of this example is to illustrate the principle of operation of the voltage-controlled oscillator (VCO) in the circuit file `mos_vco_1.sqproj`. The input voltage V_i is applied to the gate of M_5 (see Fig. 1 (a)). If V_i is increased, V_{G6} decreases, as seen in `mos_vco_1b.sqproj`. Since G_5 and G_6 are tied to G_1 and G_4, respectively, I_{M1} and I_{M4} increase as V_i is increased, and *vice versa*.

In the present example, we do not have an oscillator. Instead, we have a single inverter M_2-M_3, as shown in the figure. Our intention is to look at the propagation delays of this inverter as V_i – a DC voltage – is varied. The effect of a change in V_i can be described with the simplified circuit shown in Fig. 1 (b) in which the transistors M_1 and M_4 have been replaced with resistances[1] which vary with the input voltage V_i. As V_i increases, R_{M1} and R_{M4} decrease. As a result, larger currents (I_{M2},I_{M3}) beceome available to charge or discharge

[1]Note that this is an oversimplification. A MOS transistor is a nonlinear device and must be treated as such. The variable resistances must be viewed as a crude approximation made only for the purpose of conceptual understanding of the circuit.

the load capacitor C, leading to smaller propagation delays of the inverter.
The operation of a VCO is similar: A change in the input voltage causes a change in the propagation delays in each inverter in the ring oscillator, thereby causing a change in the oscillation frequency.

Exercise Set

1. Study the circuit file `mos_vco_1b.sqproj` to understand how V_{G6} is affected by V_{G5}.

2. Run the simulation, and plot the inverter input and output voltages versus time for $V_i \equiv V_{G5} = 2\,\mathrm{V}$. From the plot, find t_{PHL} and t_{PLH}.

3. Repeat for $V_i = 2.5$, 3, 3.5, 4, $4.5\,\mathrm{V}$. Plot t_{PHL} and t_{PLH} as a function of V_i.

References

1. R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, Prentice-Hall India, 1998.