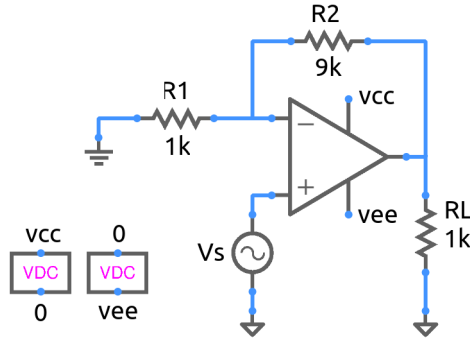


## non\_inv\_amp.sqproj



Shown in the figure is an Op Amp based non-inverting amplifier. In this circuit, the Op Amp operates in the linear regime, which guarantees that the inverting and non-inverting terminals of the Op Amp are approximately at the same potential, i.e.,

$$V_+ - V_- \approx 0V. \quad (1)$$

Since  $V_+ = V_s$ ,  $V_-$  is also nearly equal to  $V_i$ . Further, owing to a large input resistance of the Op Amp, the current entering (or leaving) the Op Amp through the inverting terminal is negligible. Using these conditions, we get

$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_s, \quad (2)$$

Eq. 2 implies that the desired gain can be achieved by simply choosing appropriate values of  $R_1$  and  $R_2$ , and it frees the user from biasing considerations which arise in a common-emitter amplifier, for example. Furthermore, the amplifier can be used to amplify a DC voltage as well, which is not possible to do with a common-emitter amplifier where the coupling capacitors would block DC voltages.

Note that the output voltage is limited by  $\pm V_{\text{sat}}$ , the saturation levels of the Op Amp (about  $(V_{CC} - 1V)$  and  $(-V_{EE} + 1V)$ ).

### Exercise Set

1. For a sinusoidal input voltage with frequency 1 kHz and amplitude 1 V, and other parameters as specified in the circuit file, plot the expected output voltage versus time. Verify with simulation.

2. Increase the input voltage amplitude to 2 V, and simulate the circuit again. Explain your observations.

## References

1. S. Franco, *Design with Operation Amplifiers and Analog Integrated Circuits*, McGraw-Hill, 1998.
2. A. S. Sedra, K. C. Smith, and A. .N. Chandorkar, *Microelectronic Circuits*, Oxford University Press, 2004.