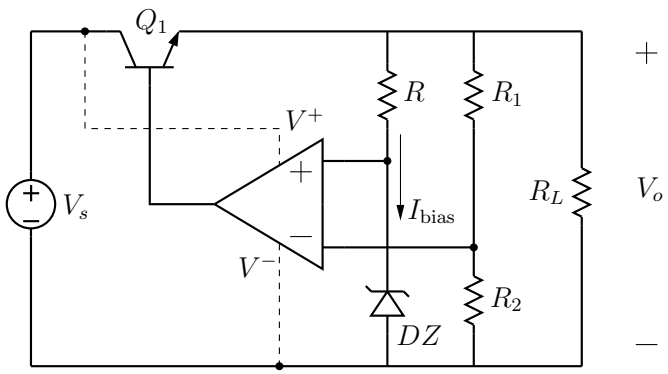
opamp_regulator_1.sqproj



The purpose of a voltage regulator is to provide a constant DC voltage to the load in spite of variations in the input DC voltage or in the load. In the circuit shown in the figure, the "control element" (Q_1) is in series with the load R_L, and this configuration is therefore called a "series mode regulator." The Zener diode provides a reference voltage. The resistor R is selected in order to bias the Zener diode:

$$I_{\text{bias}} = \frac{V_o - V_Z}{R}\,. \tag{1}$$

Assuming the Op Amp to be operating in the linear region, we have

$$V_+ \approx V_- \Rightarrow V_Z = \frac{R_2}{R_1 + R_2}\,V_o\,, \tag{2}$$

$$\text{i.e., } V_o = V_Z\left(1 + \frac{R_1}{R_2}\right)\,. \tag{3}$$

Note that the above equation does not involve the input voltage V_s. If V_s changes from V_s to $(V_s + \Delta V_s)$, the change ΔV_s gets absorbed in the V_{CE} of the transistor. In that sense, the output is isolated from the input by the transistor.

Exercise Set

1. For $V_s = 15\,V$, $V_Z = 2.9\,V$, $R_1 = 10\,\text{k}\Omega$, $R_2 = 5\,\text{k}\Omega$, $R = 5\,\text{k}\Omega$, $R_L = 100\,\Omega$, what is the expected value of V_o?

2. Vary V_s from $13\,V$ to $16\,V$, keeping the other parameters the same as before, and obtain a plot of V_o, V_{BE}, V_+, V_- versus V_s by simulation.

3. For a fixed value of V_s (say, $15\,V$), vary R_L from $100\,\Omega$ to $10\,\mathrm{k}\Omega$, and obtain a plot of V_o, V_{BE}, V_+, V_- versus $\log R_L$ by simulation.