Transient and Frequency Response Simulation of Second-Order Band-pass Switched-Capacitor Circuit (Biphase)

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Circuit file: sc_bpf_lq.in

Fig.1 shows the Band-pass switched capacitor network with all parameters. This circuit is simulated here in both domains, Frequency and Time. It is viewed as a connection of many commonly found SC blocks, namely Switched Resistor (sc_res_1), Floating capacitor (Float_cap) and Toggle Switched Inverter (TSI) and Switched-capacitor opamp (sc_opamp1).

Two such blocks are shown in Fig. 2 and Fig. 3 with its Time-domain (a) and Frequency-domain (b) equivalent circuits. As shown in the Fig.2 and Fig. 3, time-domain circuit is two-port (don't consider the nodes connected with low-value resistance (Rdl)), where as its frequency-domain (z-domain) equivalent circuit consists of four ports. Unused ports or nodes are connected with low-value resistance (Rdl) in Time-domain and High-value resistance (Rdh) in frequency-domain to avoid matrix to become singular.

All commonly found blocks are described as compound elements in SEQUEL with separate time-domain and frequency-domain description. Frequency-domain description assumes ideal elements and equal phase intervals. Time-domain description permits study of non-ideal elements and unequal phase intervals.

The simulated transient and frequency domain response are shown in Fig. 4 and Fig. 5 respectively. The approach utilized here to generate frequency response for switched-capacitor networks is such that it provides frequency response (magnitude and phase responses) for even and odd phases separately. If both of them are nonzero for the frequency-range of interests then they should be combined together by adding real parts of both phase and the same for imaginary parts. Now both terms should added after squared and square root should be calculated. Now it could be converted to gain. (Note that "lq" in sc_bpf_lq.in stands for "low-quality.")

1. Circuit Block:

```
title: 2nd order band pass filter

greal tc=0.01m roff=1e12 ron=1m rinop=1e12 av=1e5 tcby2 = 0.005m

*  Define a global parameter tc (clock period), roff and ron (switch off and on
*  resistances), rin (input resistance) and av (voltage gain) of op-amp and
*  tcby2.

begin_circuit
   eelement type=vsrcac p=a n=g a=1 f_hz=1k t0=0 phi=0

*  This element produces sine-wave source with frequency 1 khz.

   eelement name=src1 type=sc_source_2 vo_e=1e vo_o=1o g=g
+     aux1=a tc=tcby2 dt=100n s_2=5.0u
+     tau_1=5.0u tau_2=5.0u
```

```
*  This element samples the sine wave generated above at one-half of clock
*  frequency for even and odd phase and it also constructs the frequency-domain
*  representation for both even and odd phase sampled sine wave.


   eelement type=sc_res_1
+     vi_e=1e vi_o=1o vo_e=2e vo_o=2o g=g phi_e=phi_e phi_o=phi_o
+     ron=ron roff=roff c=0.0314p tc=tc

*  This element implements switched resistor shown in Fig. 2.
   eelement type=sc_float_cap
+     vi_e=2e vi_o=2o vo_e=3e vo_o=3o g=g
+     ron=ron roff=roff c=1p tc=tc

*  This element implements Floating Capacitor.

   eelement type=sc_res_1
+     vi_e=3e vi_o=3o vo_e=2e vo_o=2o g=g phi_e=phi_e phi_o=phi_o
+     ron=ron roff=roff c=0.0314p tc=tc

*  This element implements switched resistor shown in Fig. 2.

   eelement type=sc_res_1
+     vi_e=3e vi_o=3o vo_e=4e vo_o=4o g=g phi_e=phi_e phi_o=phi_o
+     ron=ron roff=roff c=0.0628p tc=tc

*  This element implements switched resistor shown in Fig. 2.

   eelement type=sc_float_cap
+     vi_e=4e vi_o=4o vo_e=5e vo_o=5o g=g
+     ron=ron roff=roff c=1p tc=tc

*  This element implements Floating Capacitor.

   eelement type=sc_tsi_1
+     vi_e=5e vi_o=5o vo_e=2e vo_o=2o g=g phi_e=phi_e phi_o=phi_o
+     ron=ron roff=roff c=0.0628p tc=tc

*  This element implements Toggle Switched Inverter shown in Fig. 3.

   eelement name=op1 type=sc_opamp1 vi_ep=g vi_em=4e vi_op=g
+     vi_om=4o  vo_eo=5e vo_oo=5o  gnd=g
+     rin=rinop rout=0 av=av

   eelement name=op2 type=sc_opamp1 vi_ep=g vi_em=2e vi_op=g
+     vi_om=2o  vo_eo=3e vo_oo=3o  gnd=g
+     rin=rinop rout=0 av=av

*  Above two statements implement two switched capacitor op-amps.
*  Each op-amp consists of two op-amps one for each phase.

   delement type=clock a=phi_e i0=1 t1=4.8u t2=5.2u t0=0
   delement type=clock a=phi_o i0=0 t1=5.2u t2=4.8u t0=0

*  These two statements generate non-overlapping clock signal to make the
*  switches on and off in even and odd phases.
```

```
   refnode=g

*  Node g is defined as the reference node for node voltages.

   outvar:
+     va=nodev_of_a v1e=nodev_of_1e v1o=nodev_of_1o
+     va_ac=nodev_ac_of_a v1e_ac=nodev_ac_of_1e v1o_ac=nodev_ac_of_1o
+     v2e=nodev_of_2e v2o=nodev_of_2o
+     v2e_ac=nodev_ac_of_2e v2o_ac=nodev_ac_of_2o
+     v3e=nodev_of_3e v3o=nodev_of_3o
+     v3e_ac=nodev_ac_of_3e v3o_ac=nodev_ac_of_3o

*  Definition of the output variables.

end_circuit
```

2. Solve Block 1:

```
begin_solve
   solve_type=startup
   initial_sol initialize
   method: t_startup=0

*  Do a "start-up" solution. As the initial guess for the
*  Newton-Raphson iterations, use the "initialize" option.
*  Since we have not generated any solution prior to this,
*  the "initialize" option has to be used.

end_solve
```

3. Solve Block 2:

```
begin_solve
   solve_type=trns
   initial_sol previous

*  Perform a transient simulation, using the previous solution
*  (obtained in the last solve block) as the initial guess for
*  the Newton-Raphson iterations. Note that "initial_sol" is
*  relevant only to get the transient simulation started (i.e.,
*  the very first time step). For subsequent time steps, the
*  solution obtained for the previous time step is always used
*  as the initial guess for the N-R iterations.

   begin_output
      filename=bpf1.dat limit_lines=2000000
      variables: v3e
   end_output

*  Specify which output files are to be generated and which
*  output variables are to be written to each of the files.
*  Note that we write here only analog variables of interest (v3e).
*  If we want to store digital variables, we should ask for one more file.
*  The two types of variables cannot be written to a single file.
*
*  Note that limit_lines has been specified in the above files
```

```
*  since the default value (10,000) is too small. The number
*  of lines which get written to the output files is larger
*  than this default value, and this would cause the program
*  to stop before the specified end time is reached.

   method: norm_2=1.0e-5 itmax_trns=1000000 back_euler=yes
+    t_start=0 t_end=5m delt_const=1u delt_min=10n

*  Specify the RHS norm ("tolerance"). The default value of
*  norm_2 is 1.0e-10. However, that turns out to be too rigid
*  for this problem and hence the need to change it.

*  Use the backward Euler method with a constant time step of
*  1 usec.

*  Specify the starting and ending times, and time step.
*  Note that itmax_trns has been specified since the default
*  value (10,000) is too small; the number of time points required
*  for this simultion is larger than the default itmax_trns.

end_solve
```

4. Solve Block 3:

```
begin_solve
   solve_type=ac
   vary_freq from 10 to 5k type=log n_points=250

*  Above two statements perform AC analysis. It is performed with
*  frequency points chosen in logarithmic fashion with number of points 250.

   begin_output
      filename=bpfmp.dat
      variables:
+       mag_of_v3e_ac phase_of_v3e_ac
+       mag_of_v3o_ac phase_of_v3o_ac
   end_output

*  Specify the output file and variables to be written.

end_solve

end_cf
```

Results:

In this example, simulated transient and frequency domain response are shown in Figs. 4 and 5, respectively. Fig. 4 shows the study of the effects of op-amp input resistance and voltage gain on output signal. The effects of non-idealities can be studied in transient analysis only.

References:

[1]K. R. Laker, “Equivalent circuits for the analysis and synthesis of switched-capacitor networks,” Bell Syst. Tech. J., vol. 58, pp. 727-767, Mar. 1979.

[2]“www.ece.utexas.edu/~holberg/lecture_notes/bk9.pdf”

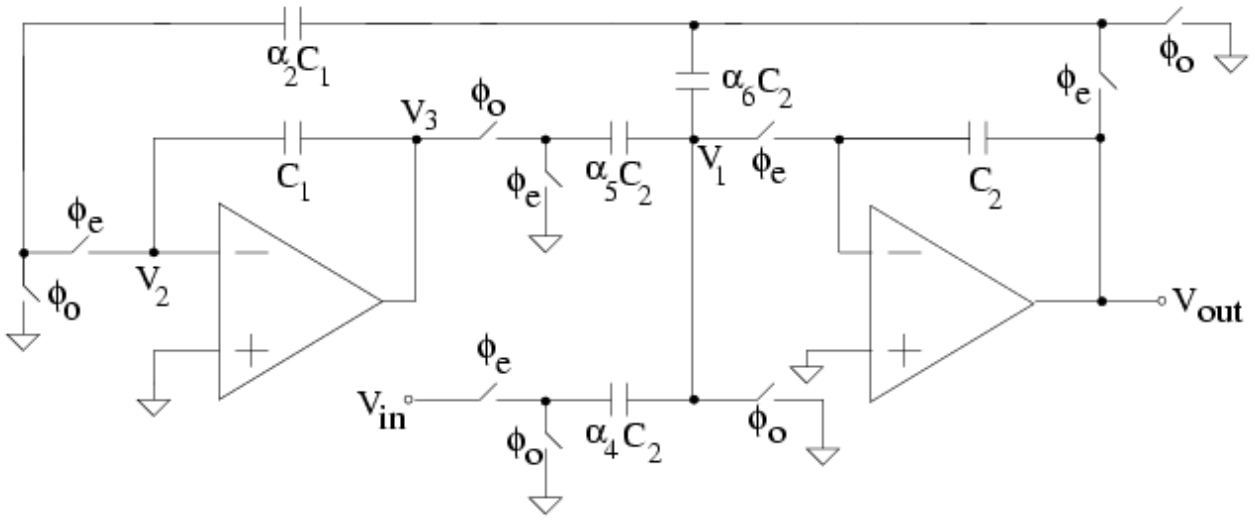

Fig. 1. Second-order band-pass SC Filter; the circuit parameters are $C_1 = C_2 = 1$ pF, $Q = 2$, $f_c = 100$ kHz, $\alpha_5 = \alpha_2 = 0.0628$ and $\alpha_4 = \alpha_6 = 0.0628$

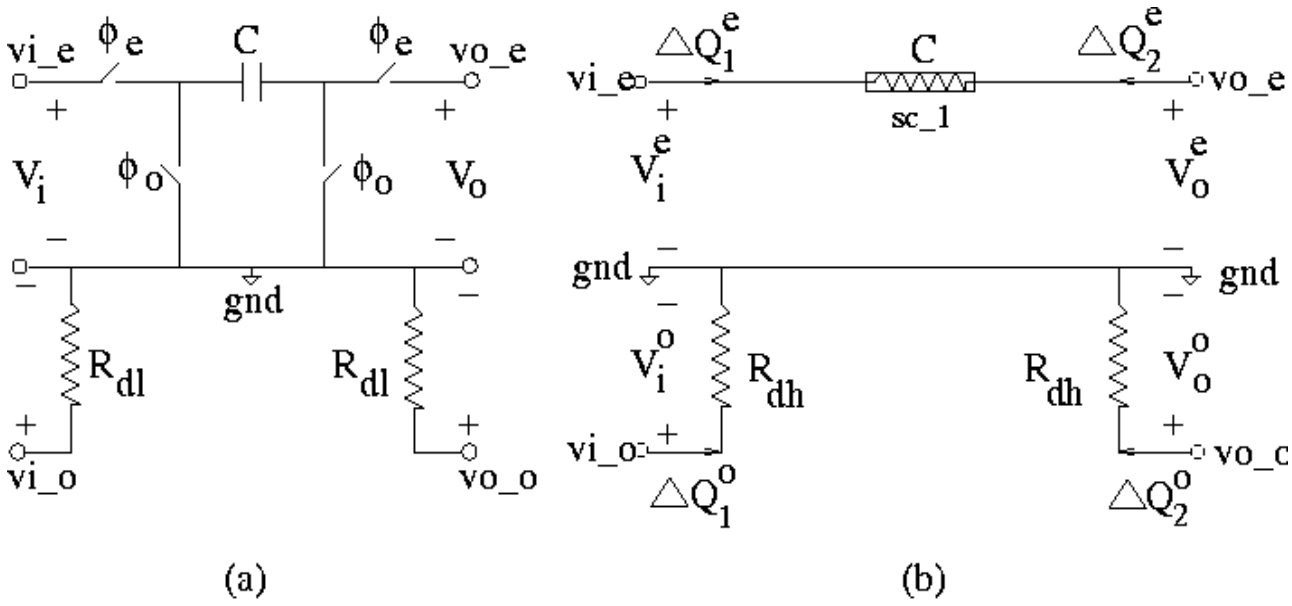

Fig. 2. Switched resistor circuit, time-domain (left) and Frequency-domain (right)

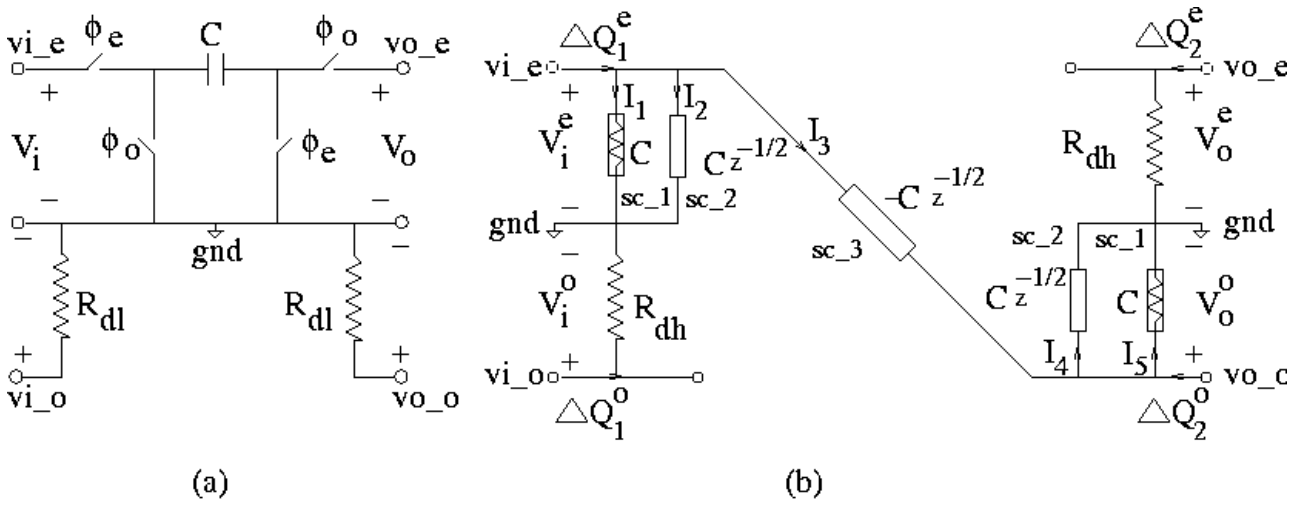

Fig. 3. Tooggle switched inverter (TSI) circuit, time-domain (left) and frequency-domain (right)

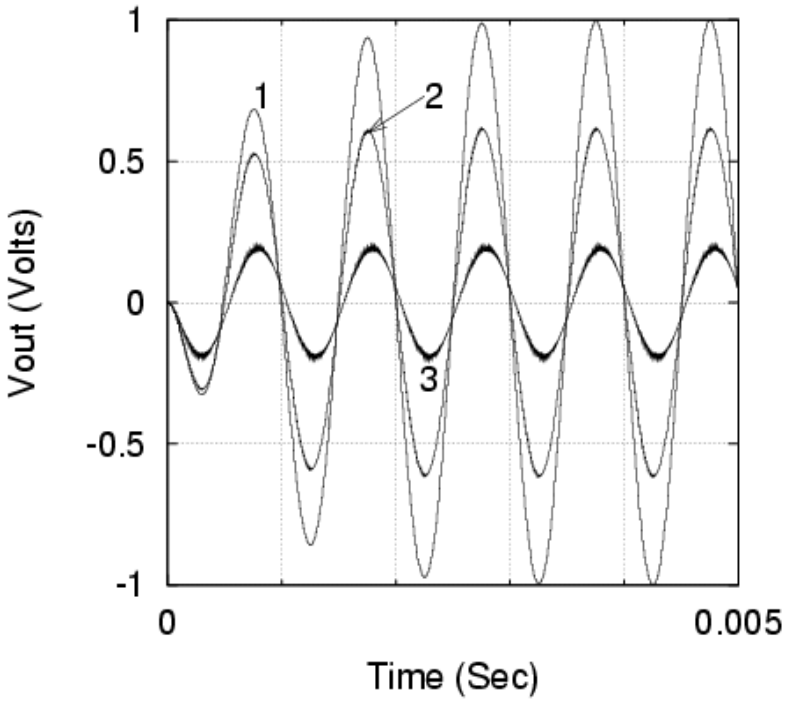

Fig. 4. Transient response showing output signal for different values of Rin (op-amp input resistance) and Av (op-amp voltage gain); (1) Rin = 10^{12}, Av= 10^5, (2) Rin = 10^4, Av= 10^5, (3) Rin = 10^4, Av= 10^4.

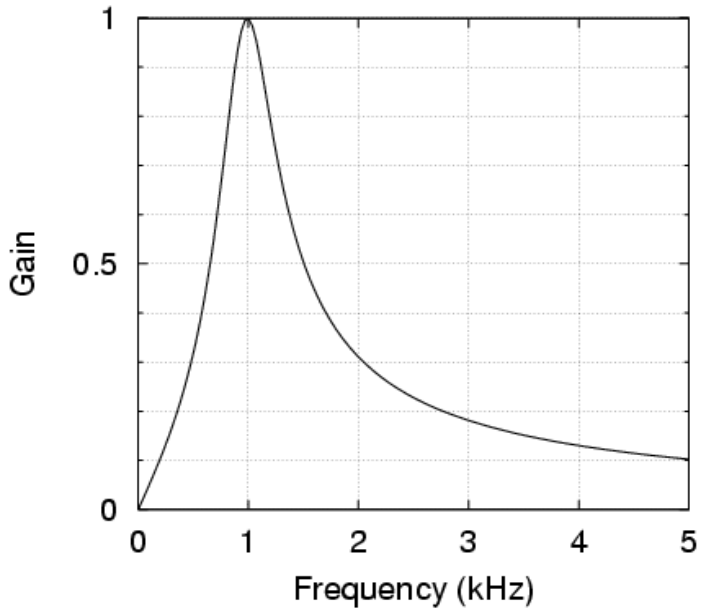

Fig. 5. Frequency-domain Response plotted after output voltage converted into gain.