Transient and Frequency Response Simulation of First-Order

Low-pass Switched-Capacitor Circuit (Biphase)

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Circuit file: sc_lpf.in

Fig.1 shows the low-pass switched capacitor network. This circuit is simulated here in both domains, Frequency and Time. It is viewed as a cascade of two blocks, namely Toggle Switched-capacitor (TSC) on left and Single Phase Grounded Capacitor (SPGC) on right.

One such block is shown in Fig.2 with its Time-domain (a) and Frequency-domain (b) equivalent circuits. As shown in the Fig.2, time-domain circuit is two-port (don't consider the nodes connected with low-value resistance (Rdl)), where as its frequency-domain (z-domain) equivalent circuit consists of four ports. Unused ports or nodes are connected with low-value resistance (Rdl) in Time-domain and High-value resistance (Rdh) in frequency-domain to avoid matrix to become singular.

All commonly found blocks are described as compound elements in SEQUEL with separate time-domain and frequency-domain description. Frequency-domain description assumes ideal elements and equal phase intervals. Time-domain description permits study of non-ideal elements and unequal phase intervals.

The simulated transient and frequency domain response are shown in Fig. 3 and Fig. 4 respectively. The approach utilized here to generate frequency response for switched-capacitor networks is such that it provides frequency response (magnitude and phase responses) for even and odd phases separately. If both of them are nonzero for the frequency-range of interests then they should be combined together by adding real parts of both phase and the same for imaginary parts. Now both terms should added after squared and square root should be calculated. Now it could be converted to gain.

1. Circuit Block:

title: Simple (without op-amp) low pass filter

greal tc=0.01m roff=1e18 ron=1m tcby2 = 0.005m

* Define a global parameter tc (clock period), roff and ron (switch off and on

* resistances) and tcby2.

begin_circuit

eelement type=vsrcac p=a n=g a=1.0 f_hz=1k t0=0 phi=0

* This element produces sine-wave source with frequency 1 khz.

eelement name=src1 type=sc_source_2 vo_e=le vo_o=lo g=g

- + aux1=a tc=tcby2 dt=2n s_2=5.0u
- + tau_1=5.0u tau_2=5.0u
- * This element samples the sine wave generated above at one-half of clock
- * frequency for even and odd phase and it also constructs the frequency-domain
- * representation for both even and odd phase sampled sine wave.

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eelement type=sc_tsc_1
     vi_e=1e vi_o=1o vo_e=2e vo_o=2o g=g phi_e=phi_e phi_o=phi_o
+
+
     ron=ron roff=roff c=1p tc=tc
* This element is one of the commonly found blocks in SC networks. Here it is
* called as "Toggle Switched-capacitor (TSC)".
   eelement type=sc_spgc_2
+
     vi_e=2e vi_o=2o vo_e=3e vo_o=3o g=g phi_o=phi_o
+
     ron=ron roff=roff c=1p tc=tc
* This element is another commonly found block in SC networks. Here it is
* called as "Single Phase Grounded-capacitor (SPGC)". These two blocks together
* in cascade makes the complete circuit shown in Fig. 1.
  delement type=clock a=phi_e i0=1 t1=4.8u t2=5.2u t0=0
   delement type=clock a=phi_o i0=0 t1=5.2u t2=4.8u t0=0
* These two statements generate non-overlapping clock signal to make the
* switches on and off in even and odd phases.
  refnode=g
* Node g is defined as the reference node for node voltages.
   outvar:
+
     va=nodev_of_a vle=nodev_of_le vlo=nodev_of_lo
     va_ac=nodev_ac_of_a v1e_ac=nodev_ac_of_1e v1o_ac=nodev_ac_of_1o
+
     v2e=nodev_of_2e v2o=nodev_of_2o
+
     v2e_ac=nodev_ac_of_2e v2o_ac=nodev_ac_of_2o
+
     v3e=nodev_of_3e v3o=nodev_of_3o
+
     v3e_ac=nodev_ac_of_3e v3o_ac=nodev_ac_of_3o
     p1=dvar_of_phi_e p2=dvar_of_phi_o
* Definition of the output variables.
end_circuit
2. Solve Block 1:
begin solve
   solve_type=startup
   initial_sol initialize
  method: t_startup=0
* Do a "start-up" solution. As the initial guess for the
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- * Newton-Raphson iterations, use the "initialize" option.
- * Since we have not generated any solution prior to this,
- since we have not generated any boraction prior to the
- * the "initialize" option has to be used.

end_solve

3. Solve Block 2:

begin_solve

solve_type=trns
initial_sol previous

* Perform a transient simulation, using the previous solution (obtained in the last solve block) as the initial guess for the Newton-Raphson iterations. Note that "initial_sol" is * relevant only to get the transient simulation started (i.e., the very first time step). For subsequent time steps, the * solution obtained for the previous time step is always used * as the initial guess for the N-R iterations. begin_output filename=sc2a.dat limit_lines=300000 variables: v1e v3e end_output begin_output filename=sc2b.dat limit_lines=300000 variables: p1 p2 end_output * Specify which output files are to be generated and which output variables are to be written to each of the files. Note that we have asked for two files here, one for the analog variables of interest (v1e v3e) and the other for the digital variables (p1 and p2). The two types of variables cannot be written to a single file. * Note that limit lines has been specified in the above files since the default value (10,000) is too small. The number of lines which get written to the output files is larger than this default value, and this would cause the program to stop before the specified end time is reached. method: norm_2=1.0e-5 itmax_trns=300000 back_euler=yes t_start=0 t_end=1m delt_const=0.1u delt_min=1n + * Specify the RHS norm ("tolerance"). The default value of norm_2 is 1.0e-10. However, that turns out to be too rigid for this problem and hence the need to change it. * Use the backward Euler method with a constant time step of * 100 nsec. * Specify the starting and ending times, and time step. * Note that itmax_trns has been specified since the default value (10,000) is too small; the number of time points required * for this simultion is larger than the default itmax_trns. end_solve 4. Solve Block 3: begin solve solve_type=ac vary_freq from 1 to 10k type=log n_points=250

* Above two statements perform AC analysis. The complete frequency range of

* interest is divided in two parts. The first range is evaluated here with * frequency points chosen in logarithmic fashion with number of points 250. begin_output filename=sc2ac1.dat variables: + mag_of_vle_ac phase_of_vle_ac mag_of_vlo_ac phase_of_vlo_ac + mag_of_v3e_ac phase_of_v3e_ac + + mag_of_v3o_ac phase_of_v3o_ac end_output Specify the output file and variables to be written. end_solve 5. Solve Block 4: begin_solve solve_type=ac vary_freq from 10k to 99k type=log n_points=100 * Above two statements perform AC analysis for second range of frequency with number of points 100. This helps to get a higher resolution in the * appropriate frequency range. begin_output filename=sc2ac1.dat append=yes variables: mag_of_vle_ac phase_of_vle_ac + mag_of_vlo_ac phase_of_vlo_ac + mag_of_v3e_ac phase_of_v3e_ac + mag_of_v3o_ac phase_of_v3o_ac + end_output Specify the same output file and variables to be written, which are mentioned for first frequency range (Solve Block 3). Indicate "Append" to add the data. end_solve end cf

Results:

In this example, simulated transient and frequency domain response are shown in Figs. 3 and 4, respectively.

Reference:

[1]K. R. Laker, "Equivalent circuits for the analysis and synthesis of switchedcapacitor networks," Bell Syst. Tech. J., vol. 58, pp. 727-767, Mar. 1979.

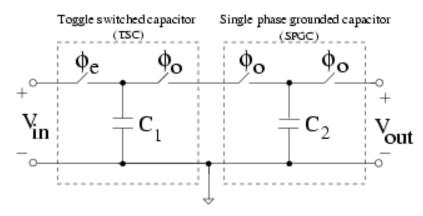
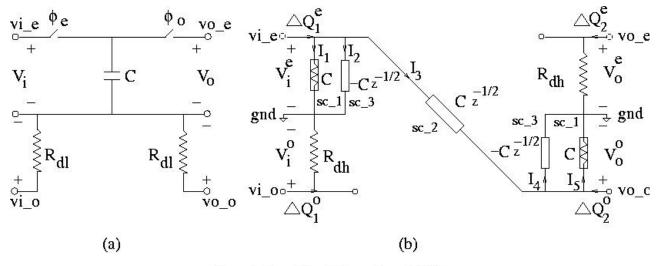


Fig. 1. Low-Pass SC Filter



Toggle Switched Capacitor (TSC)

Fig. 2. Toggle Switched-Capacitor circuit, time-domain (left) and frequency-domain (right).

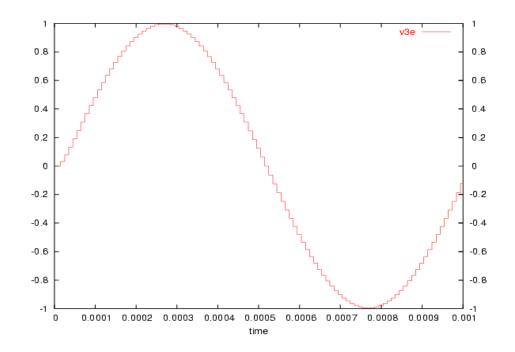


Fig. 3. Time-domain response showing output signal.

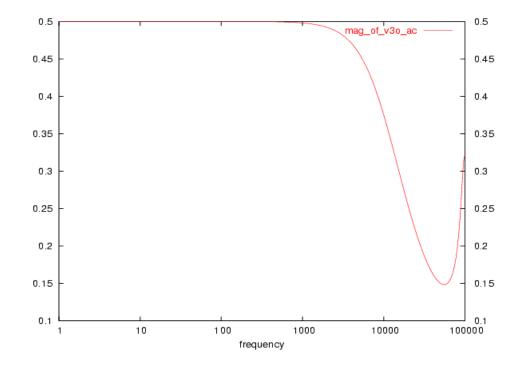


Fig. 4. Frequency-domain response plotted on logarithmic X-axis scale.