Transient and Frequency Response Simulation of Fifth-Order Low-pass Switched-Capacitor Circuit (Biphase)

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Circuit file: sc_lpf_5th_3.in

Fig.1 shows the 5th-order low-pass switched capacitor network with all parameters. This circuit is simulated here in both domains, Frequency and Time. It is viewed as a connection of many commonly found SC blocks, namely series odd switch (sc_swo), parallel even switch (sc_swpe), Floating capacitor (Float_cap) and Grounded capacitor (ground_cap), Switched-capacitor opamp (sc_opamp2, without diode) and Switched-capacitor Buffer (sc_bu).

One such block is shown in Fig. 2 with its Time-domain (a) and Frequency-domain (b) equivalent circuits. As shown in the Fig.2, time-domain circuit is two-port (don't consider the nodes connected with low-value resistance (Rdl)), where as its frequency-domain (z-domain) equivalent circuit consists of four ports. Unused ports or nodes are connected with low-value resistance (Rdl) in Time-domain and High-value resistance (Rdh) in frequency-domain to avoid matrix to become singular.

All commonly found blocks are described as compound elements in SEQUEL with separate time-domain and frequency-domain description. Frequency-domain description assumes ideal elements and equal phase intervals. Time-domain description permits study of non-ideal elements and unequal phase intervals.

The simulated transient and frequency domain response are shown in Fig. 3 and Fig. 4 respectively. The approach utilized here to generate frequency response for switched-capacitor networks is such that it provides frequency response (magnitude and phase responses) for even and odd phases separately. If both of them are nonzero for the frequency-range of interests then they should be combined together by adding real parts of both phase and the same for imaginary parts. Now both terms should added after squared and square root should be calculated. Now it could be converted to gain.

1. Circuit Block:

```
title: 5th order low pass filter

greal tc=0.0312m roff=1e18 ron=1m rinop=1e18 av=1e5 tcby2 = 0.015625m

*  Define a global parameter tc (clock period), roff and ron (switch off and on
*  resistances), rin (input resistance) and av (voltage gain) of op-amp and
*  tcby2.

begin_circuit
   eelement type=vsrcac p=a n=g a=1 f_hz=1k t0=0 phi=0

*  This element produces sine-wave source with frequency 1 khz.

   eelement name=src1 type=sc_source_2 vo_e=1e vo_o=1o g=g
+     aux1=a tc=tcby2 dt=100n s_2=15.6u
+     tau_1=15.6u tau_2=15.6u
```

```
*  This element samples the sinewave generated above at one-half of clock
*  frequency for even and odd phase and it also constructs the frequency-domain
*  representation for both even and odd phase sampled sinewave.


   eelement type=sc_swo
+     vi_e=1e vi_o=1o vo_e=2e vo_o=2o g=g  phi_o=phi_o
+     ron=1m roff=roff

*  This element implements series odd phase switch.

   eelement type=sc_swpe
+     vi_e=2e vi_o=2o vo_e=3e vo_o=3o g=g phi_e=phi_e
+     ron=1m roff=roff

*  This element implements parallel even phase switch.

   eelement type=sc_float_cap
+     vi_e=3e vi_o=3o vo_e=4e vo_o=4o g=g
+      c=0.566692p tc=tc

*  This element implements floating capacitor.

   eelement type=sc_swpe
+     vi_e=4e vi_o=4o vo_e=5e vo_o=5o g=g phi_e=phi_e
+     ron=1m roff=roff

*  This element implements parallel even phase switch.

   eelement type=sc_float_cap
+     vi_e=5e vi_o=5o vo_e=6e vo_o=6o g=g
+      c=1.25575p tc=tc

*  This element implements floating capacitor.

   eelement type=sc_swpe
+     vi_e=6e vi_o=6o vo_e=7e vo_o=7o g=g phi_e=phi_e
+     ron=1m roff=roff

*  This element implements parallel even phase switch.

   eelement type=sc_swo
+     vi_e=7e vi_o=7o vo_e=8e vo_o=8o g=g  phi_o=phi_o
+     ron=1m roff=roff

*  This element implements series odd phase switch.

   eelement type=sc_float_cap
+     vi_e=8e vi_o=8o vo_e=9e vo_o=9o g=g
+      c=1.58619p tc=tc

*  This element implements floating capacitor.

   eelement type=sc_swo
+     vi_e=9e vi_o=9o vo_e=10e vo_o=10o g=g  phi_o=phi_o
+     ron=1m roff=roff
```

```
*  This element implements series odd phase switch.

   eelement type=sc_swe
+     vi_e=10e vi_o=10o vo_e=11e vo_o=11o g=g  phi_e=phi_e
+     ron=1m roff=roff

*  This element implements series even phase switch.

   eelement type=sc_float_cap
+     vi_e=10e vi_o=10o vo_e=12e vo_o=12o g=g
+      c=1.62988p tc=tc

*  This element implements floating capacitor.

   eelement type=sc_swe
+     vi_e=12e vi_o=12o vo_e=13e vo_o=13o g=g  phi_e=phi_e
+     ron=1m roff=roff

*  This element implements series even phase switch.

   eelement type=sc_swo
+     vi_e=12e vi_o=12o vo_e=11e vo_o=11o g=g  phi_o=phi_o
+     ron=1m roff=roff

*  This element implements series odd phase switch.

   eelement type=sc_ground_cap
+     vi_e=13e vi_o=13o vo_e=14e vo_o=14o g=g
+     c=1.58619p tc=tc

*  This element implements grounded capacitor.

   eelement type=sc_float_cap
+     vi_e=5e vi_o=5o vo_e=15e vo_o=15o g=g
+      c=0.50898p tc=tc

*  This element implements floating capacitor.

   eelement type=sc_swpe
+     vi_e=15e vi_o=15o vo_e=16e vo_o=16o g=g phi_e=phi_e
+     ron=1m roff=roff

*  This element implements parallel even phase switch.

   eelement type=sc_float_cap
+     vi_e=15e vi_o=15o vo_e=17e vo_o=17o g=g
+      c=3.49058p tc=tc

*  This element implements floating capacitor.

   eelement type=sc_swpe
+     vi_e=17e vi_o=17o vo_e=18e vo_o=18o g=g phi_e=phi_e
+     ron=1m roff=roff

*  This element implements parallel even phase switch.
```

```
    eelement type=sc_swo
+     vi_e=18e vi_o=18o vo_e=19e vo_o=19o g=g  phi_o=phi_o
+     ron=1m roff=roff

*  This element implements series odd phase switch.

   eelement type=sc_float_cap
+     vi_e=19e vi_o=19o vo_e=20e vo_o=20o g=g
+      c=1.58527p tc=tc

*  This element implements floating capacitor.

   eelement type=sc_swo
+     vi_e=20e vi_o=20o vo_e=21e vo_o=21o g=g  phi_o=phi_o
+     ron=1m roff=roff

*  This element implements series odd phase switch.

   eelement type=sc_swe
+     vi_e=21e vi_o=21o vo_e=22e vo_o=22o g=g  phi_e=phi_e
+     ron=1m roff=roff

*  This element implements series even phase switch.

   eelement type=sc_float_cap
+     vi_e=21e vi_o=21o vo_e=23e vo_o=23o g=g
+      c=1.39769p tc=tc

*  This element implements floating capacitor.

   eelement type=sc_swo
+     vi_e=23e vi_o=23o vo_e=22e vo_o=22o g=g  phi_o=phi_o
+     ron=1m roff=roff

*  This element implements series odd phase switch.

   eelement type=sc_swe
+     vi_e=23e vi_o=23o vo_e=24e vo_o=24o g=g  phi_e=phi_e
+     ron=1m roff=roff

*  This element implements series even phase switch.

   eelement type=sc_ground_cap
+     vi_e=24e vi_o=24o vo_e=25e vo_o=25o g=g
+     c=1.58527p tc=tc

*  This element implements grounded capacitor.

   eelement type=sc_float_cap
+     vi_e=16e vi_o=16o vo_e=26e vo_o=26o g=g
+      c=2.3622p tc=tc

*  This element implements floating capacitor.
```

```
   eelement type=sc_swpe
+     vi_e=26e vi_o=26o vo_e=27e vo_o=27o g=g phi_e=phi_e
+     ron=1m roff=roff

*  This element implements parallel even phase switch.

   eelement type=sc_swo
+     vi_e=27e vi_o=27o vo_e=28e vo_o=28o g=g  phi_o=phi_o
+     ron=1m roff=roff

*  This element implements series odd phase switch.

   eelement type=sc_ground_cap
+     vi_e=28e vi_o=28o vo_e=29e vo_o=29o g=g
+     c=1p tc=tc

*  This element implements grounded capacitor.

   eelement type=resistor p=28o n=g resist=roff

*  This element implements resistor.

   eelement name=op1 type=sc_opamp2 vi_ep=11e vi_em=8e vi_op=11o
+     vi_om=8o  vo_eo=9e vo_oo=9o  gnd=g
+     rin=rinop rout=1e-9

*  Above statement implements switched capacitor op-amp.
*  This op-amp consists of two op-amps one for each phase.

   eelement name=op2 type=sc_bu vi_e=13e  vi_o=13o
+     vo_e=11e vo_o=11o  gnd=g
+     rin=rinop rout=1e-9

*  Above statement implements switched capacitor buffer (unity gain).
*  This buffer consists of two buffers one for each phase.

   eelement name=op3 type=sc_opamp2 vi_ep=22e vi_em=19e vi_op=22o
+     vi_om=19o  vo_eo=20e vo_oo=20o  gnd=g
+     rin=rinop rout=1e-9

*  This statement implements switched capacitor op-amp.

   eelement name=op4 type=sc_bu vi_e=24e  vi_o=24o
+     vo_e=22e vo_o=22o  gnd=g
+     rin=rinop rout=1e-9

*  This statement implements switched capacitor buffer.

   delement type=clock a=phi_e i0=0 t1=16.25u t2=15u t0=0
   delement type=clock a=phi_o i0=1 t1=15u t2=16.25u t0=0

*  These two statements generate non-overlapping clock signal to make the
*  switches on and off in even and odd phases.

   refnode=g

*  Node g is defined as the reference node for node voltages.
```

```
   outvar:
+     va=nodev_of_a v1e=nodev_of_1e v1o=nodev_of_1o
+     va_ac=nodev_ac_of_a v1e_ac=nodev_ac_of_1e v1o_ac=nodev_ac_of_1o
+     v5e=nodev_of_5e v5o=nodev_of_5o
+     v5e_ac=nodev_ac_of_5e v5o_ac=nodev_ac_of_5o
+     v9e=nodev_of_9e v9o=nodev_of_9o
+     v9e_ac=nodev_ac_of_9e v9o_ac=nodev_ac_of_9o
+     v28e=nodev_of_28e v28o=nodev_of_28o
+     v28e_ac=nodev_ac_of_28e v28o_ac=nodev_ac_of_28o

*  Definition of the output variables.

end_circuit
```

2. Solve Block 1:

```
begin_solve
   solve_type=startup
   initial_sol initialize
   method: t_startup=0

*  Do a "start-up" solution. As the initial guess for the
*  Newton-Raphson iterations, use the "initialize" option.
*  Since we have not generated any solution prior to this,
*  the "initialize" option has to be used.

end_solve
```

3. Solve Block 2:

```
begin_solve
   solve_type=trns
   initial_sol previous

*  Perform a transient simulation, using the previous solution
*  (obtained in the last solve block) as the initial guess for
*  the Newton-Raphson iterations. Note that "initial_sol" is
*  relevant only to get the transient simulation started (i.e.,
*  the very first time step). For subsequent time steps, the
*  solution obtained for the previous time step is always used
*  as the initial guess for the N-R iterations.

   begin_output
      filename=sn_tr.dat limit_lines=20000000
      variables: v28e
   end_output

*  Specify which output files are to be generated and which
*  output variables are to be written to each of the files.
*  Note that we write here only analog variables of interest (v28e).
*  If we want to store digital variables, we should ask for one more file.
*  The two types of variables cannot be written to a single file.
*
*  Note that limit_lines has been specified in the above files
*  since the default value (10,000) is too small. The number
*  of lines which get written to the output files is larger
```

```
*  than this default value, and this would cause the program
*  to stop before the specified end time is reached.

   method: norm_2=1.0e-5 itmax_trns=10000000 back_euler=yes
+    t_start=0 t_end=2.5m delt_const=0.1u delt_min=5n

*  Specify the RHS norm ("tolerance"). The default value of
*  norm_2 is 1.0e-10. However, that turns out to be too rigid
*  for this problem and hence the need to change it.

*  Use the backward Euler method with a constant time step of
*  0.1 usec.

*  Specify the starting and ending times, and time step.
*  Note that itmax_trns has been specified since the default
*  value (10,000) is too small; the number of time points required
*  for this simultion is larger than the default itmax_trns.

end_solve
```

4. Solve Block 3:

```
begin_solve
   solve_type=ac
   vary_freq from 1 to 3k type=log n_points=500

*  Above two statements perform AC analysis. The complete frequency range of
*  interest is divided in four parts. The first range is evaluated here with
*  frequency points chosen in logarithmic fashion with number of points 500.

   begin_output
      filename=sn_fr.dat
      variables:
+       mag_of_v28e_ac phase_of_v28e_ac
+       mag_of_v28o_ac phase_of_v28o_ac
   end_output

*  Specify the output file and variables to be written.

end_solve
```

5. Solve Block 4:

```
begin_solve
   solve_type=ac
   vary_freq from 3k to 3.4k type=log n_points=100

*  Above two statements perform AC analysis for second range of frequency
*  with number of points 100.

   begin_output
      filename=sn_fr.dat append=yes
      variables:
+       mag_of_v28e_ac phase_of_v28e_ac
+       mag_of_v28o_ac phase_of_v28o_ac
   end_output
```

```
*  Specify the same output file and variables to be written, which are mentioned
*  for first frequency range (Solve Block 3). Indicate “Append” to add the data.

end_solve
```

6. Solve Block 5:

```
begin_solve
   solve_type=ac
   vary_freq from 3.4k to 6k type=log n_points=400

*  Above two statements perform AC analysis for third range of frequency
*  with number of points 400.

   begin_output
      filename=sn_fr.dat append=yes
      variables:
+       mag_of_v28e_ac phase_of_v28e_ac
+       mag_of_v28o_ac phase_of_v28o_ac
   end_output

*  Specify the same output file and variables to be written, which are mentioned
*  for first frequency range (Solve Block 3). Indicate “Append” to add the data.

end_solve
```

7. Solve Block 6:

```
begin_solve
   solve_type=ac
   vary_freq from 6k to 10k type=log n_points=400

*  Above two statements perform AC analysis for fourth range of frequency
*  with number of points 400.

   begin_output
      filename=sn_fr.dat append=yes
      variables:
+       mag_of_v28e_ac phase_of_v28e_ac
+       mag_of_v28o_ac phase_of_v28o_ac
   end_output

*  Specify the same output file and variables to be written, which are mentioned
*  for first frequency range (Solve Block 3). Indicate “Append” to add the data.

end_solve
end_cf
```

Results:

In this example, simulated transient and frequency domain response are shown in Figs. 3 and 4, respectively.

References:

[1]K. R. Laker, “Equivalent circuits for the analysis and synthesis of switched-capacitor networks,” Bell Syst. Tech. J., vol. 58, pp. 727-767, Mar. 1979.

[2]Opal and J. Vlach, “Analysis and sensitivity of periodically switched linear networks,” IEEE Trans. Circuits and Syst., Vol. 36, No. 4, pp. 522-532, April –1989.

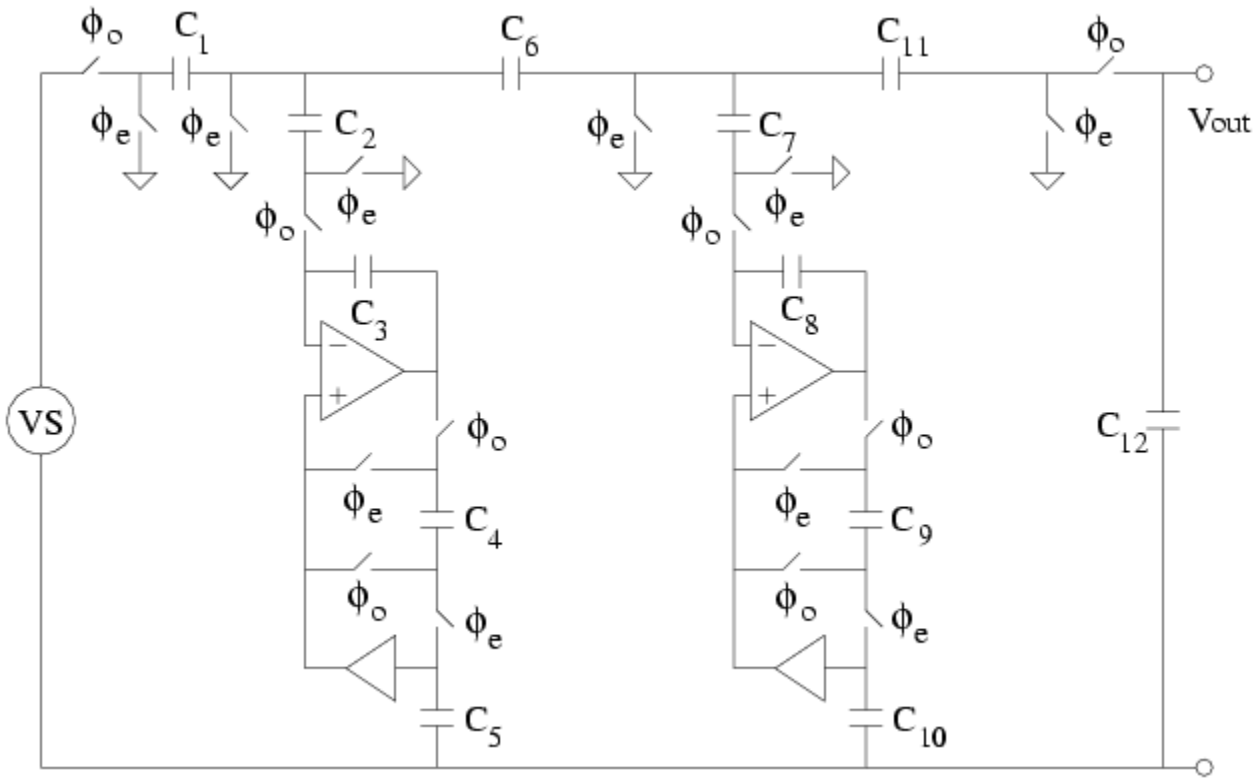

Fig. 1. Fifth-order Low-pass filter; the parameters are C_1 = 0.566692 pF, C_2 = 1.25575 pF, C_3 = 1.58619 pF, C_4 = 1.62988 pF, C_5 = 1.58619 pF, C_6 = 0.50898 pF, C_7 = 3.49058 pF, C_8 = 1.58527 pF, C_9 = 1.36769 pF, C_{10} = 1.58527 pF, C_{11} = 2.3622 pF, C_{12} = 1 pF, f_c = 32 kHz.

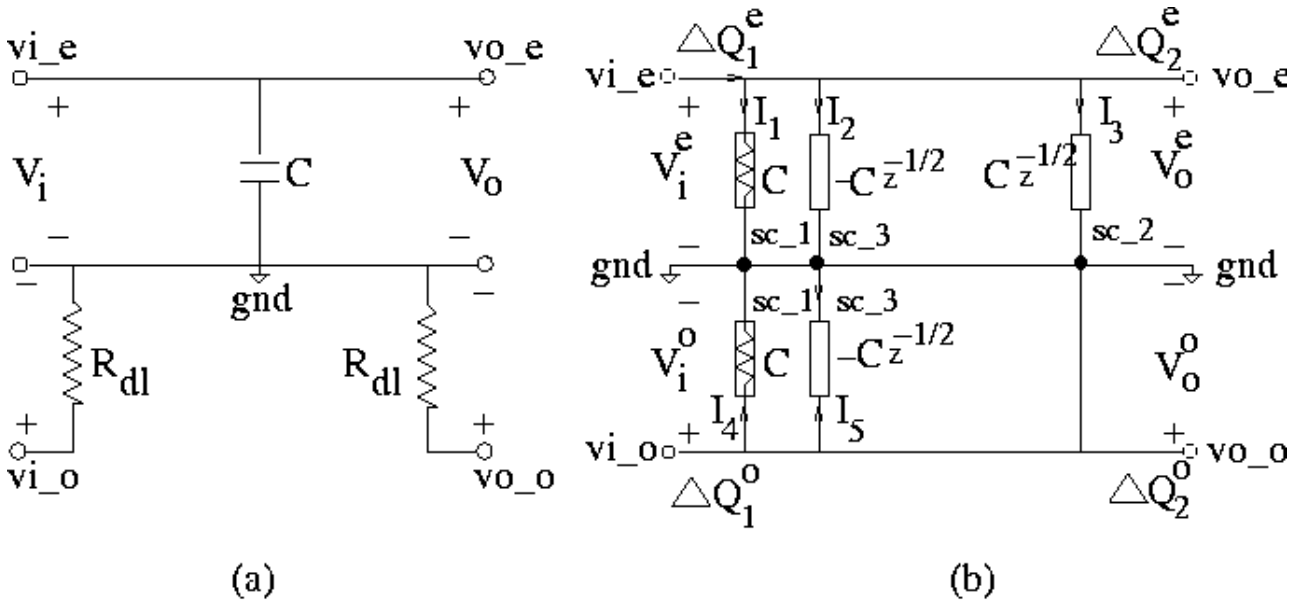

Fig. 2. Grounded capacitor (sc_ground_cap) circuit, time-domain (left) and frequency-domain (right).

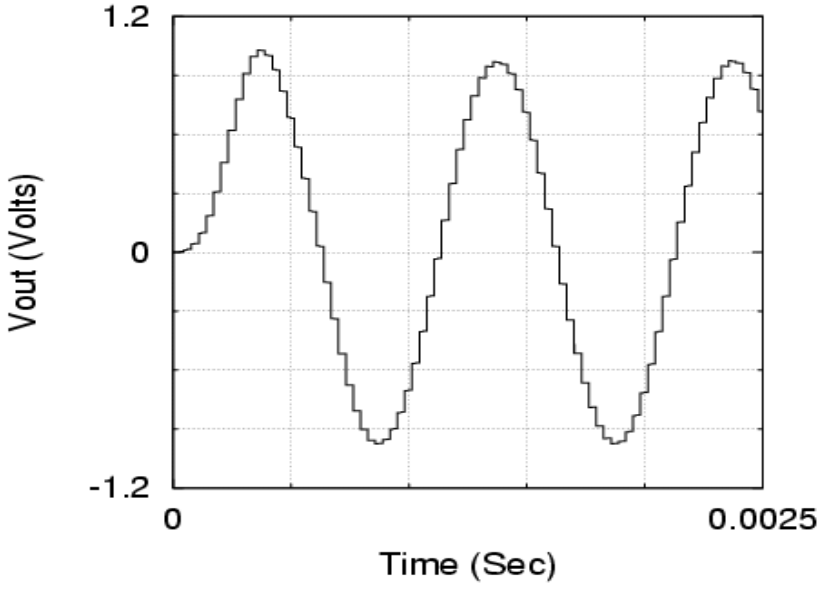

Fig. 3. Transient response showing output signal at node v28e to an input with frequency 1 kHz.

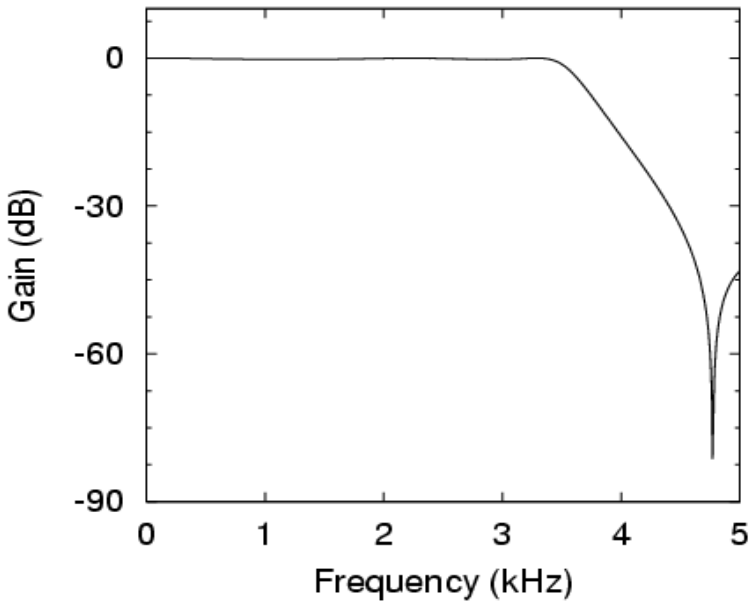

Fig. 4. Frequency-domain response.