Saurabh Lodha

Professor, Department of Electrical Engineering, IIT Bombay, Powai, Mumbai- 400076
Website: http://www.ee.iitb.ac.in/~slodha/
Email: slodha@ee.iitb.ac.in, Phone: +91-9819927460

Professional Positions

- **Institute chair Professor, Department of Electrical Engineering IIT Bombay, Dec 2018 – present**
  - ✓ Ge/GeSn and Ga_2O_3 devices for advanced CMOS and power electronics
  - ✓ 2D TMDC electronic and optoelectronic devices
- **Visiting Professor, Department of Precision and Micro Systems Engineering, TU Delft, Oct 2020 – Aug 2021**
- **Visiting Professor, Department of Applied Physics, TU Eindhoven, Oct 2020 – Aug 2021**
- **Associate Professor, Department of Electrical Engineering IIT Bombay, Sep 2014 – Dec 2018**
  - ✓ Ge/SiGe devices for advanced CMOS
  - ✓ 2D TMDC electronic devices
- **Assistant Professor, Department of Electrical Engineering IIT Bombay, July 2010 – Sep 2014**
  - ✓ Ge/SiGe devices for advanced CMOS
- **Member of Technical Staff, Logic Technology Development, Intel Corporation, Mar 2010 – June 2010**
  - ✓ Front-end transistor process R&D for Intel's 14 and 22 nm CMOS technologies
- **Senior Process Integration Engineer, Logic Technology Development, Intel Corporation, Apr 2005 – Mar 2010**
  - ✓ Front-end transistor process R&D for Intel's 45 (industry first Hi-K/MG) and 32 nm CMOS technologies
- **Graduate Research Assistant, School of Electrical and Computer Engg., Purdue University, Jan 2000 – Dec 2004**
  - ✓ Heterostructure molecular electronic devices (doctoral thesis) and contacts to III-V semiconductors (masters)
- **Graduate Teaching Assistant, School of Electrical and Computer Engg., Purdue University, Aug – Dec 1999**
  - ✓ Instructor for undergraduate electronic devices laboratory

Other Affiliations

- **Professor-in-charge,** IIT Bombay-Ohio State University Frontier Science and Engineering Research Center, Apr 2019 – present

Education

Ph.D. in Electrical and Computer Engineering, GPA- 4.00/4.00 **Aug 2001 – Dec 2004**
Purdue University West Lafayette, IN, USA
Thesis: An experimental study of molecular electronic devices
Advisor: Prof. David B. Janes

M.S. in Electrical and Computer Engineering, GPA- 3.92/4.00 **Aug 1999 – Dec 2001**
Purdue University West Lafayette, IN, USA
Thesis: Experimental and modeling studies of Schottky contacts to LTG:GaAs
Advisor: Prof. David B. Janes

Bachelor of Technology in Electrical Engineering, GPA- 8.99/10.00 **Jul 1995 – May 1999**
Indian Institute of Technology- Bombay, Mumbai, India
Thesis: Radiation and reverse bias stressing damage in Si-SiGe HBTs and Si BJTs
Advisor: Prof. Juzer Vasi

Awards and Recognitions

- KLC Memorial Distinguished Lecture Award, IIT Delhi, 2023
- Institute Chair Professor, IIT Bombay, 2021-2024
- Fellow, Indian National Academy of Engineering (INAE), 2021
- Young Career Award by DST Nano Mission, Govt. of India, 2020
- Senior Member, IEEE (Electron Devices Society), 2020
- Best paper, best manuscript and best poster awards, 4th IEEE ICEE, Bengaluru 2018
- Best research paper award, IIT Bombay, 2018
- Swarna Jayanti Fellowship (Engineering Sciences) from Dept. of Science and Technology, Govt. of India, 2017
- Ohio State University Global Partnership Award, 2016
- Malhotra Weikfield Foundation NanoScience Fellowship Award to PhD student Naveen Kaushik, 2016
- Best paper award, IEEE Indicon (Mumbai), 2013
- Young Investigator Award, IIT Bombay, 2012

- Paper shortlisted for best paper award, IEEE VLSI-TSA (Taiwan), 2014
- DST SERC project rated "Excellent" by EECS review committee, 2014
- Applied Materials Awards for collaborative research, 2011 and 2012
- Five Intel Logic Technology Awards for outstanding contributions to development of 45nm and 32nm CMOS Technologies (Intel Corporation) (2006, 2008, 2008, 2009, 2010)
- Outstanding Process Integration Engineer (Intel Corporation) for the year 2008-2009
- Undergraduate thesis nominated for the "most outstanding B. Tech. Project" by the EE Dept., IIT Bombay (1999)
- National Merit Scholarship for academic excellence, Govt. of India (1994)

Sponsored Research Grants (Government of India (GOI) and Industry)

Sponsoring Agency	Title of project	Period
As Principal Investigator		
DST SERB	Wafer-scale and area-selective ALD of 2D semiconductors and high-k dielectrics for advanced semiconductor technologies	'22-'24
MeitY, GOI	Indian Nanoelectronics Users' Program – Idea to Innovation	'21-'24
NWO, Netherlands	Agricultural and environmental 2D gas sensors	'20-'21
Applied Materials (PI)	Fast ALD for Thick Dielectrics	'19-'21
*DST (Swarnajayanti)	High Speed 2D Electronic and Optoelectronic Devices	'18-'23
*MeitY, DST (PI- one out of three)	Nanoelectronics Network for Research and Applications (NNetRA)	'18-'21
MeitY, GOI (PI- one out of three)	Indian Nanoelectronics Users' Program (Phase II)	'14-'19
Applied Materials (PI)	ALD Process Development for Carbon and Low-K Dielectrics	'18-'19
DST, GOI (PI)	Silicon Solar Cells with Carrier Selective Contacts	'16-'19
Applied Materials (PI)	Si/SiGe/Ge Vertical Gate All Around Transistor Pathfinding Project	'13-'18
Applied Materials (PI)	ALE hardware and process devpt.	'16-'18
Danish Agency for Science, Technology and Innovation	Electron transport in advanced semiconductor materials	'15-'16
DST, GOI (PI) (rated "Excellent")	Ge-based device development for sub-22nm node CMOS logic	'11-'14
Applied Materials (PI)	Ge Transistor Pathfinding Project	'11-'13
As Co-Principal Investigator		
DST Nano Mission	Emergent Phenomena in 2D Heterostructures	'20-'25
MHRD, GOI (co-PI, one out of two)	IIT Bombay Research Park	'15-'20
Applied Materials (co-PI)	Material screening for memory and logic application	'13-'16
DST, GOI (co-PI, one out of three)	Dielectrics & their integration into Nanoscale logic and memory devices	'12-'16
DST, GOI (co-PI)	Monolithic Integration of High-Performance Germanium based Infrared Detector on Silicon	'13-'16

DST, GOI (co-PI)	Inkjet Printed Flexible Thin TFTs	'13-'16
DST, GOI (co-PI)	Nanoscale Selection Device Dev for sub-20nm node High-Density Embedded Non-Volatile Memory	'11-'14
Synopsys Inc. (co-PI, one out of four)	Modelling and simulation of Germanium-based devices	'11-'13
As Investigator		
DeitY, GOI	Centre of Excellence in Nano-electronics (Phase II)	'12-'17
MNRE, GOI	NCPRE Phase II	'16-'21

*DST: Department of Science and Technology, Govt. of India

*MeitY: Ministry of Electronics and Information Technology, Govt. of India

Book Chapters

1. N. Kaushik, S. Grover, M. Deshmukh and **S. Lodha**, "Metal contacts to MoS_2" in "2D Inorganic Materials beyond Graphene" edited by Prof. Umesh Waghmare and Prof. C. N. R. Rao, World Scientific Publishing (2018).
2. K. Thakar and **S. Lodha**, "2D Materials for Optoelectronics" in "2D Materials for Electronics, Sensors and Devices: Synthesis, Characterization, Fabrication and Application", edited by Prof. Saptarshi Das (Penn State Univ.), Elsevier (2022).

International Journal Publications (Total: 88, h-index: 32, i10-index: 68, 4547 citations as per Google Scholar on 16 Mar 2023)

1. N. Manikanthababu, C. Joishi, J. Biswas, K. Prajna, K. Asokan, J. V. Vas, R. Medwal, R. C. Meena, **S. Lodha**, and R. Singh, "Ion irradiation-induced interface mixing and the charge trap profiles investigated by in situ electrical measurements in Pt/Al2O3/β-Ga_2O_3 MOSCAPs", to appear in IEEE Transactions on Electron Devices, 2023
2. H. Jawa, N. Khandare, A. Varghese, S. Sahoo, **S. Lodha**, "Enhanced Photoresponse of a Dielectric-free Suspended WSe_2-ReS_2 Heterostructure Photodetector, Applied Physics Letters, 122 (12), 121105, 2023.
3. R. Lengare, C. Joishi, S. Lodha, "Electrostatic Engineering of β-Ga_2O_3 Trench Metal–Insulator–Semiconductor Schottky Barrier Diodes Using a Bilayer Dielectric Stack", IEEE Transactions on Electron Devices, 69, 10, 5476-5483, 2022. (IF:2.92)
4. H. Jawa, A. Varghese, S. Ghosh, S. Sahoo, Y. Yin, N. Medhekar, **S. Lodha**, "Wavelength-Controlled Photocurrent Polarity Switching in BP-MoS2 Heterostructure", Advanced Functional Materials, 32 (25), 2112696, 2022. (IF: 18.81)
5. A. Varghese, Y. Yin, M. Wang, **S. Lodha**, and N. V. Medhekar, "Near-Infrared and Visible-range Optoelectronics in 2D Hybrid Perovskite/Transition Metal Dichalcogenide Heterostructures", Advanced Materials Interfaces, 9 (14), 2102174, 2022. (IF:6.15)
6. S. Ghosh, A. Varghese, H. Jawa, Y. Yin, N. V. Medhekar, and **S. Lodha**, "Polarity-Tunable Photocurrent through Band Alignment Engineering in a High-Speed WSe_2/$SnSe_2$ Diode with Large Negative Responsivity", ACS Nano, 16, 3, 4578–4587, 2022. (IF: 15.88)
7. P Tiwari, J, Biswas, C. Joishi, **S. Lodha**, "Nb_2O_5 high-k dielectric enabled electric field engineering of β-Ga_2O_3 metal-insulator-semiconductor (MIS) diode" Journal of Applied Physics, 130 (24), 245701, 2021. (IF: 2.55)
8. K. Thakar and **S. Lodha**, "Multi-Bit Analog Transmission Enabled by Electrostatically Reconfigurable Ambipolar and Anti-Ambipolar Transport", ACS Nano, 15 (12), 19692-19701, 2021. (IF: 15.88)
9. D. Saha and **S. Lodha**, "First-principles based simulations of electronic transmission in ReS2/WSe2 and ReS_2/$MoSe_2$ type-II vdW heterointerfaces", Scientific Reports, 11 (1), 1-10, 2021. (IF: 4.38)
10. S. Nayak, **S. Lodha**, S. Ganguly, "Stress Engineering for Drive Current Enhancement in Silicon Carbide (SiC) Power MOSFETs", IEEE Journal of the Electron Devices Society, vol. 9, pp. 876-880, 2021. (IF: 2.66)
11. S. Ghosh, A. Varghese, S. Dhara, K. Thakar and **S. Lodha,** "Enhanced responsivity and detectivity of fast WSe_2 phototransistor using electrostatically tunable in-plane lateral p-n homojunction", Nature Communications 12 (1), 1-9, 2021. (IF: 14.92, 35 citations)
12. S. Dhara, H Jawa, S Ghosh, A Varghese, D Karmakar, **S. Lodha**, "All-Electrical High-Sensitivity, Low-Power Dual-Mode Gas Sensing and Recovery with a WSe2/MoS2 pn Heterodiode", ACS Applied Materials and Interfaces, 13 (26), 30785-30796, 2021. (IF 9.23)
13. S. Nayak, B. SanthiBhushan, **S. Lodha**, S. Ganguly, "Silicon carbide planar junctionless transistor for low-medium voltage power electronics", Journal of Physics Communications 5 (2), 025009, 2021. (IF: 1.2)
14. H. Jawa, A. Varghese, **S. Lodha**, "Electrically Tunable Room Temperature Hysteresis Crossover in Underlap MoS_2 FETs", ACS Applied Materials and Interfaces, 13, 7, 9186–9194, 2021. (IF: 9.23)
15. A. Tyagi, J. Biswas, A. Kottantharayil, K. Ghosh, **S. Lodha**, "Performance Analysis of Silicon Carrier Selective Contact Solar Cells with ALD MoOx as Hole Selective Layer", Silicon, 1-8, 2021. (IF: 2.67)

16. J. Biswas, G. Bajaj, A. Tyagi, P. Goradia, **S. Lodha**, "Tunable optical and electrical properties of thermal and plasma-enhanced atomic layer deposited Si-rich $Si_xTi_{1-x}O_2$ thin films", Journal of Applied Physics, 129 (5), 055303, 2021. (IF:2.55)
17. D. Biswas, C. Joishi, J. Biswas, P. Tiwari, **S. Lodha**, "Charge trap layer enabled positive tunable V_{fb} in β-Ga_2O_3 gate stacks for enhancement mode transistors", Applied Physics Letters, 117, 172101, 2020. (IF:3.79)
18. C. Joishi, Z. Xia, J.S. Jamison, S.H. Sohel, R.C. Myers, **S. Lodha**, S. Rajan, "Deep-Recessed β-Ga_2O_3 Delta-Doped Field-Effect Transistors With In Situ Epitaxial Passivation", IEEE Transactions on Electron Devices, 67, 11, 4813-4819, 2020. (IF: 2.92)
19. A. Varghese, D. Saha, K. Thakar, V. Jindal, S. Ghosh, N. Medhekar, S. Ghosh, **S. Lodha**, "Near-direct bandgap WSe_2/ReS_2 type-II pn heterojunction for enhanced ultrafast photodetection and high-performance photovoltaics", Nano Letters, 20, 3, 1707-1717, 2020. (IF: 11.19, 99 citations)
20. P. Kumar, K. Thakar, N. C. Verma, J. Biswas, T. Maeda, A. Roy, K. Kaneko, C. K. Nandi, **S. Lodha**, V. Balakrishnan, "Polymorphic In-Plane Heterostructures of Monolayer WS_2 for Light-Triggered Field Effect Transistors", ACS Applied Nano Materials, 3, 4, 3750-3759, 2020. (IF: 4.86)
21. S. Dev, K. Khiangte, **S. Lodha**, "Wafer-scale mono-crystalline GeSn alloy on Ge by sputtering and solid phase epitaxy", Journal of Physics D, 53, 21, 2020. (IF: 3.21)
22. N. Goyal, D. M. A. Mackenzie, V. Panchal, H. Jawa, O. Kazakova, D. H. Petersen, **S. Lodha**, "Enhanced thermally aided memory performance using few-layer ReS_2 transistors", 116 (5), 052104, Applied Physics Letters, 2020. (IF:3.79)
23. D. Saha, A. Varghese and **S. Lodha**, "Atomistic Modeling of van der Waals Heterostructures with Group-6 and Group-7 Monolayer Transition Metal Dichalcogenides for Near Infrared/Short-wave Infrared Photodetection" ACS Applied Nano Materials, 3 (1), 820-829, 2020. (IF: 4.86)
24. S. Dev, N. Pradhan, N. Variam and **S. Lodha**, "Impact of N_2 Co-implant on Phosphorus Diffusion and Activation for n^+/p Ge Junctions", IEEE Transactions on Electron Devices, 67 (2), 419-423, 2020. (IF:2.92)
25. K. Thakar and **S. Lodha**, ""Optoelectronic and Photonic Devices based on Transition Metal Dichalcogenides", invited review article in special issue of Materials Research Express, 7 (1), 014002, 2020. (IF: 1.62, 67 citations)
26. J. F. McGlone, Z. Xia, C. Joishi, **S. Lodha**, S. Rajan, S. A. Ringel, and A. R. Arehart, "Identification of Critical Buffer Traps in Si Delta-doped β-Ga_2O_3 MESFETs", Applied Physics Letters, 115 (15), 153501, 2019. (IF:3.79, 33 citations)
27. N. Goyal, S. Mahapatra and **S. Lodha**, "Ultra-fast Characterization of Hole Trapping Near Black Phosphorus (BP)/SiO_2 Interface During NBTI Stress in 2D BP p-FETs," (Invited Paper) IEEE Transactions on Electron Devices, 66 (11), 4572-4577, 2019. (IF:2.92)
28. K. Deka, A. Guleria, D. Kumar, J. Biswas, **S. Lodha**, S. D. Kaushik, S. Dasgupta, P. Deb, "Exclusive T2 MRI contrast enhancement by mesoporous carbon framework encapsulated manganese oxide nanoparticles", Current Applied Physics 20 (1), 89-95, 2019. (IF: 2.48)
29. S. Dev and **S. Lodha**, "Process Variation-Induced Contact Resistivity Variability in Nanoscale MS and MIS Contacts", IEEE Transactions on Electron Devices, vol. 66, no. 10, 4320 - 4325, 2019. (IF:2.92)
30. P. Kumar, J. Biswas, J. Pandey, K. Thakar, A. Soni, **S. Lodha** and V. Balakrishnan "Selective oxidation of WS_2 defect domain with sub monolayer thickness leads to multi-fold enhancement in Photoluminescence" Advanced Material Interfaces, 1900962, 6 (20), 2019. (IF:6.15)
31. N. Goyal, N. Parihar, H. Jawa, S. Mahapatra, **S. Lodha** "Accurate Threshold Voltage Reliability Evaluation of Thin Al_2O_3 Top Gate Dielectric Black Phosphorous FETs Using Ultrafast Measurement Pulses", ACS Applied Materials and Interfaces, 11, 26, 23673-23680, 2019. (IF:9.23)
32. C. Joishi, Y. Zhang, Z. Xia, W. Sun, A. R. Arehart, S. Ringel, **S. Lodha**, and S. Rajan, "Breakdown characteristics of β-$(Al_{0.22}Ga_{0.78})_2O_3/Ga_2O_3$ field-plated modulation doped field effect transistors with SiNx passivation", IEEE Electron Device Letters, 40 (8), 1241-1244, 2019. (IF:4.5, 72 citations)
33. Z. Xia, H. Xuu, C. Joishi, J. McGlone, N. K. Kalarickal, S. H. Sohel, M. Brenner, S. Ringel, **S. Lodha,** W. Lu, S. Rajan, "β-Ga_2O_3 Delta-Doped Field Effect Transistors with Current Gain Cutoff Frequency of 27 GHz", IEEE Electron Device Letters, 40 (7), 1052-1055, 2019. (IF:4.5, 113 citations)
34. D. Biswas, C. Joishi, J. Biswas, K. Thakar, S. Rajan, and **S. Lodha**, "Enhanced n-type β-Ga_2O_3 (-201) gate stack performance using Al_2O_3/SiO_2 bi-layer dielectric", Applied Physics Letters, 114, 212106, 2019. (IF:3.79, 22 citations)
35. J. Biswas, N. Pradhan, D. Biswas, S. Das, S. Mahapatra, **S. Lodha**, "Impact of punch-through stop implants on channel doping and junction leakage for Ge p-FinFET applications", IEEE Transactions on Electron Devices, 66 (4), 1635-1641, 2019. (IF:2.92)
36. A. Tyagi, K. Ghosh, A. Kottantharayil, **S. Lodha**, "An Analytical Model for the Electrical Characteristics of Passivated Carrier- Selective Contact Solar Cell", IEEE Transactions on Electron Devices, 66 (3), 1377-1385, 2019. (IF:2.92)
37. K. Deka, A. Guleria, D. Kumar, J. Biswas, **S. Lodha**, S. Kaushik, S. Choudhary, S. Dasgupta and P. Deb, "Janus Nanoparticles for Contrast Enhancement of T1-T2 Dual Mode Magnetic Resonance Imaging", Dalton Transactions, 48 (3), 1075-1083 (2019). (IF:4.39)
38. K. Thakar, B. Mukherjee, S. Grover, N. Kaushik, M. Deshmukh, **S. Lodha**, ""Multilayer ReS_2 Photodetectors with Gate Tunability for High Responsivity and High-Speed Applications", ACS Applied Materials and Interfaces, 10 (42), 36512 (2018). (IF:9.23, 54 citations)

39. K. Saikia, K. Bhattacharya, D. Sen, S. D. Kaushik, J. Biswas, **S. Lodha**, B. Gogoi, A. K. Buragohain, W. Kockenberger, P. Deb, "Solvent evaporation driven entrapment of magnetic nanoparticles in mesoporous frame for designing a highly efficient MRI contrast probe", Applied Surface Science, 464, 567-576 (2018). (IF:6.71)
40. C. Joishi, Z. Xia, J. MacGlone, Y. Zhang, A. R. Arehart, S. Ringel, **S. Lodha**, S. Rajan, "Effect of Buffer Iron Doping on Delta-Doped β-Ga_2O_3 Metal Semiconductor Field Effect Transistors", Applied Physics Letters, 113, 123501 (2018). (IF: 3.79, 54 citations)
41. C. Joishi, S. Ghosh, S. Kothari, N. Parihar, S. Mukhopadhyay, S. Mahapatra, **S. Lodha**, "Understanding PBTI in replacement metal gate Ge n-channel FETs with ultrathin Al_2O_3 and GeO_x ILs using ultrafast charge trap-detrap techniques", IEEE Transactions on Electron Devices, 65 (10), 4245-4253 (2018). (IF:2.92)
42. D. Vaidya, **S. Lodha**, S. Ganguly, "Electrical-equivalent van der Waals gap for two-dimensional bilayers", Physical Review Applied, 10 (3), 034070 (2018). (IF:4.98)
43. S. Singh, K. Thakar, N. Kaushik, B. Muralidharan, **S. Lodha**, "Performance Projections for Two-dimensional Materials in Radio-Frequency Applications" Physical Review Applied, 10 (1), 014022 (2018). (IF:4.98)
44. N. Kaushik, S. Ghosh and **S. Lodha**, "Low-Frequency Noise in Supported and Suspended MoS_2 Transistors", (Invited Paper) IEEE Transactions on Electron Devices, vol. 65, no. 10, 4135-4140 (2018). (IF:2.92)
45. S. Dev, M. Meena, Harshvardhan, **S. Lodha**, "Statistical Simulation Study of Metal Grain Orientation Induced MS and MIS Contact Resistivity Variability for 7 nm FinFETs", IEEE Transactions on Electron Devices, 65 (8), 3104-3111 (2018). (IF:2.92)
46. Y. Zhang, C. Joishi, Z. Xia, M. Brenner, **S. Lodha**, S. Rajan, "Demonstration of β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ Double Heterostructure Field Effect Transistors", Applied Physics Letters, 112 (23), 233503 (2018). (IF: 3.79, 137 citations)
47. J. McGlone, Z. Xia, Y. Zhang, C. Joishi, **S. Lodha**, S. Rajan, S. Ringel, A. Arehart, "Trapping effects in Si δ-doped β-Ga_2O_3 MESFETs on an Fe-doped β-Ga_2O_3 substrate" IEEE Electron Device Letters, 39 (7), 1042-1045 (2018). (IF: 4.5, 87 citations)
48. N. Goyal, N. Kaushik, H. Jawa, and **S. Lodha**, "Enhanced Stability and Performance of Few-Layer Black Phosphorus Transistors by Electron Beam Irradiation", Nanoscale, vol. 10, issue 24, pp. 11616-11623 (2018). (IF: 7.3, 25 citations)
49. S. Kothari, D. Vaidya, H. Nejad, N. Variam, S. Ganguly, and **S. Lodha**, "Plasma-assisted As Implants For Effective Work Function Modulation of TiN/HfO_2 Gate Stacks on Germanium", Applied Physics Letters, 112 (20), 203503 (2018). **(IF: 3.79)**
50. Z. Xia, C. Joishi, S. Krishnamoorthy, S.Bajaj, Y. Zhang, M. Brenner, **S. Lodha**, S. Rajan. "Delta doped β-Ga_2O_3Field Effect Transistors with Regrown Ohmic Contacts", IEEE Electron Device Letters, vol. 39, issue 4, pp. 568 - 571 (2018). (IF: 4.5, 114 citations)
51. C. Joishi, S. Rafique, Z. Xia, L. Han, S. Krishnamoorthy, Y. Zhang, **S. Lodha**, H. Zhao, S. Rajan, "LPCVD grown β-Ga_2O_3 Bevel Field-plated Schottky Barrier Diodes", Applied Physics Express, vol. 11, no. 3 (2018). (IF:2.89, 109 citations) Featured in "Semiconductor Today"
52. P. Kumar, N. Verma, N. Goyal, J. Biswas, **S. Lodha**, C. Nandi, V. Balakrishnan, "Phase engineering of seamless heterophase homojunctions with co-existing 3R and 2H phases in WS_2 monolayers", Nanoscale, 10, pp. 3320-3330 (2018). (IF: 7.3, 23 citations)
53. K. Deka, A. Guleria, D. Kumar, J. Biswas, **S. Lodha**, S. D. Kaushik, S. Dasgupta, P. Deb, "Mesoporous 3D Carbon Framework Encapsulated Manganese Oxide Nanoparticles as Biocompatible T1 MR Imaging Probe", Colloids and Surfaces A: Physicochemical and Engineering Aspects, Vol. 539, pp. 229–236 (2018). (IF:4.54)
54. A. Tyagi, A. Kottantharayil, K. Ghosh, **S. Lodha**, "Performance Evaluation of Passivated Silicon Carrier Selective Contact Solar Cell", IEEE Transactions on Electron Devices, vol. 65, 1 (2018). (IF:2.92)
55. N. Kaushik, D. Mackenzie, K. Thakar, N. Goyal, B. Mukherjee, P. Boggild, D. H. Petersen, and **S. Lodha**, "Reversible Hysteresis Inversion in MoS_2 Field Effect Transistors", Nature 2D Materials and Applications (2017), 1, 34 (2017). (IF: 11.11, 65 citations)
56. S. Krishnamoorthy, Z. Xia, C. Joishi, Y. Zhang, J. McGlone, J. Johnson, M. Brenner, A. Arehart, J. Hwang, **S. Lodha**, S. Rajan, "Modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ Field-Effect Transistor", Appl. Phys. Lett., 111, 023502 (2017). (IF: 3.79, 248 citations)
57. D. Vaidya, **S. Lodha** and S. Ganguly, "Ab-initio Study of NiGe/Ge Schottky Contact", Journal of Applied Physics, 121, 145701 (2017). (IF: 2.55)
58. D. Biswas, J. Biswas, S. Ghosh, B. Wood, and **S. Lodha**, "Enhanced thermal stability of Ti/TiO_2/n-Ge contacts through plasma nitridation of TiO_2 interfacial layer" Applied Physics Letters, 110, 052104 (2017). (IF: 3.79, 21 citations)
59. B. Mukherjee, N. Kaushik, R. P. N. Tripathi, A. M. Joseph, P. K. Mohapatra, S. Dhar, B. P. Singh, G. V. Pavan Kumar, E. Simsek, and **S. Lodha,** "Exciton Emission Intensity Modulation of Monolayer MoS_2 via Au Plasmon Coupling" Scientific Reports, 7, 41175 (2017). (IF: 4.38, 51 citations)
60. S. Karande, N. Kaushik, D. Narang, D. Late, and **S. Lodha**, "Thickness Tunable Transport in Alloyed WSSe Field Effect Transistors", Applied Physics Letters, 109, 142101 (2016) (IF: 3.79, 28 citations)
61. S. Ghosh, P. Bhatt, Y. Tiwari, C. Joishi, and **S. Lodha**, "Temperature and Field Dependent Low Frequency Noise Characterization of Ge n-FETs", Journal of Applied Physics, 120, 095703 (2016). (IF: 2.55)
62. S. Kothari, C. Joishi, H. Nejad, N. Variam, and **S. Lodha**, "Plasma-assisted low energy N_2 implant for V_{fb} tuning of Ge gate stacks", Applied Physics Letters, 109 (7), 072105 (2016). (IF: 3.79)

63. S. Kothari, C. Joishi, S. Ghosh, D. Biswas, D. Vaidya, S. Ganguly and **S. Lodha**, "Impact of varying Al% in HfAlO high-k on n-channel Ge gate stack performance," Applied Physics Express, 9 (7), 071302 (2016). (IF:2.89)
64. S. Dev, N. Remesh, Y. Rawal, P. P. Manik, B. Wood, and **S. Lodha**, "Low resistivity contact on n-type Ge using low work-function Yb with a thin TiO_2 interfacial layer", Applied Physics Letters, 108 (10), 103507, 2016. (IF: 3.79, 33 citations)
65. A. Nipane, D. Karmakar, S. Karande, N. Kaushik and **S. Lodha**, "Few Layer MoS_2 p-Type Devices Enabled by Selective Doping Using Low Energy Phosphorus Implantation", 10 (2), pp. 2128–2137, ACS Nano, 2016. Best Research Paper Award IIT Bombay 2018 (IF: 15.88, 321 citations)
66. N. Kaushik, D. Karmakar, A. Nipane, S. Karande, and **S. Lodha,** "Interfacial n-Doping using an Ultra-Thin TiO_2 Layer for Contact Resistance Reduction in MoS_2", 8 (1), pp 256–263, ACS Applied Materials and Interfaces, 2016. (IF:9.23, 115 citations)
67. P. Paramahans Manik and **S. Lodha**, "Contacts on n-type Germanium using variably doped ZnO and highly doped ITO interfacial layers", Applied Physics Express 8 (5), 051302, 2015. (IF:3.1, 43 citations)
68. P. Bhatt, P. Swarnkar, A. Misra, J. Biswas, C. Hatem, A. Nainani, and **S. Lodha**, "Enhanced Ge n^+/p Junction Performance Using Cryogenic Phosphorous Implantation", IEEE Transactions on Electron Devices, 62 (1), 69 (2015). (IF:2.92)
69. N. Kaushik, A. Nipane, F. Basheer, S. Dubey, S. Grover, M. Deshmukh, **S. Lodha**, "Schottky Barrier Heights for Au and Pd Contacts to MoS_2", Applied Physics Letters, 105, 113505 (2014). (IF: 3.79, 236 citations)
70. P. Ray, R. Nori, P. Bhatt, **S. Lodha**, R. Pinto, V. R. Rao, F. Jomard, M. Neumann-Spallart, "Optimization of a plasma immersion ion implantation process for shallow junctions in silicon", Journal of Vacuum Science & Technology A 32 (6), 061302 (2014). (IF: 2.43)
71. S. Mukherjee, R. Singh, S. Gopinathan, S. Murugan, S. Gawali, B. Saha, J. Biswas, **S. Lodha**, A. Kumar,"Solution Processed Poly(3,4-ethylenedioxythiophene) thin films as transparent Conductor: Effect of p-Toluenesulphonic Acid in Dimethyl Sulfoxide", ACS Applied Materials & Interfaces, 6 (20), 17792–17803 (2014). (IF:9.23, 61 citations)
72. S. Mittal, S. Gupta, A. Nainani, M.C. Abraham, K. Schuegraf, **S. Lodha**, and U. Ganguly "Epitaxially Defined (ED) FinFET: Variability Resistant and High Performance Technology", IEEE Transactions on Electron Devices, 61 (8), 2711-2718 (2014). **(IF:2.92)**
73. P. Bhatt, P. Swarnkar, F. Basheer, C. Hatem, A. Nainani, **S. Lodha**, "High Performance 400 ºC p^+/n Ge Junctions Using Cryogenic Boron Implantation", IEEE Electron Device Letters, 35 (7), 717-719 (2014). (IF:4.5, 30 citations)
74. P. Bhatt, K. Chaudhuri, S. Kothari, A. Nainani, **S. Lodha**, "Germanium oxynitride gate interlayer dielectric formed on Ge (100) using decoupled plasma nitridation", Applied Physics Letters, 103, 172107 (2013). (IF: 3.79, 44 citations)
75. R. Mandapati, A. Borkar, V. S. S. Srinivasan, P. Bafna, P. Karkare, **S. Lodha**, B. Rajendran, and U. Ganguly, "On Pairing of Bipolar RRAM Memory with NPN Selector based on Set/Reset Array Power Considerations", IEEE Transactions of Nanotechnology, 12 (6), 1178-1184, 2013. (IF:1.82)
76. R. Mandapati, A. Borkar, V. S. S. Srinivasan, P. Bafna, P. Karkare, **S. Lodha**, U. Ganguly, "The Impact of n-p-n Selector-Based Bipolar RRAM Cross-Point on Array Performance", IEEE Transactions on Electron Devices, 60 (10), 3385-3392, 2013. (IF: 2.92, 22 citations)
77. S. Gupta, P. Paramahans, R. K. Mishra, A. Nainani, M. C. Abraham, **S. Lodha**, "Contact Resistivity Reduction through Interfacial Layer Doping in Metal-Interfacial Layer-Semiconductor Contacts," Journal of Applied Physics, 113, 234505 (2013). (IF:2.55, 106 citations)
78. S. Sant, **S. Lodha**, U. Ganguly, S. Mahapatra, S. Ganguly, V. Moroz, L. Smith, and F. Heinz, "Calculations of band gap bowing and band offsets in relaxed and strained $Si_{1-x}Ge_x$ alloys by employing a new nonlinear interpolation scheme," Journal of Applied Physics, 113, 033708 (2013). (IF:2.55, 45 citations)
79. P. Paramahans, R. K. Mishra, V. Pavan Kishore, P. Ray, A. Nainani, Y-C. Huang, M. C. Abraham, U. Ganguly, and **S. Lodha**, "Fermi-level unpinning and low resistivity in contacts to n-type Ge with a thin ZnO interfacial layer", Applied Physics Letters, vol. 101, pp. 182105, 2012. (IF: 3.79, 130 citations)
80. S. Srinivasan, S. Chopra, P. Karkare, P. Bafna, Y. Kim, S. Srinivasan, S. Kuppurao, **S. Lodha**, U. Ganguly, "Punch-through Diode based Bipolar RRAM Selector", IEEE Electron Devices Letters, vol. 33, pp. 1396, 2012. (IF:4.5, 99 citations)
81. P. Kishore, P. Paramahans, S. Sadana, U. Ganguly, **S. Lodha**, "Nanocrystal-based Ohmic contacts on n and p-type germanium", Applied Physics Letters, 100, 142107, 2012. (IF: 3.79, 33 citations)
82. P. Carpenter, **S. Lodha**, A. Walker, D. B. Janes, "Structural and electrical characterization of evaporated contacts in Au/molecule/GaAs devices," Chemical Physics Letters, 472, 4-6, 2009, pp. 220-223. (IF:2.34)
83. S. Ghosh, H. Halimun, A. Mahapatro, J. Choi, **S. Lodha,** D. B. Janes, "Device structure for electronic transport through individual molecules using nanoelectrodes," Applied Physics Letters, 87, 2005, pp. 233509. (IF: 3.79, 67 citations)
84. **S. Lodha,** D. B. Janes, "Metal/Molecule/P-type GaAs Heterostructure Devices," Journal of Applied Physics, 100, 2006, pp. 024503. (IF:2.55, 33 citations)
85. **S. Lodha**, P. Carpenter, D. B. Janes, "Effect of Contact Properties on Current Transport in Metal/Molecule/GaAs Devices," Journal of Applied Physics, 99, 2006, pp. 024510. (IF:2.55, 33 citations)
86. **S. Lodha,** D. B. Janes, "Enhanced current densities in Au/molecule/GaAs devices,"Applied Physics Letters, 85, 2004, pp. 2809. (IF: 3.79, 45 citations)

87. **S. Lodha**, D. B. Janes, N.-P. Chen, "Unpinned interface Fermi level in Schottky contacts to n-GaAs capped with low-temperature-grown GaAs; experiments and modeling using defect state distributions," Journal of Applied Physics, 93, 2003, pp. 2772. (IF:2.55, 29 citations)
88. **S. Lodha**, D. B. Janes, N.-P. Chen, "Fermi level unpinning in ex-situ Schottky contacts on n-GaAs capped with low-temperature-grown GaAs," Applied Physics Letters, 80, 2002, pp. 4452. (IF: 3.79)

Patents Granted (US-2, India-4):

1. P. Paramahans, U. Ganguly, A. Nainani, M. Abraham, **S. Lodha,** "Metal-interfacial semiconductor layer-semiconductor (MISS) contact on a semiconductor substrate and method of fabricating thereof", Indian patent No. 411104, November 9, 2022.
2. S. Mittal, S. Gupta, U. Ganguly, A. Nainani, **S. Lodha**, S. Ganguly, M. Abraham, E.-X. Ping, "Transistor design for improved performance and variability and method of fabrication", Indian Patent No. 358169, February 10, 2021.
3. **S. Lodha and** U. Ganguly, "Low resistance metal-interfacial layer-semiconductor (MIS) contact and method of forming thereof", Indian Patent No. 341586, July 15, 2020.
4. U. Ganguly, **S. Lodha**, P. Bafna, P. Karkare, P. Kumbhare, S. Srinivasan, "Selector device for Bipolar RRAM", Indian Patent Number 323295, 21 October, 2019.
5. R. R. Arnepalli, P. Goradia, R. Visser, N. Ingle, M. Korolik, J. Biswas, **S. Lodha**, "Self-limiting atomic thermal etching systems and methods", US Patent No. 10,043,684, Aug 07, 2018. [79 citations]
6. **S. Lodha**, P. Ranade, C. Auth, "Method of forming CMOS transistors with dual metal silicide formed through the contact openings and structures formed thereby**",** US Patent No. 7,861,406, Jan 04, 2011. [18 citations]

Patents Filed (India-3):

1. S. Ghosh and **S. Lodha**, "Methods and systems for improving photoconductivity in a semiconductor photodiode", Indian patent application number 202321011545, Feb 2023.
2. A. Tyagi, K. Ghosh, A Kottantharayil, **S. Lodha**, "Rear structured solar cells with carrier selective contacts for better efficiency and low cost solution in photovoltaics", Indian patent application no. 201721004570, Feb 2018.
3. D. Biswas and **S. Lodha**, "Method for improving thermal stability of metal-interfacial layer-semiconductor (MIS) contact structures", Indian patent application no. 201821003281, Jan 2018.

Refereed Conference Presentations and Publications (91 Total, International: 87, National: 4)

1. S. Sahoo, A. Varghese, **S. Lodha**, "Ferroelectric induced Multidirectional Polarization in MoS2 for Memory Applications", 81st Device Research Conference, UCSB, June, 2023.
2. Abhay VS, A. Varghese, **S. Lodha**, A. Kumar, "Engineering exciton emission in monolayer TMDCs by dielectric encapsulation", APS Fall Meeting, March, 2023.
3. A. Varghese, A. Pandey, N. Medhekar, U. Ganguly, **S. Lodha**, "Strain Engineering in Transition Metal Dichalcogenide and Piezoelectric Thin Film Based Heterostructures", MRS Fall Meeting, Nov. 30, 2022.
4. K. Thakar, B. Rajendran, S. Lodha, "Biomimetic Spiking Neuron Enabled by Subthreshold Operation of 2D Material-Based Transistor with ~500 Picojoules/Spike", 80th Device Research Conference, June 26-29, Columbius, Ohio, USA.
5. A. Varghese, Y. Yin, **S. Lodha**, N. Medhekar, "Optoelectronics based on Transition Metal Dichalcogenide/2D Perovskite Heterostructures", APS March Meeting, March 18, 2021.
6. S. Nayak, **S. Lodha**, S. Ganguly, "Hybrid gate dielectric with Si3N4 stressor for LDMOSFET", IEEE Latin America Electron Devices Conference (LAEDC), April, 2021.
7. S. Nayak, **S. Lodha,** S. Ganguly, "Fully/partially suspended gate SiC-based FET for power applications", IEEE Latin America Electron Devices Conference (LAEDC), April, 2021.
8. K. Thakar and **S. Lodha**, "Electrostatically Gated Multi-functional WSe_2 Transistor to Enable Multi-bit Communication Schemes", MRS Virtual Spring/Fall Meeting & Exhibit, Nov 28 - Dec 4, 2020.
9. D. Saha and **S. Lodha**, "Study of Transmission Properties of Distorted 1T ReS_2 Based Type-II van der Waals Heterostructures", 2020 MRS Virtual Spring/Fall Meeting & Exhibit, November 28- December 4, 2020.
10. R. Lengare, C. Joishi and **S. Lodha**, "Bilayer dielectrics enabled enhanced RESURF of β-Ga_2O_3 trench Schottky barrier diodes", 5th IEEE ICEE, New Delhi, Nov. 2020.
11. P. Tiwari, J. Biswas, C. Joishi, **S. Lodha**, " Nb_2O_5 high permittivity dielectric enabled electric field engineering of β-Ga_2O_3 Schottky heterojunction diodes", 5th IEEE ICEE, Delhi, Nov. 2020.
12. H. Jawa, S. Ghosh and **S. Lodha**, "Enhanced photo response in MoS_2 transistor using embedded BP", 78th Device Research Conference, June 21-24, 2020.
13. K. Thakar and **S. Lodha**, "Optically-induced Frequency and Phase Modulation in Electrostatically Doped Anti ambipolar WSe_2 Transistors", 78th Device Research Conference, June 21-24, 2020.
14. S. Ghosh, S. Dhara, A. Varghese, K. Thakar, **S. Lodha**, "Tunable WSe_2 phototransistor enabled by electrostatically doped lateral p-n homojunction", 77th Device Research Conference, Ann Arbor, June 23-26, 2019.
15. K. Thakar, **S. Lodha**, "Photo-amplification in Bipolar WSe_2 Transistors with Electrostatic Gating", 77th Device Research Conference, Ann Arbor, June 23-26, 2019.

16. S. Dhara, K. Thakar, S. Ghosh, A. Varghese, S. Mahapatra, **S. Lodha**, "Comparative Evaluation of vdW Materials Based PN Junction and FET for Gas Sensing", 77th Device Research Conference, Ann Arbor, June 23-26, 2019.
17. S. Lodha, K. Thakar, S. Singh, B. Mukherjee, N. Kaushik, S. Grover, B. Muralidharan, M. Deshmukh and **S. Lodha**, "Physics and Modeling of Two-dimensional (2D) RF Transistors and Photodetectors", Invited talk at 3rd IEEE EDTM, Singapore, March 2019.
18. S. Kothari, J. S. Rathore, K. Khiangte, S. Mahapatra and **S. Lodha**, "Interlayer Engineering in GeSn Gate Stacks for Advanced CMOS", 4th IEEE ICEE, Bengaluru, Dec. 2018. Best paper award
19. S. Dev, N. Pradhan, N. Variam, **S. Lodha**, "Impact of N_2 implant on Phosphorus diffusion for shallow n^+/p Ge junctions", 4th IEEE ICEE, Bengaluru, Dec. 2018. Best poster award
20. K. Thakar, A. Varghese, S. Dhara, S. Ghosh and **S. Lodha**, "Low-EOT MoS_2 FET for Efficient Photodetection and Gas Sensing", 4th IEEE ICEE, Bengaluru, Dec. 2018. Best manuscript award
21. B. Mukherjee, S. Roy, E. Simsek, S. Ghosh, V. G. Achanta, **S. Lodha**, "Plasmonic Enhancement in Anisotropic Thin Films of Rhenium Disulphide (ReS_2), 31st Annual Conference of the IEEE Photonics Society, Reston, VA, USA, Sept. 30-Oct 4, (2018).
22. A. Varghese, D. Joseph, S. Ghosh, K. Thakar, N. Medhekar, **S. Lodha**, "WSe_2/ReS_2 vdW Heterostructure for Versatile Optoelectronic Applications", 76th Device Research Conference, Santa Barbara, June 24-27, 2018.
23. N. Goyal, D. M.A. Mackenzie, V. Panchal, H. Jawa, O. Kazakova, D. H. Petersen, **S. Lodha**, "Thermally Aided Nonvolatile Memory Using ReS_2 Transistors", 76th Device Research Conference, Santa Barbara, June 24-27, 2018.
24. H. Jawa, S. Dhara, K. Thakar, S. Ghosh, **S. Lodha**, "Evaluating Performance of Dual-Gate InSe FETs", 76th Device Research Conference, Santa Barbara, June 24-27, 2018.
25. C. Joishi, Z. Xia, J. McGlone, Y. Zhang, A. R. Arehart, S. Ringel, **S. Lodha**, S. Rajan, "Substrate Effects on Transport and Dispersion in Delta-Doped β-Ga_2O_3 Field Effect Transistors", 60th Electronic Materials Conference, Santa Barbara, June 27-29, 2018.
26. Z. Xia, C. Joishi, S. Krishnamoorthy, S. Bajaj, Y. Zhang, M. Brenner, **S. Lodha**, S. Rajan, "Delta-doped β-Ga_2O_3 Field Effect Transistors for Radio Frequency Operation", 60th Electronic Materials Conference, Santa Barbara, June 27-29, 2018.
27. D. M. A. Mackenzie, P. R. Whelan, A. Shivayogimath, N. Kaushik, N. Goyal, J. M. Caridad, J. D. Thomsen, T. J. Booth, L. Gammelgaard, B. S. Jessen, **S. Lodha**, P. Bøggild, D. H. Petersen, "Quality Assessment of 2D Materials: continuity, uniformity and accuracy of mobility measurements", GraphIn2018, Bilbao, Spain, March 13-15, 2018.
28. D. Vaidya, **S. Lodha** and S. Ganguly, "Comparison of Basis Sets for Efficient Ab-initio Modeling of Semiconductors", SISPAD, Japan, 2017.
29. S. Kothari, H. Nejad, N. Variam, **S. Lodha**, "Multi-V_T with metal gate work-function modulation by PLAD implants for Ge FinFET applications", SSDM, Japan, 2017.
30. S. Krishnamoorthy, Z. Xia, C. Joishi, S. Bajaj, Y. Zhang, M. Brenner, **S. Lodha**, S. Rajan, "Towards Modulation-doped β-$(AlGa)_2O_3$/ Ga_2O_3 Field Effect Transistors for High Frequency Electronics", 2nd International Workshop on Gallium Oxide and Related Materials Parma (Italy) – September 12-15, 2017.
31. Z. Xia, S. Krishnamoorthy, C. Joishi, S. Bajaj, Y. Zhang, M. Brenner, **S. Lodha**, S. Rajan, "Delta-doped β-Ga_2O_3 Metal Semiconductor Field Effect Transistors with Regrown Ohmic Contacts", 2nd International Workshop on Gallium Oxide and Related Materials Parma (Italy) – September 12-15, 2017.
32. Z. Xia, S. Krishnamoorthy, C. Joishi, S. Bajaj, Y. Zhang, M. Brenner, **S. Lodha**, S. Rajan "Delta-doped β-Ga_2O_3 Field Effect Transistors with Patterned Regrown Ohmic Contacts," MRS Fall Meeting, Boston, 2017.
33. S. Das, A. Singh, T. Kundu, **S. Lodha**, V. R. Rao, "Off-stoichiometry thiol-ene polymer with tunable localized surface-plasmon resonance for flexible optoelectronic Lab-on Chip device application", International Conference on Smart Materials, Structure & System (ISSS2017), IISc, Bangalore, July 2017.
34. B. Mukherjee, K. Thakar N. Kaushik and **S. Lodha**, "Suspended ReS2 FET for Improved Photocurrent-time Response", Device Research Conference, Notre Dame, USA, 2017.
35. N. Goyal, N. Kaushik, H. Jawa and **S. Lodha**, "Effect of Electron Beam Irradiation on Black Phosphorus Field Effect Transistor Performance", Device Research Conference, Notre Dame, USA, 2017.
36. A. Tyagi, K. Ghosh, A. Kottantharayil, and S. Lodha, "Carrier Selective Back Contact (CSBC) Solar Cell using Transition Metal Oxides", PVSC, Washington, 2017.
37. C. Joishi, S. Kothari, S. Ghosh, S. Mukhopadhyay, S. Mahapatra, and, **S. Lodha** "Ultrafast PBTI characterization on Si-free gate last Ge nFETs with stable and ultrathin Al_2O_3 IL" International Reliability Physics Symposium (IRPS), Monterey, CA, April 2017.
38. P. P. Manik, S. Dev, N. Remesh, Y. Rawal, S. Khopkar, **S. Lodha**, "Ge n-channel FinFET Performance Enhancement Using Low Work Function Metal-Interfacial Layer-Ge Contacts" VLSI-TSA, Hsinchu, Taiwan, April 2017.
39. S. Bhatia, S. Kothari, N. Raorane, **S. Lodha**, P. R. Nair, A. Antony, "Minority Carrier Lifetime Enhancement of C-Si/TiO_2 Heterojunction by Post Deposition Annealing", 32nd European Photovoltaic Solar Energy Conference and Exhibition, Munich, 2016.
40. S. Ghosh, P. Bhatt, Y. Tiwari, **S. Lodha**, "Low Frequency Noise and Mobility Correlation from RT to Low Temperatures for n-Channel Ge MOSFETs", SSDM, Japan, 2015.
41. D. Vaidya, A. Nainani, N. Yoshida, B. Wood, **S. Lodha**, S. Ganguly, "Integrated modeling platform for high-k/alternate channel material heterostructure stacks", SISPAD, September 9-11, Washington DC, USA, 2015.

42. S. Kothari, C. Joishi, D. Vaidya, H. Nejad, B. Colombeau, S. Ganguly, **S. Lodha**, "Metal Gate V_T Modulation Using PLAD N_2 Implants for Ge P-FinFET Applications", ESSDERC, Austria, 2015.
43. Nipane, N. Kaushik, S. Karande, D. Karmakar and **S. Lodha**, "P-type doping of MoS_2 with phosphorus using a plasma immersion ion implantation (PIII) process", Device Research Conference, Ohio, 2015.
44. N. Kaushik, A. Nipane, S. Karande and **S. Lodha**, "Contact resistance reduction in MoS_2 FETs using ultra-thin TiO_2 interfacial layers", Device Research Conference, Ohio, 2015.
45. S. Kothari, C. Joishi, D. Biswas, D. Vaidya, S. Ganguly, **S. Lodha**, "Enhanced Ge n-channel gate stack performance using HfAlO high-k dielectric", Device Research Conference, Ohio, 2015.
46. N. Remesh, S. Dev, Y. Rawal, S. Khopkar, P. P. Manik, B. Wood, A. Brand, **S. Lodha**, "Contact barrier height and resistivity reduction using low work-function metal (Yb)-interfacial layer-semiconductor contacts on n-type Si and Ge", Device Research Conference, Ohio, 2015.
47. S. Dutta, S. Mittal, **S. Lodha**, U. Ganguly, J. Schulze, "A Bulk Planar SiGe Quantum-Well based ZRAM with Low V_T Variability", International Memory Workshop, Monterey, CA, 2015.
48. P. Bhatt, P. Swarnkar, S. Mittal, F. Basheer, C. Thomidis, C. Hatem, B. Colombeau, N. Variam, A. Nainani, and **S. Lodha**, "Cryogenic implantation for source/drain junctions in Ge p-channel (Fin)FETs," Device Research Conference, June 22-26, Santa Barbara, USA, 2014.
49. P. P. Manik, R. K. Mishra, U. Ganguly, **S. Lodha**, "Indium tin oxide (ITO) and Al-doped ZnO (AZO) interfacial layers for Ohmic contacts on n-type Germanium," Device Research Conference, June 22-26, Santa Barbara, USA, 2014.
50. N. Kaushik, A. Nipane, F. Basheer, S. Dubey, S. Grover, M. Deshmukh, **S. Lodha**, "Evaluating Au and Pd contacts in mono and multilayer MoS2 transistors," Device Research Conference, June 22-26, Santa Barbara, USA, 2014.
51. S. Mittal, S. Kurude, S. Dutta, P. Debashis, S. Ganguly, **S. Lodha**, A. Laha, U. Ganguly, "Epitaxial Rare Earth Oxide (EOx) FinFET: a variability-resistant Ge FinFET architecture with multi VT," DRC, June 22-26, Santa Barbara, USA, 2014.
52. Yaksh Rawal, Debashree Burman*, Prashanth P. Manik, Piyush Bhatt, Anoop C., **Saurabh Lodha**, Swaroop Ganguly, Maryam Shojaei Baghini, "Performance Comparison of MIM and MIS Diodes for Energy Harvesting Applications," IEEE Intl. Conference of Electron Devices and Solid-State Circuits, Chengdu, June 18-20, 2014.
53. R. Meshram, B. Das, R. Mandapati, S. Lashkare, S. Deshmukh, J. Schulze, **S. Lodha**, U. Ganguly, "High Performance Triangular Barrier Engineered NIPIN Selector for Bipolar RRAM", International Memory Workshop, Taiwan, 2014.
54. P. Bhatt, P. Swarnkar, A. Misra, C. Hatem, A. Nainani and **S. Lodha**, "Cryo Implanted High Performance n+/p Junctions in Ge for future CMOS", IEEE VLSI TSA, Hsinchu, Taiwan, April 2014. Shortlisted for best paper award
55. P. Debashis, S. Mittal, **S. Lodha** and U. Ganguly "Dopant Deactivation: A new challenge in sub-20nm Scaled FinFETs", IEEE VLSI TSA, Hsinchu, Taiwan, April 2014.
56. P. Bhatt, P. Swarnkar, A. Misra, J. Biswas, C. Hatem, A. Nainani, **S. Lodha**, "Ge n^+/p junctions using temperature-based phosphorous implantation," 7th International SiGe Technology and Device Meeting (ISTDM 2014), 2 – 4 June 2014, Singapore.
57. D. Vaidya, S. Sant, A. Hegde, **S. Lodha**, U. Ganguly, S. Ganguly, "Modeling Charge Control in Heterostructure Nanoscale Transistors", Invited talk at IWPSD, New Delhi, December 2013.
58. S. Mittal, P. Debashis, A. Nainani, M. C. Abraham, **S. Lodha** and U. Ganguly " Epi Defined (ED) FinFET with Dynamic Threshold: Reduced VT Variability, Enhanced Performance, and a novel Multiple V_T", IEEE INDICON, Mumbai, December 2013**.** Best Paper Award
59. R. K. Mishra, P. P. Manik, A. Nainani, **S. Lodha**, "Contacts to N-Type Si/Ge/Si:C Using Rare Earth Metals", MRS Fall Meeting, Boston, Dec, 2013.
60. H. Mehta, **S. Lodha**, U. Ganguly, S. Ganguly, "Calibration of the Density-Gradient TCAD Model for Germanium FinFETs", IEEE Regional Symposium on Micro and Nanoelectronics, Malaysia, Sept, 2013.
61. R. K. Mishra, U. Ganguly, S. Ganguly, **S. Lodha**, A. Nainani, M. Abraham, "Nickel germanide with rare earth interlayers for Ge CMOS applications", IEEE Intl. Conf. on Electron Devices and Solid-State Circuits, Hong Kong, June, 2013.
62. S. Lashkare, P. Karkare, P. Bafna, M.V.S. Raju, V.S.S. Srinivasan, J. Schulze, S. Chopra, **S. Lodha**, U. Ganguly, "A Bipolar RRAM Selector with Designable Polarity Dependent On-Voltage Asymmetry", International Memory Workshop, California, Jun, 2013.
63. P. Bhatt, K. Chaudhuri, R.Banerjee, A. Nainani, M. Abraham, M. Subramaniam, U. Ganguly, **S. Lodha**, "Improved Nitridation of GeO_2 Interfacial layer for Ge Gate Stack Technology", vol. 1561, MRS Online Proc. Library, 2013.
64. S. Mittal, S. Gupta, A. Nainani, M. Abhraham, K. Schuegraf, **S. Lodha**, and U. Ganguly, " Epi Defined (ED) FinFET: An alternate device architecture for high mobility Ge channel integration in PMOSFET", 5th IEEE International Nanoelectronics Conference (INEC), Jan. 2-4, 367 (2013).
65. R. Mandapati, A. Borkar, S. Srinivasan, P. Bafna, P. Karkare, **S. Lodha**, and U.Ganguly, "On Pairing Bipolar RRAM memory element with novel punchthrough diode based selector: Compact modeling to array performance", 5th IEEE International Nanoelectronics Conference (INEC), Jan. 2-4, 309 (2013).
66. K. Chaudhuri, P. Bhatt, A. Nainani, M. Abraham, M Subramaniam, S. Kapadia, K. Schuegraf, U. Ganguly, **S. Lodha**, "Comparison of plasma and thermal nitridation of GeO_2 interfacial layer for Ge CMOS", 43rd IEEE Semiconductor Interface Specialists Conference, San Diego, CA, December 6-8, 2012.
67. S. Sant, **S. Lodha**, U. Ganguly, S. Ganguly, "Novel nonlinear interpolation for Si1−xGex bandstructure parameters", IEEE International Conference of Electron Devices and Solid-State Circuits, Bangkok, Dec, 2012.

68. S. Deshmukh, R. Mandapati, S. Lashkare, A. Borkar, V. S. S. Srinivasan, **S. Lodha**, U. Ganguly, "Comparison of novel punch-through diode (NPN) selector with MIM selector for Bipolar RRAM", 2012 12th Non-Volatile Memory Technology Symposium (NVMTS 2012) Oct 31st –Nov 2nd, 2012, Singapore.
69. S. Chopra, P. Bafna, P. Karkare, S. Srinivasan, S. Lashkare, P. Kumbhare, Y. Kim, S. Srinivasan, S. Kuppurao, **S. Lodha**, and U. Ganguly, "A Two Terminal Vertical Selector Device for Bipolar RRAM", Pacific Rim Meeting on Electrochemical and Solid State Science (PRiME), Honolulu, Hawaii, USA, October 7-12 2012.
70. S. Mittal, S. Gupta, A. Nainani, M.C. Abraham, K. Schuegraf, **S. Lodha**, U. Ganguly, "Epitaxialy defined (ED) FinFET: to reduce V_T variability and enable multiple V_T" Device Research Conference, USA, June 20-22, 2012.
71. P. Bafna, P. Karkare, S. Srinivasan, S. Chopra, S. Lashkare, Y. Kim, S. Srinivasan, S. Kuppurao**, S. Lodha**, U. Ganguly, "Epitaxial Si Punch-Through based Selector for Bipolar RRAM", Device Research Conference, USA June 20-22, 2012.
72. P. Paramahans, S. Gupta, R. K. Mishra, N. Agarwal, A. Nainani, Y. Huang, M.C. Abraham, S. Kapadia, U. Ganguly, **S. Lodha**, "ZnO: an attractive option for n-type metal-interfacial layer-semiconductor (Si, Ge, SiC) contacts", VLSI Symposium in Technology, USA, June 12-15, 2012.
73. V. Pavan Kishore, P. Paramahans, S. Sadana, U. Ganguly, **S. Lodha**, "Contact Resistance Reduction on Germanium through Metal Work Function Engineering", MRS Spring Meeting, USA, April 9-13, 2012.
74. P. Paramahans, P. Ray, S. Mane, P. Nyaupane, U. Ganguly, **S. Lodha**, "Ohmic contacts to n-type Germanium using a thin ZnO interfacial layer", MRS Spring Meeting, USA, April 9-13, 2012.
75. V. Pavan Kishore, P. Paramahans, S. Sadana, U. Ganguly, **S. Lodha**, "Novel Nanocrystal-based Contacts on n and p-type Germanium", 39th Conf. on Physics and Chemistry of Surfaces & Interfaces (PCSI-39), USA, Jan. 22 – 26, 2012.
76. P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani,O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S.-H. Lee, M. Liu, **S. Lodha**, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, k. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo, S. Natarajan, "High performance 32nm logic technology featuring 2nd generation high-k + metal gate transistors", International Electron Devices Meeting, USA, Dec. 7-9 2009. (278 citations)
77. S. Natarajan, M. Armstrong; M. Bost., R. Brain, M. Brazier, C.-H. Chang, V. Chikarmane, M. Childs, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner,R. James, I. Jin, C. Kenyon, S. Klopcic, S.-H. Lee, M. Liu, **S. Lodha**, B. McFadden, A. Murthy, L. Neiberg, J. Neirynck, P. Packan, S. Pae, C. Parker, C. Pelto, L. Pipes, J. Sebastian, J. Seiple, B. Sell, S. Sivakumar, B. Song, K. Tone, T. Troeger, C. Weber, M. Yang, A. Yeoh, K. Zhang, "A 32nm logic technology featuring 2nd-generation high-k + metal-gate transistors, enhanced channel strain and 0.171 μm2 SRAM cell size in a 291Mb array", International Electron Devices Meeting, USA, Dec. 15-17 2008. (279 citations)
78. P. Carpenter, A. Scott, **S. Lodha**, D. Janes, C. Risko, M. Ratner, "Substrate and Dipole Effects in Metal-Molecule-Semiconductor Heterostructures", Proceedings of the 6thIEEE conference on Nanotechnology, USA, July 17-20 2006, vol. 1, pp. 104-107.
79. **S. Lodha,** D. B. Janes, "Fabrication and electrical characterization of Au/molecule/GaAs devices," Proceedings of the 4th IEEE conference on Nanotechnology, Germany, Aug. 16-19 2004, pp. 278-80.
80. D. B. Janes, S. Ghosh, **S. Lodha**, J. Choi, S. Bhattacharya, "Metal-Molecule-Metal and Metal-Molecule-Semiconductor Devices," IEEE Nanoscale Devices and Systems Integration Conference, USA, Feb. 16-19, 2004.
81. **S. Lodha,** D. B. Janes, "Metal-molecule-semiconductor heterostructures for nanoelectronic applications," Proceedings of the International Semiconductor Device Research Symposium, USA, Dec. 10-12 2003, pp. 446-7.
82. J. Choi, D. Janes, H. Halimun, **S. Lodha**, "Metal-Molecule-Metal Structures with Pre-Fabricated Contacts," Proceedings of the 4th International Conference on Intelligent Processing and Manufacturing of Materials, Japan, May 18-23 2003.
83. **S. Lodha**, J. Choi, S. Bhattacharya, D. B. Janes, "Metal-molecule-semiconductor heterostructures for nano-device applications," Proceedings of the 3rd IEEE conference on Nanotechnology, USA, Aug. 12-14, 2003, pp. 311-314.
84. S. Bhattacharya, J. Choi, **S. Lodha**, D. B. Janes, A. Bonilla, K. Jeong, G. Lee, "Electronic Conduction in DNA attached to Gold Electrodes," Proceedings of the 3rd IEEE conference on Nanotechnology, USA, Aug. 12-14 2003, pp. 79-82.
85. J. Choi, D. B. Janes, **S. Lodha**, Y. Chen, R. Agarwal, R. P. Andres, S. Burns, C. P. Kubiak, "Conduction through molecule-gold cluster complexes and applications," Proceedings of the 3rd IEEE conference on Nanotechnology, USA, Aug. 12-14, 2003, pp. 164-167.
86. D. B. Janes, S. Ghosh, J. Choi, **S. Lodha,** S. Bhattacharya, "Circuit characteristics of molecular electronic components," Proceedings of IEEE international conference on Application-Specific Systems, Architectures, and Processors, Netherlands, June 24-26 2003, pp. 120-126.
87. S. Bhattacharya, D. B. Janes, G. Lee, J. Choi, **S. Lodha**, A. Bonilla, "Measuring Electronic Conduction in DNA Attached to Au-Electrodes," 45th Electronics Materials Conference, Salt Lake City, USA, June 25-27, 2003.
88. J. Choi, D. B. Janes, **S. Lodha**, Y. Chen, H. Halimun, S. Ghosh, S. Burns, C. P. Kubiak, "Metal-Molecules-Metal Devices with Preformed Metal Contact Structures," 45th Electronics Materials Conference, Salt Lake City, USA, June 25-27, 2003.
89. **S. Lodha**, N-P. Chen, D. B. Janes, "Interface Fermi Level Unpinning in Schottky Contacts on N-Type Gallium Arsenide with a Thin Low-Temperature-Grown Cap Layer," 44th Electronics Materials Conference, Santa Barbara, USA, June 26-28, 2002.

90. **S. Lodha**, D. B. Janes, S. Howell, M. V. Batistuta, E. H. Chen, R. Reifenberger, "Experimental and Modeling Studies of Schottky Contacts to Low-Temperature-Grown GaAs in Ex-Situ Structures," 43rd Electronics Materials Conference, Notre Dame, USA, June 27-29, 2001.
91. A. Topkar, **S. Lodha,** J. Vasi, "Ionizing radiation induced degradation of SiGe HBTs," Proceedings of the 10th Intl. Workshop on Physics of Semiconductor Devices, India, Dec. 1999, pp. 659-662.

Visiting Faculty Positions

1. Visiting Professor, Department of Precision and Micro Systems Engineering, Delft University of Technology (TU Delft), Oct 2020 – Aug 2021
2. Visiting Professor, Department of Applied Physics, Eindhoven University of Technology (TU Eindhoven), Oct 2020 – Aug 2021
3. Guest Professor, Department of Micro and Nanotechnology, Technical University of Denmark, June 1-20, 2016

Invited Talks

1. Invited talk at 2D TMDs 2023, University of Cambridge, UK, June 2023.
2. "Transition Metal Dichalcogenide Device Engineering using Piezoelectric Thin Films" Invited talk at 1st Indo-Swedish meeting on "Divergent Quantum Materials, Methods and Applications-2023" (DQMMA 2023), Goa, Feb 2-4, 2023.
3. "Few-layer 2D semiconductors and their heterostructures for enhanced photodetection performance", Keynote talk at Platinum Jubilee Conference, PMR 2022, June 22, IISc, Bengaluru, 2022.
4. "Few-layer 2D semiconductors and their heterostructures for enhanced photodetection performance", Invited lecture at "75th anniversary of transistors" workshop, IEEE EDS, IIT Kanpur, October 11, 2022.
5. Invite talk at workshop on "Two-dimensional materials-based devices and their applications", IIT Gandhinagar, Dec 3-4, 2022.
6. Invited talk at 4th International Conference on Emerging Advanced Nanomaterials (ICEAN 2021), October 17-21, Newcastle, Australia, 2022.
7. Invited EDS Webinar on "Photodetectors based on few-layer 2D semiconductors and their heterostructures", June 29th, 2022.
8. "Photodetectors based on few-layer 2D semiconductors and their heterostructures", IEEE Workshop on Devices and Circuits, Goa, India, March, 2022.
9. "Enhanced photodetection and multi-bit encoding with WSe_2 (photo)transistors using novel electrostatic gating techniques", IWPSD, IIT Delhi, Dec., 2021.
10. "Thin Film XPS and UPS Studies for Semiconductor Device Applications", at PHI European/EMEA Workshop, March 02, 2021.
11. "Few-layer TMDs and their heterostructures for high performance photodetection", ICEE 2020, Delhi, November 26, 2020.
12. "Perspectives on Indo-Dutch Scientific Collaboration", TU Delft, Netherlands, Nov. 05, 2020.
13. "Few-layer TMDs and their heterostructures for high performance photodetection", ICONSAT, Kolkata, Mar 06, 2020.
14. "Insights into photoresponsivity and speed trade-off in TMDC photodetectors", XXth IWPSD, Kolkata, Dec. 2019.
15. "Photodetection using few-layer TMDs and their heterostructures", Flatlands and beyond-2DM, S. N. Bose National Centre for Basic Sciences, Kolkata, Sept. 6, 2019.
16. "Engineering photodetection in 2D layered semiconductors and their heterostructures" 2nd Conference on Quantum Condensed Matter (Q-Mar2019), IISc Bangalore, July 10, 2019.
17. "Gate stack and doping implants in Germanium and 2D MoS_2" Applied Materials Implant Technology Division, Gloucester, Boston (MA), June 27, 2019.
18. "Physics and Modeling of Two-dimensional (2D) RF Transistors and Photodetectors", 3rd IEEE EDTM, Singapore, March 12-15, 2019.
19. "Photodetection using 2D layered semiconductors and their heterostructures", Invited talk at 30th Annual General Meeting of the Materials Research Society of India, IISc Bangalore, Feb 14, 2019.
20. "Optoelectronic devices using 2D van der Waals materials", 4th IEEE ICEE, Bengaluru, Dec 2018.
21. "Emerging Electronic and Optoelectronic Materials and Devices", Keynote talk at 10th Bangalore Nano, Dec 2018.
22. "Optoelectronic devices using 2D van der Waals materials", 5th ISSMD, VNIT, Nagpur, Dec 2018.
23. "2D Materials for Optoelectronic Applications", Oxford Instruments "Bringing The Nanoworld Together" Workshop, Mumbai, Nov 2018.
24. "Electronic and optoelectronic devices using 2D van der Waals materials", National Taiwan University, Taipei, Sep 2018.
25. "Electronic and optoelectronic devices using 2D van der Waals materials", University of Iceland, Reykjavik, Aug 2018.
26. "Isolation in FinFETs", Applied Materials, Boston, June 21, 2018.

27. "Electronic and optoelectronic devices using 2D van der Waals materials", IIT Mandi, May, 2018.
28. "Engineering Ge and 2D MoS_2 transistors for advanced CMOS", IEEE CONECCT, Bangalore, March, 2018.
29. "Gate stack and source-drain contact engineering in Ge and 2D MoS_2 devices", NCTU, April 24, Hsinchu, Taiwan, 2017.
30. "Gate stack and source-drain contact engineering in Ge and 2D MoS_2 devices", NTHU, April 27, Hsinchu, Taiwan, 2017.
31. "Contact resistance, doping and carrier transport in emerging MoS_2 devices", Monash University, March 13, 2017.
32. "Contacts, junctions and gate stacks in emerging CMOS materials", IIT Kanpur, March, 2017.
33. "Gate stack engineering in Germanium channel FETs for advanced CMOS applications", IUMRS-ICYRAM, IISc Bangalore, December 15, 2016.
34. "Contact Resistance and Doping in Few-Layer MoS_2 Transistors", Tech. Univ. of Denmark, June 7, 2016.
35. "Metal-semiconductor contacts", School on Nanoscale Electronic Transport and Magnetism: Fundamentals to Applications, HRI Allahabad, Mar, 2016.
36. "Ge and 2D MoS_2 devices for sub-10 nm transistor technologies", IWPSD, IISc, Dec, 2015.
37. "Source-drain and gate stack engineering in Ge and 2D MoS_2 devices", Applied Materials Implant Technology Division, Gloucester, Boston (MA), June, 2015.
38. "Novel materials and devices for future low power electronics", 5th MRS Trilateral Conference on Advances in Nanomaterials: Energy, Water & Healthcare, Shenyang, China, Sep, 2014.
39. "Gate Stack and Source/Drain Engineering in Ge and MoS_2", Applied Materials Implant Technology Division, Gloucester, Boston (MA), June, 2014
40. "Materials, Processes and Devices for beyond 22nm CMOS", 6th Bangalore India Nano-Exhibition & Conference, Bengaluru, Dec, 2013
41. "Beyond 22nm CMOS Logic Roadmap", Applied Materials, Santa Clara, USA, Aug, 2013.
42. D. Vaidya, S. Sant, A. Hegde, S. Lodha, U. Ganguly, S. Ganguly, "Modeling Charge Control in Heterostructure Nanoscale Transistors", IWPSD, New Delhi, December 2013.
43. "Gate stack and source/drain engineering for enabling Ge CMOS", IEEE International Conference on Emerging Electronics (ICEE), IIT Bombay, December 16, 2012.
44. "Germanium CMOS for next generation logic technology", Applied Materials, Santa Clara, USA, April 12, 2012.
45. "Fabrication and Characterization of Ge devices", Summer School "nanoMASTD-12" on Frontiers of Nano Materials, Structures and Devices, Department of Radio Physics and Electronics, Calcutta University, July 2nd, 2012.

Professional Activities

1. Member, AICTE Committee on "Capacity Building in Semiconductor Domain under Semicon India Program", May 2022-Dec 2022.
2. Member, DST-SERB Committee on Fund for Industrial Research Engagement (SERB-FIRE), Nov. 2021-present.
3. Member, Department Advisory Committee, Department of Physics, IIT Jammu, 2021-present
4. Member, Standing Consultative Committee of Young Scientists, DST, Govt. of India, 2018-2023
5. Steering Committee Member 5th IEEE ICEE Nov 26-28 IIT Delhi 2020, TPC Member 4th IEEE ICEE Bengaluru December 16-19 2018, General Chair 3rd IEEE ICEE Dec 27-30 IIT Bombay 2016, Technical Program Co-Chair 2nd IEEE Intl. Conference on Emerging Electronics Dec 3-6 2014
6. TPC Member, 76th (UCSB, Jun24-27, 2018), 77th (U. Mich. Ann Arbor, June 23-26, 2019) and 78th (Ohio State Univ., June, 2020) Device Research Conferences
7. TPC Member, International Symposium on VLSI Technology, Systems and Applications, Hsinchu, Taiwan, April 19-22 2021, Aug 10-13 2020, April 22-25 2019, April 16-19 2018, April 24-27 2017
8. TPC Member, XXth IWPSD, S. N. Bose Centre for Basic Sciences, Kolkata, Dec. 17-20, 2019
9. Chair, Indo-US workshop on Frontiers of Wide and Ultra-wide Bandgap Power Devices and Electronics, Dec. 14-15, 2019
10. TPC Member, 3rd IEEE EDTM Conference, Singapore, March 12-15, 2019
11. Technical sub-committee chair of Symposium on SiGe, IUMRS-ICYRAM 2016, IISc, Bengaluru, India, Dec 11-15, 2016
12. Technical sub-committee chair of Symposium on Nanotechnology, International Workshop on Physics of Semiconductor Devices, IISc, Bengaluru, India, Dec 7-10, 2015
13. Organizing Chair, 27th International Conference on VLSI Design, Mumbai, Jan 5-9, 2014
14. Co-ordinator for India's first hands-on course on "Semiconductor Technology and Manufacturing" offered through CEP, IIT Bombay for Indian industry and academia, 2012, 2013, 2014
15. Member, Technical Program Committee, 17th and 19th International Symposium on VLSI Design and Test (VDAT), Jaipur, July 27-30, 2013 and Ahmedabad, June 26-29, 2015
16. Invited Member, 4th Review Meeting of Electronic and Telecom Sector Skill Councils, MeitY, Govt. of India, April 2013

17. Reviewer for Advanced Materials, ACS Nano, Nano Letters, Nature Communications, Nature 2D Materials and Applications, Nature Scientific Reports, ACS Applied Materials and Interfaces, Nature Asia Materials, Applied Physics Letters, IEEE Transactions on Electron Devices, Circuits and Systems, Nanotechnology and Electron Device Letters
18. External Examiner (PhD Thesis), TIFR, IIT-KGP, IIT-K, IISc Bangalore, IIT-D, IIT Roorkee, IIT Hyderabad, BITS Pilani

Administrative positions

1. Co-Professor-in-charge, IIT Bombay Research Park, Apr 2015 – Jul 2021
2. Co-convener of Institute Nano Facility Committee, 2016-present
3. Chairman (Technical) at IIT Bombay, 2016-2018
4. Member, Institute Charging Committee, 2017-present
5. Member, Institute of Eminence Committee, 2017-present
6. Member of EE department policy, post-graduate and admissions committees

Outreach talks

1. "2D MoS_2 Devices for Logic Applications", NIT Silchar, January 28, 2019
2. "2D MoS_2 Devices for Logic Applications", KIIT, Bhubaneshwar, April 28, 2018
3. "Device Fabrication for advanced CMOS technologies", IIST Trivandrum, April 16, 2016
4. "2D MoS_2 devices for logic applications", NIT Agartala, Feb 16, 2016
5. "Germanium CMOS for beyond 22 nm logic applications", PSGIAS Coimbatore, October 24, 2013
6. "Germanium CMOS for beyond 22 nm logic applications", IIT Guwahati, September 29, 2012
7. "Germanium CMOS for beyond 22 nm logic applications", NIT Calicut, February 17, 2012
8. "Future of CMOS technology: challenges and opportunities", Department of Electronic Science, Calcutta University, September 17, 2010

Research Guidance

- Post-doctoral fellows: 7 (past), 2 (current)
- PhDs: 16 graduated (11 as supervisor), 7 ongoing
- Masters' students: 30 graduated, 2 ongoing

Courses Taught and Developed

- Undergraduate: Introduction to Electrical and Electronic Circuits, Digital Systems, Introduction to Microelectronics, Electronic Devices and Circuits, Digital Systems Lab, Electronic Design Lab, Electronic Devices Lab
- Postgraduate: Solid State Devices, 2D Materials and Devices, Microelectronics Fabrication Lab, Microelectronics Simulation Lab