NANOCHIP

Technology Journal

ENHANCING Ge nMOSFET PERFORMANCE WITH GeON GATE DIELECTRIC

IN THIS ISSUE

- Integrating Ge Channel Materials in pMOSFET With Epi-Defined FinFET
- Tuning Threshold Voltage for 10nm CMOS Integration
- Dry Removal Technology for Advanced CMOS Devices

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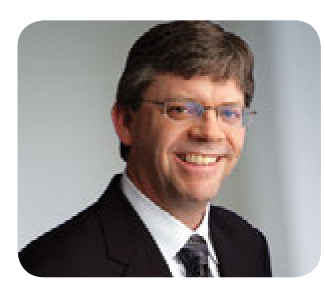
A MESSAGE FROM GARY MINER



Gary Miner
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Necessity is the mother of invention. This proverb is particularly apt in the context of evolving semiconductor technology. Each successive node has posed new challenges, raised the performance bar, and inspired ingenious solutions. This Nanochip highlights creative solutions to issues demanding considerable ingenuity to resolve as we prepare for sub-2xnm nodes.

Shrinking transistor dimensions are intensifying the focus on channel mobility. Germanium is attracting much interest as silicon's successor, but crucial properties exclude GeO_2 from serious consideration. In contrast, we find that GeON produced by plasma nitridation is more stable and exhibits peak electron mobility twice that of GeON formed through RTP. Pulsed plasma improves mobility even more while preserving nitrogen concentration. These findings confirm the feasibility of incorporating high-mobility GeON into Ge nMOSFETs, complementing Ge PMOS to enable true Ge CMOS technology.

Integrating high-mobility channel materials in FinFETs is a challenge as their narrow band gap leads to high band-to-band tunneling leakage. Fin width also affects band-to-band leakage; eliminating line edge roughness (LER) is essential. A new approach minimizes LER by defining channel depletion through an epitaxy-defined FinFET rather than by lithography. This method achieves additional structural and electrical benefits unmatched by conventional FinFETs.

Large-scale integrations at the 10nm node and beyond will require high performance, low operating power, and low standby power technologies on the same die. This will necessitate achieving multiple threshold voltages. We present studies of binary metal composition and nitrogen implant effects on effective work function that leads to threshold voltage tuning capability over a 600mV range.

Shrinking geometries are also challenging us to find alternatives to processes standard for larger nodes. We present a dry removal alternative to wet cleaning and etch processes that avoids pattern deformation and can be tuned to prevent pattern loading. Highly selective and insensitive to differences in oxide density, it is well suited for the soft dielectrics in advanced devices.

Hardware is also improving. We review the evolution in chamber materials accompanying the change in feature scale and process chemistries, and highlight a new plasma coating material that demonstrates benchmark low defectivity in a wide range of environments.

Future-generation designs could employ silicon nanowire devices, such as gate-all-around CMOS architecture that demonstrates superior gate control and immunity to short-channel effects. Thin suspended SiNWs pose a significant challenge for CDSEM metrology, prompting development of a height map reconstruction technique detailed in this issue.

I trust you will find the topics here of interest. They demonstrate our focus on solving our customers' high value problems and also our efforts to develop new capabilities in anticipation of challenges that future nodes will pose.

Cover: Lower nitrogen concentration and an ultra-smooth interface with Ge help improve carrier mobility and maintain thermal stability of GeON, making it an effective interlayer dielectric for future Ge CMOS gate stacks.

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Enhancing Ge nMOSFET Performance

With GeON Gate Dielectric

KEYWORDS

Continuous Wave
Decoupled Plasma Nitridation
Gate Interdielectric
GeON
Germanium
MOSFET
Pulsed Wave

MOSFETs are experiencing numerous changes in materials and fabrication in response to demands of mobile technologies. Ge has attracted particular interest as a channel material, owing to its high bulk hole and electron mobilities, but GeO_2 exhibits poor thermal and chemical stability. A novel GeON process creates a more viable gate interlayer dielectric. This plasma-nitrided material shows enhanced thermal stability and scalability with peak electron mobility of 818cm^2/V.s—twice the highest reported value for Ge nMOSFETs using thermally nitrided GeON. Pulsing the plasma yields a further 1.2X improvement while preserving overall nitrogen concentration.

Since the first experimental demonstration in 1960, the Si-based MOSFET has become the driving force of the semiconductor industry. Although the architecture and working principle of the MOSFET have remained the same, the physical dimensions have been steadily decreasing to double the number of transistors on a chip every two years, consistent with Moore's Law. However, conventional device dimension scaling cannot continue indefinitely. Since scaling reached the sub-100nm regime, more non-Si elements have been incorporated into Si technology at every generation. At the 90nm node, the SiGe source/drain (S/D) was introduced to achieve uniaxial strain in the channel; the high-κ metal gate followed at the 45nm node, marking the biggest change in transistor technology to that point.

While half of the periodic table elements are present in today's advanced ICs, silicon has remained the MOSFET channel material—until now. Several candidate replacements are being considered, as shown in Table 1, which compares the key metrics for these materials. Ge has substantially higher bulk electron and hole mobilities, approximately two and four times higher, respectively, than those of Si. Based on mobility numbers alone, the best combination would seem to be Ge for PMOS and III-V for NMOS. However, realizing a nanoscale III-V transistor on a Si platform poses many process, integration, and cost issues, some of which may not be easily resolved. On the other hand, Ge offers the advantages of process compatibility and easy integration with Si technology. Integrating Ge as the channel material in advanced CMOS technology would be straightforward, considering SiGe's earlier integration into the S/D regions of current MOSFETs.

Besides its higher hole and electron mobilities than Si, Ge is emerging as the candidate of greatest interest based on advances in high-κ dielectric-based gate stacks and epitaxial growth of high quality silicon germanium/germanium (SiGe/Ge) quantum well layers.[1] However, while gate stacks employing a GeO_2 interlayer (IL) dielectric have been shown to achieve low interface trap density (D_{it}) and carrier mobilities higher than those of Si,[2] the GeO_2 dielectric constant (~5.5-5.9), and poor thermal and chemical stability make it non-ideal for effective oxide thickness (EOT) scaling and CMOS process integration.[3,4] Nitridation of GeO_2 (GeON) has therefore been proposed to enhance thermal and chemical stability, increase the dielectric constant, and improve resistance to impurity diffusion through the gate dielectric.[5] Several research groups have already successfully demonstrated high-mobility Ge PMOS, but higher D_{it} near the conduction band edge vs. the valence band edge (E_V) have made high-mobility Ge nMOSFETs more challenging to achieve.[6] This is especially true for GeON, for which the highest reported nFET mobility is 400cm^2/V.s,[7] much lower than the 1020cm^2/V.s for Ge(100) using a GeO_2 IL.[2] Hence, incorporating high-mobility GeON into a Ge nMOSFET can help enable true Ge CMOS technology.

In this work, we correlate chemical (such as nitrogen concentration) and physical (such as IL/Ge interface roughness) properties of three different in-situ ILs for Ge gate stacks with electrical performance metrics, such as the carrier mobility and D_{it} measured on the same n-channel Ge transistors. Three experimental stacks were studied, namely (a) GeO_2, (b) GeO_2 nitrided using RTP, and (c) GeO_2 nitrided by decoupled plasma nitridation (DPN). Angle Resolved X-ray Photoemission Spectroscopy (AR-XPS) studies were conducted to estimate the nitrogen profile in the ILs and transmission electron microscopy (TEM) studies investigated the thickness and nature of the IL/Ge interface. Results from both correlate well with mobility and D_{it} values for the different ILs. The DPN process resulted in lower nitrogen concentration and less roughness at the GeON/Ge interface compared to the RTP process. These two attributes help improve carrier mobility and lower D_{it} without degrading thermal stability.

DEVICE FABRICATION

Gallium-doped p-type Ge(100) 1-10ohm-cm wafers were used to fabricate MOS capacitors (MOSCAPs) and MOSFETs. For MOSCAPs, an organic clean was followed by cyclic hydrofluoric acid:deionized water (HF:DI) dips to remove impurities and native oxides.[7] After a hydrochloric acid treatment for surface passivation, the samples were immediately loaded into a gate stack cluster tool for in-situ IL growth. GeO_2 was grown by RTP at 400°C followed by ammonia RTP nitridation at 600°C (RTP GeON) or by room temperature DPN nitridation at 20mTorr followed by a post-nitridation anneal (PNA) at 500°C in low-pressure O_2 ambient to anneal out plasma damage (DPN+PNA GeON).

DPN employs an inductively coupled RF magnetic field parallel to the wafer to generate plasma with a high ion density but low ion energy. This results in higher N_2 incorporation at the surface of the dielectric and less risk of ion damage.[8] The three ILs were capped with SiO_2 (10nm) using low-temperature (400°C) CVD. SiO_2 was used as a capping layer instead of high-κ alternatives to avoid high-κ related effects on the extraction of D_{it} and carrier mobility.[9] Finally, aluminum gate metal was deposited and patterned followed by a forming gas anneal at 350°C for 30 minutes.

A gate-last process was used in fabricating the nMOSFET (Figure 1a). After a chemical clean and active area definition using SiO_2, a 400nm SiO_2 dummy gate was deposited using plasma enhanced CVD (PECVD) and lithographically patterned. This was followed by S/D junction formation by spin coating of phosphorus spin-on-dopant (SOD), an activation RTP anneal at 650°C and removal of residual SOD and dummy gate in 5% HF. The actual gate stack was then formed using the same process as for MOSCAP fabrication. Finally, nickel S/D contacts were defined using lithography and liftoff, and backside bulk contact was formed by evaporating aluminum.

Table 1

Property	Material				
	Si	Ge	GaAs	InAs	InSb
Electron Mobility	1600	3900	9200	40000	77000
Hole Mobility	430	1900	400	500	850
Bandgap (eV)	1.12	0.66	1.424	0.36	0.17
Dielectric Constant	11.8	16	12.4	14.8	17.7

Table 1. Comparison of key metrics for advanced semiconductor materials.

Figure 1

- **Wet Chemical Clean**
- **Active Area Patterning: LPCVD SiO_2**
- **Dummy Gate Oxide Patterning: PECVD SiO_2**
- **S/D Junction Formation: Spin-on-Dopant(P) + Anneal**
- **Gate Stack: GeON (Plasma or Thermal) + SiO_2 (~10nm) + Al Gate**
- **S/D Contact Patterning: Ni Liftoff**
- **Backside Back Contact: Al**

(a)

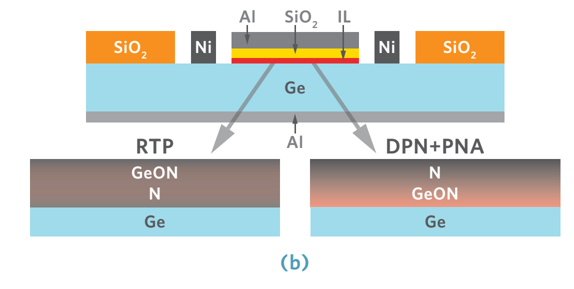

Figure 1. (a) Process flow for Ge nMOSFET fabrication. **(b)** Schematic of the MOSFET; DPN+PNA GeON (right) shows higher N concentration near the surface, but N is more uniformly distributed in RTP GeON (left).

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Figure 2

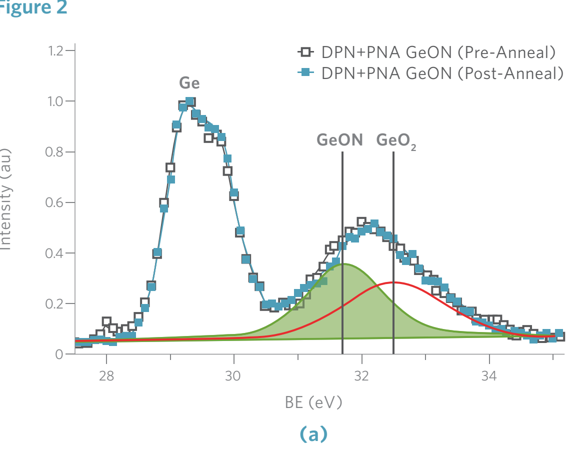


Photo Electron Take-Off Angle
Interface
Surface
(b)

Figure 2. **(a)** Ge 3D XPS spectra for decoupled plasma nitrided GeO_2 (DPN+PNA GeON) pre- and post-thermal stability anneal at 575°C. **(b)** AR-XPS analysis of different ILs.

GeON AND ELECTRICAL CHARACTERIZATION

Gate Stack IL Characterization

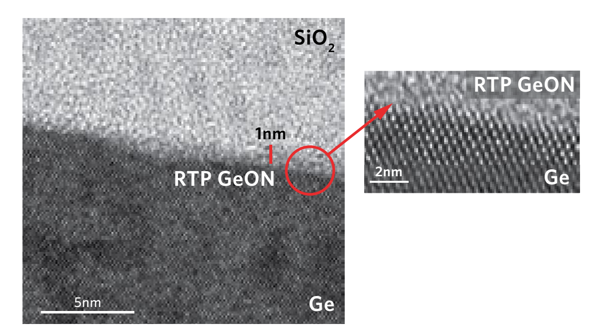
The different ILs were characterized using AR-XPS and TEM. Figure 2a shows the Ge 3D XPS spectra for the DPN+PNA GeON IL with and without a thermal stability anneal (TSA) at 575°C. Peaks with ~3.3eV and ~2.6eV chemical shifts in binding energy (BE) from the bulk Ge 3D peak in the pre-TSA spectrum confirm the growth of the initial GeO_2 layer and nitrogen incorporation during the plasma process, respectively.[4] That there were no significant changes in intensity and BE values pre- and post-TSA demonstrates thermal stability of DPN+PNA GeON up to 575°C, unlike GeO_2, which volatilizes above 400°C.[4] Figure 2b shows nitrogen profiles in the RTP and DPN+PNA GeON ILs, obtained using AR-XPS. DPN+PNA GeON exhibits a lower nitrogen concentration near the Ge/IL interface that increases towards the surface, whereas the RTP GeON shows a more uniform distribution.

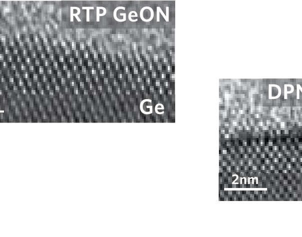
This could lead to a lower D_{it} for the DPN+PNA IL at the IL/Ge interface.[8] The IL thickness is estimated from TEM images (Figure 3) to be 1nm and 1.3nm for RTP GeON and DPN+PNA GeON, respectively. The images also show the amorphous nature of both ILs and smoother interface for DPN+PNA GeON. The DPN+PNA GeON IL is slightly thicker, likely due to some GeO_2 re-growth at the interface during the PNA in O_2 ambient.

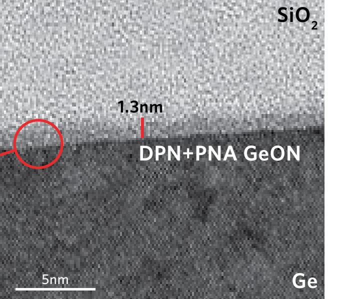
Electrical Characterization

Figure 4a shows frequency-dependent capacitance voltage (C-V) characteristics of MOSCAPs with an $Al/SiO_2/GeON/Ge$ stack. RTP GeON exhibits a much wider frequency dispersion in minimum capacitance compared to DPN+PNA GeON, due to significant generation of minority carriers, which indicates degraded GeON/Ge interface properties. Room-temperature conductance measurements yielded the lowest near-midgap (at E_V-0.35eV) D_{it} of 4.2E+11cm^{-2}eV^{-1} for GeO_2 (Figure 4b). RTP nitridation results in a significant increase in the D_{it} value to 1.05E+12cm^{-2}eV^{-1}, whereas the DPN+PNA process results in a smaller increase to 5.4E+11cm^{-2}eV^{-1}. This trend in D_{it} values is likely correlated to the nitrogen concentration at the GeON/Ge interface.

Figure 3







SiO2
1.3nm
DPN+PNA GeON
5nm
Ge

Applied Materials internal data

Figure 3. TEM images of the SiO_2/IL/Ge stack show the IL thicknesses (left and right) and amorphous IL growth on crystalline Ge (center).

nMOSFET output characteristics showed a 23% improvement in saturation drive current for DPN+PNA GeON compared to RTP GeON IL. Figure 4c plots the electron mobility extracted using the split C-V method, which shows a peak mobility of 1007cm^2/V.s for the GeO_2 IL vs. 818cm^2/V.s for DPN+PNA GeON. The DPN+PNA process shows overall improvement in mobility vs. RTP, indicating fewer coulomb scattering centers (traps) at and near the Ge/GeON interface and less surface roughness, as shown in Figure 3.[10]

Mean D_{it} values were also extracted using the charge pumping (CP) technique. A larger negative V_{FB} shift from ideal was observed in C-V data for RTP GeON (540mV) compared to DPN+PNA GeON (90mV) and GeO_2 (40mV). The lowest mean D_{it} of 2E+12cm^{-2}eV^{-1} was obtained for the Ge/GeO_2 interface. Figure 4b shows RTP GeON with the highest mean D_{it} of 6.3E+12cm^{-2}eV^{-1}, i.e., 1.5 times higher than that for DPN+PNA GeON.

Pulsed vs. Continuous Wave DPN

Further studies examined DPN in pulsed wave (PW) mode vs. continuous wave (CW) mode. For a given effective power (EP) and pressure, PW plasma generates electron density (Ne)—and therefore overall nitrogen concentration—similar to that of CW plasma (Figure 5a). But as its electron temperature (kTe) and plasma potential (Vp) are lower (Figure 5b), PW plasma is gentler and results in less plasma-induced damage in the IL. Given that plasma power is one of the key tuning mechanisms by which to influence nitrogen incorporation in the IL, device comparison of PW vs. CW DPN was conducted with EP held constant. EP for PW DPN is defined as the RF power multiplied by the pulsing duty cycle (DC). Figure 5c shows a decreasing trend of near-midgap D_{it} (at E_V-0.35eV), which can be correlated to the 1.2X improvement in mobility over the CW DPN IL. Enhanced mobility indicates that PW DPN results in less roughness and also improves other properties of the GeON/Ge interface, likely because of the reduced plasma-induced damage to the IL dielectric attributable to the plasma's lower kTe and Vp.

Figure 4

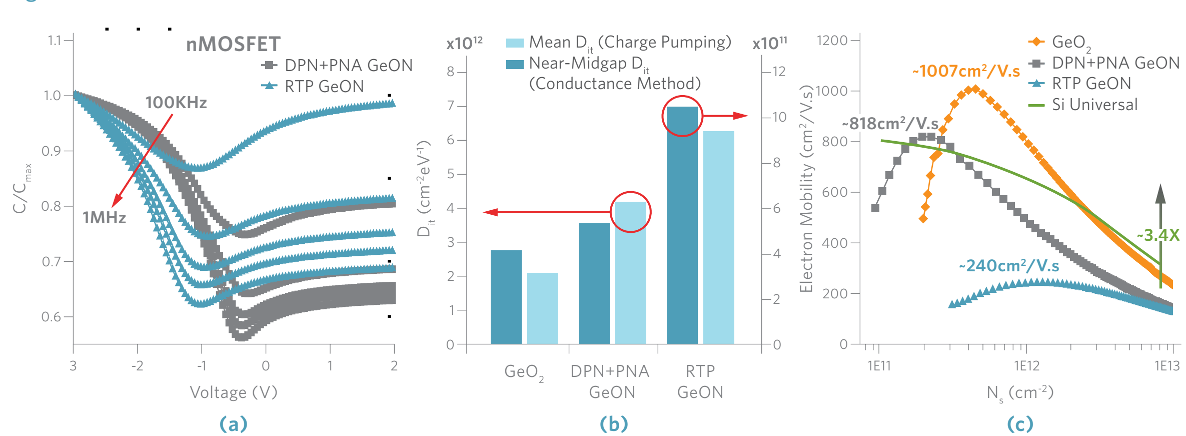


Figure 4. **(a)** Multi-frequency normalized C-V characteristics measured on MOSCAPs for $Al/SiO_2/GeON/p$-Ge stack (EOT~5.5nm) with RTP GeON IL and DPN+PNA GeON IL. **(b)** Mean D_{it} of different ILs as measured using CP method (left axis) and near-midgap (at E_V-0.35eV), and D_{it} obtained using conductance method (right axis). **(c)** Comparative electron mobilities of GeO_2, DPN+PNA GeON, and RTP GeON.

Figure 5

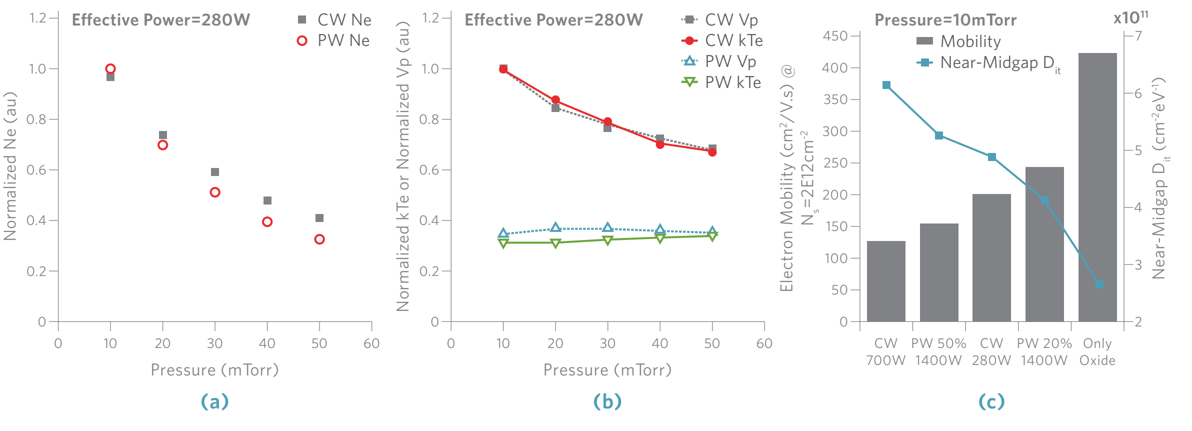


Figure 5. Effect of pressure on CW and PW plasma parameters (frequency=10KHz and DC=20%). **(a)** Normalized Ne and **(b)** normalized kTe and Vp. **(c)** Correlation between electron mobility at N_s=2E12cm^{-2} and near-midgap D_{it} extracted from the conductance method.

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Table 2. Key properties of different IL options for Ge nMOSFETs.

Table 2

IL Property	GeO_2	DPN+PNA GeON	RTP GeON
D_{it}	Best	Better	Worse
Electron Mobility	Best	Better	Worse
Thermal Stability	Unstable[4]	Stable	Stable
Dielectric Constant	~5.5-5.9[3]	Better	6.5[11]

CONCLUSION

A novel GeON formation process using DPN slightly reduces mobility and D_{it}, but exhibits greater thermal stability than GeO_2. This enables a peak electron mobility of 818cm^2/V.s, which is twice the highest reported value for Ge nMOSFETs using GeON ILs formed by RTP (Figure 4c). PW DPN, which reduces the risk of damage to the IL, achieves a further 1.2X mobility improvement over CW DPN while preserving overall nitrogen concentration. These findings confirm GeON as an effective IL for next-generation Ge CMOS gate stack technology. Table 2 summarizes key properties of available IL options.

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PROCESS SYSTEM USED IN STUDY

Applied Centura® DPN Gate Stack

Integrating Ge Channel Materials in pMOSFET

With Epi-Defined FinFET

Conventional integration of Ge p-channel in FinFET architecture is challenging, because very narrow fins are required to reduce I_{off} caused by band-to-band tunneling (BTBT) induced by quantum confinement. The increased I_{off} in turn amplifies the threshold voltage variation that derives from the relatively large ratio of line edge roughness (LER) to fin width. A novel solution defines channel depletion using low-doped, highly uniform epitaxy, exhibiting ten-fold improvement in LER-related variability and 27% higher I_{on}. The approach enables defect-free integration of Ge into FinFET architecture.

FinFET architecture was introduced at the 22nm node to enable scaling that was otherwise being constrained by short-channel effects in planar architecture. Integrating high-mobility channel material in FinFET architecture is the next big challenge. A fundamental problem with high-mobility channel materials is their narrow band gap, which leads to high BTBT leakage current. BTBT leakage must, therefore, be overcome to enable high-mobility materials in FinFET architecture. This can be done by reducing the fin width (W_{fin}). In FinFETs, channel material is confined from two sides by gate oxide, forming a potential well from gate oxide to gate oxide. Reducing W_{fin} increases quantum confinement, which in turn increases band gap. As band gap increases, BTBT leakage decreases.

Device variability has also become a challenging issue accompanying scaling.[1,2] With the introduction of FinFETs, random dopant-fluctuation-based variability is less of a concern.[3] However, the requirement for very narrow fins (~L_G/3)[4] to optimize electrostatic control of the channel makes FinFETs prone to LER-related V_{th} variability.[5] LER in turn leads to W_{fin} variation, which results in greater quantum confinement effects in narrow sections of the fin. For high-mobility channel materials, the W_{fin} affects not only electrostatic control but also BTBT leakage. Thus, W_{fin} requirements could be even more stringent for such materials.

This work focused on these two issues as they relate to a PMOS, in which Ge, with its high hole mobility, was selected as the channel material. Figure 1a shows I_{on} and I_{off} achieved for a Ge PMOS FinFET with various W_{fin}. It shows that a fin 4nm wide is needed to satisfy a specification of 100nA/μm I_{off}, a target more stringent than that for a Si FinFET. Given the rule of thumb L_G/3, a Si FinFET would have to be 5nm wide. Figure 1a also shows the I_{on} boost achieved by the Ge FinFET over the Si FinFET, demonstrating the benefit of integrating Ge as a channel material.

Figure 1b shows the shift in V_{th} as W_{fin} varies. These studies used 3σ variation of 1.5nm on both edges of the FinFET. Wang, et al., used a 3σ variation of 2nm,[5] but that value would result in W_{fin} of zero for thinner fins. A Si FinFET W_{fin} of 4nm was also used for comparison. Note that for fins of less-than-nominal widths, V_{th} fluctuation could be 250mV more for Ge than for Si. The reason for the difference is that Ge is a lower band gap material; consequently, it is subjected to more confinement effects than Si. This effect manifests itself in a large V_{th} variation as W_{fin} varies. Given that these results are based on only moderate LER, it is clear that LER-related variability is a critical factor in Ge FinFETs.

These studies investigated the feasibility of eliminating the effect of LER on device performance by defining channel depletion through creation of an epitaxy-defined (ED) FinFET rather than by lithographic patterning.

KEYWORDS
Epi-Defined FinFET
Epitaxy
FinFET
Germanium
Leakage Current
V_{th} Variability

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Epi-Defined FinFET

Figure 1

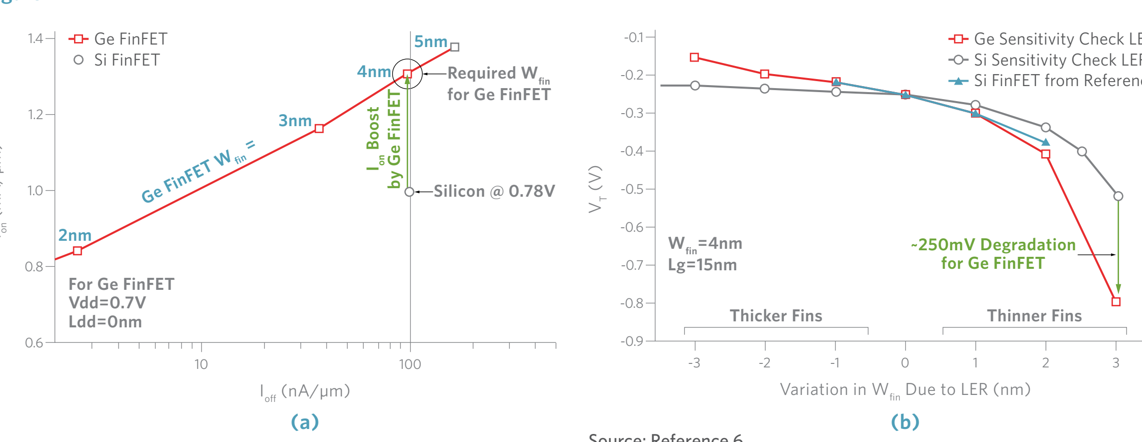

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Figure 1. (a) I_{on} and I_{off} vs. W_{fin}, and I_{on} boost in Ge FinFET over Si FinFET. **(b)** Change in V_{th} as W_{fin} varies in Si and Ge FinFETs.

FABRICATION

Figure 2a illustrates the fabrication sequence for an EDFinFET. To simulate LER-related variability, structures were generated by a Gaussian autocorrelation model[1] with the root mean square amplitude 3σ=1.5nm and correlation length Λ=30nm, and modeled by a sine function (i.e., LER=3σsin(2πx/Λ)±W/2) in which W is the W_{fin} (Figure 2b).[7] For Ge FinFETs, only a sensitivity check was performed, equivalent to a correlation length of infinity. With an increase in correlation length, V_{th} variability decreases; hence, the results shown are conservative and can be considered valid.

To determine I_{on} for an EDFinFET, Monte Carlo simulations with the inclusion of biaxial stress were performed, using the Sentaurus™ non-local tunneling model.[7] This model has been well-calibrated to data in the literature[8] to account for BTBT leakage in Ge. Trap-assisted tunneling and Shockley-Read-Hall recombination/generation models and mobility models also calibrate well with the literature.[8] Biaxial stress was calculated using Sentaurus Sband.

Figure 2

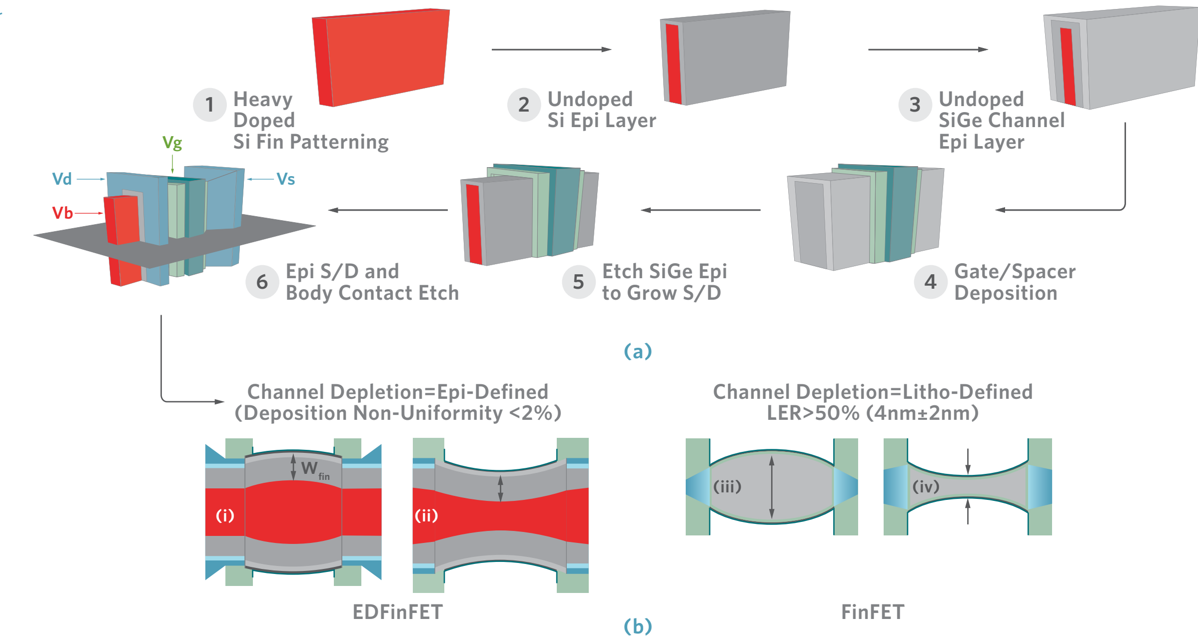


Figure 2. (a) Process flow for fabricating a SiGe channel EDFinFET. **(b)** EDFinFET and FinFET structure subjected to LER variation of 3σ=1.5nm and Λ=30nm.

ANALYSIS AND RESULTS

V_{th} Variability

FinFETs suffer from LER-related variability because the fin is fully depleted or subjected to bulk inversion dependent on bias conditions and the entire W_{fin} contributes both in electrostatics and transport [e.g., enhanced quantization in narrow regions (Figure 2b-iv)]. To overcome the extreme quantum confinement effects responsible for the V_{th} variability seen in Ge FinFETs, Ge PMOS EDFinFETs can be fabricated according to the steps shown in Figure 2a.[9] They are similar to those cited by Mittal[9] except for depositing a layer of epitaxial SiGe on top of undoped epitaxial Si. The SiGe forms the channel layer and is confined by SiO_2 on one side and Si on the other. This produces the quantum confinement required to reduce BTBT leakage current.

Figure 2b-i and ii show channel depletion in EDFinFETs defined by a thin, lightly doped, highly uniform epitaxy (thickness non-uniformity <2%) over a thick, highly doped Si fin rather than by lithographic patterning subject to LER (non-uniformity <50%, i.e., <2nm LER on a 4nm fin) as shown in Figure 2b-iii and iv. Because the depletion width is defined by undoped SiGe epitaxy, it remains uniform, unaffected by LER on the heavily doped fin beneath. The underlying W_{fin} cannot be depleted so cannot contribute to electrostatics. This configuration thereby eliminates V_{th} fluctuation caused by quantum confinement.

Figure 3a shows the improvement in LER-related variability obtained. EDFinFET improves V_{th} variability by approximately 500mV over Ge FinFETs for the reasons mentioned above. As LER 3σ numbers depend highly on the lithography scheme used, further analysis addressed overall variability of the three next-generation lithography techniques, namely self-aligned dual patterning (SADP), nano-imprint lithography (NIL), and extreme ultra-violet lithography (EUV).

Figure 3b shows that EDFinFET technology has an advantage over FinFET regardless of lithographic approach and that the dynamic threshold (DT) MOS[10] configuration substantially boosts the advantage. Thus, EDFinFET appears to solve one of the major problems in integrating SiGe or Ge into FinFET architecture.

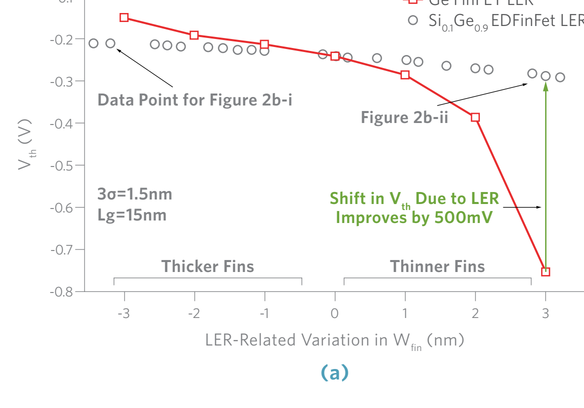
Performance

BTBT leakage in SiGe EDFinFET can be reduced through quantum confinement obtained by sandwiching a layer of strained SiGe between the SiO_2 and Si. Strained Ge has a narrower band gap than does relaxed Ge, which would increase quantum confinement even further. The net effective band gap obtained in this manner is sufficient to reduce BTBT leakage below the specification limit. As shown in Figure 4a, an epitaxial SiGe layer less than 1.5nm thick reduces I_{off} to less than 100nA/μm.

Simulations were performed for three different percentages of Ge in the SiGe layer. Figure 4b shows the structure in which the I_{off} criterion was met, i.e., I_{on} at I_{off}=100nA/μm. Note that as the Ge percentage increases, I_{on} increases. Higher I_{on} is achieved with 1.5nm of 100% Ge grown on top of the Si. Krishnamohan has shown that it is possible to grow defect-free Ge this thick.[11] The EDFinFET approach enables defect-free integration of Ge into FinFET architecture.

Figure 5 compares drain current with gate voltage for several FinFET configurations. Drift-diffusion plots are shown on a log scale on the left y-axis and Monte-Carlo

Figure 3



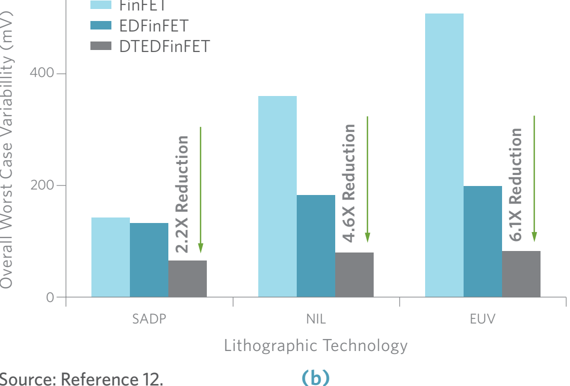


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Figure 3. (a) LER-related V_{th} variation in SiGe EDFinFET and Ge FinFET, showing 500mV improvement in EDFinFET over Ge FinFET. **(b)** EDFinFET and DTEDFinFET exhibit less V_{th} variability than FinFET for leading next-generation lithographic technologies.

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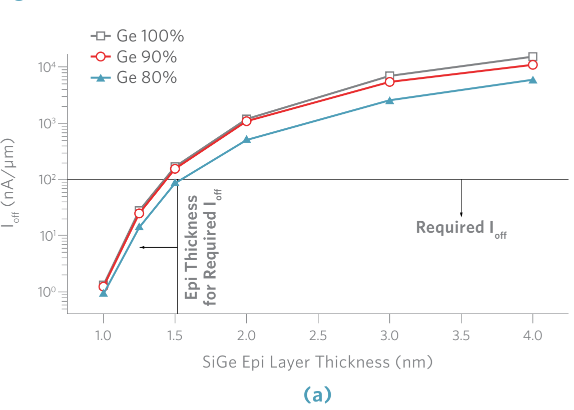
Figure 4



(b)

Figure 4. (a) For SiGe 1.5nm thick or less, I_{off} is less than 100nA/μm for all compositions. **(b)** Current boost due to biaxial strain. I_{on} is calculated using Monte Carlo simulations and shown for the case when I_{off} is below 100nA/μm.

plots are shown on a linear scale on the right y-axis. The latter show that I_{on} in the EDFinFET substantially exceeds that in the FinFET. This is because the EDFinFET is biaxially stressed from beneath. Also, the EDFinFET is a surface inversion device, while FinFETs are bulk inversion devices. The EDFinFET therefore has an inherent effective oxide thickness benefit.[9] EDFinFET, however, suffers from poor sub-threshold slope (SS), the result of being essentially a single-gate device. But SS can be restored in the DTMOS[13] configuration, which also improves I_{on} by 43% over the FinFET, as shown on the log scale plot.

Multiple V_{th} Capability

A body terminal for each EDFinFET device can also be integrated into the process flow for making the device, affording a unique advantage in reducing system-level power. The body effect coefficient of EDFinFETs is a robust 425mV/V vs. 6-9mV/V for FinFETs.[13] By changing the fixed bias at the body terminal, the V_{th} of different devices can be variously tuned during operation. Multiple V_{th} is much desired for enabling high performance (HP), low operating power (LOP), and low standby power (LSTP) technologies on the same die. Setting different body biases during operation allows EDFinFETs to function in any one of these modes (Figure 6). The weak body effect coefficient of conventional FinFETS rules out this capability. To achieve the same effect in planar devices is even more complex, as evident by reports in the literature of simulating multiple work-functions for the gate electrode and gate-source/drain overlap engineering.[14]

I_{on} Per Unit Area

EDFinFET fins are 33nm wide compared to 4nm in FinFETs. Consequently, they are more stable and can be grown taller. Applying Choi's stable fin calculation,[15] it can be shown that EDFinFET fins are 2.4 times taller for the same area. Multiplying this added height by the inherent I_{on} benefits of the EDFinFET can triple the I_{on} per footprint. Similarly, the inherent I_{on} benefit of DTEDFinFET is higher than that of the EDFinFET. This translates into a three- to six-fold improvement in I_{on} per unit footprint, depending on device configuration, proving that the slight increase in the thickness of fins in EDFinFETs is not necessarily an advantage.

Figure 5

Figure 5. Comparison of FinFET, EDFinFET, and DTEDFinFET drain current vs. gate voltage. EDFinFET improves current by 27% and DTEDFinFET by 83%.

Figure 6

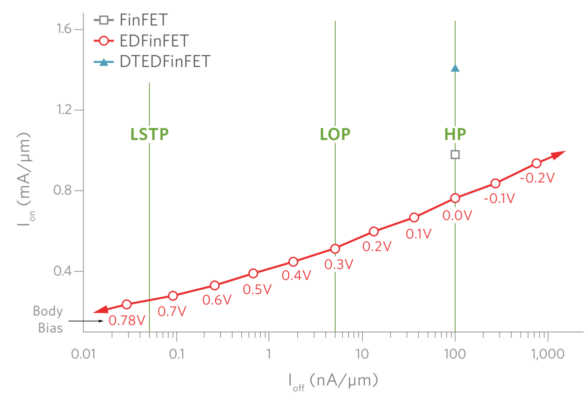


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Figure 6. Setting EDFinFET body biases during by-operation enables multiple V_{th} and multiple power modes on the same die.

CONCLUSION

The modified EDFinFET proposed here solves key Ge FinFET integration problems in the following ways. First, it defines channel depletion through epitaxy instead of lithography, leading to ten-fold improvement in worst-case LER-related V_{th} variability. Second, very thin layers of defect-free Ge can be epitaxially grown on Si to help reduce confinement-induced I_{off} and increase I_{on} by biaxial strain. Third, greater fin thickness enhances mechanical stability and enables taller fins that produce three to six times higher I_{on} per unit footprint. Finally, multiple V_{th} capability can be realized by varying the bias at the body following fabrication. Based on these advantages, EDFinFETs make possible the integration of high-mobility Ge into FinFET architecture with a variety of benefits unmatched by conventional FinFETs.

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PROCESS SYSTEM USED IN STUDY

Applied Centura® RP Epi

Tuning Threshold Voltage for 10nm CMOS Integration

Using Metal Gate Work Function Modulation

KEYWORDS

Conductance
Metal Gate
Multi-V_{th} Tuning
Self-Aligned Contact
Threshold Voltage
Work Function Metal

Viable replacement gate FinFET architecture is essential for extending high-performance CMOS scaling. Similarly, multiple threshold voltage (V_{th}) capability will be required for future ultra-large-scale integrations. Conformal deposition of differing work metals in conjunction with ion implantation achieves precise control of effective work function for multiple V_{th}, good conductivity in <15nm gate trenches, and compatibility with self-aligned contacts.

With continued downward scaling, the leading edge of the industry is capitalizing on the third dimension to enable logic and memory devices that deliver high performance at low power levels.[1,2] Integrating 3D devices into ICs at the 10nm node and beyond requires solutions to several new requirements. This study focused on aspects of metal gate performance that will be critical for 10nm node CMOS technology and beyond. These are 1) precise effective work function (eWF) control over a 600mV range to enable multiple V_{th}; 2) sustained conductivity in sub-15nm gate trenches; and 3) compatibility with self-aligned contact (SAC).

SAMPLE PREPARATION

A MOSCAP was used to evaluate the impact of metal composition and ion implantation on eWF. Some of the samples were implanted after high-κ and work function metal (WFM) deposition on blanket wafers (Figure 1). As a concept and feasibility check, beam-line implantation was used based on TRIM simulation.[3] The samples were subjected to forming gas anneal at 400˚C after MOSCAP patterning; high frequency capacitance voltage and input voltage were then measured. A single damascene structure was used to measure resistance in sub-20nm lines. A planar MOSFET was also used for evaluating impact on V_{th} and its variability.

PERFORMANCE EVALUATION

Work Function Modulation

Figure 2a shows the eWF of the reference RFPVD Ti-Al compared with that of three differing compositions of NMOS nWFM. The 550mV range in eWF derives from nWFM composition control. Figure 2b illustrates the additional 100-150mV WF enhancement that results from nitrogen implant into the nWFM. The WF range now extends from a low of 4.1eV to an above mid-gap value of 4.7eV. The range can be extended to 5.0eV with a pWFM (e.g., TiN). As shown in Figure 2c, the WF shift corresponds closely to implant dose levels; therefore implant can target the desired WF/V_{th} by increments of 100-150mV. Furthermore, implant into nWFM does not degrade gate leakage and effective oxide thickness performance.

Figure 1

- p-/p+ Wafers
- Pre-Clean
- Interface Oxide and ALD HfO_2
- High-κ Cap TiN 1-2nm
- Work Function Metal 4-5nm
- Ion Implant
- Pad Metal TiN
- MOSCAP Patterning
- FGA at 400°C

Figure 1. MOSCAP process flow.

Conductance for the 10nm Node

According to the ITRS roadmap, gate length is expected to be 17nm at the 10nm node.[4] At these geometries, deposition of the high-κ cap and etch-stop layer results in gate trench CD of 15nm or less, severely limiting the volume available for metal fill.[5] One solution is to fully or mostly fill the trench with a WFM such as Ti-Al for NMOS and TiN for PMOS. Figure 3a is a top-down SEM image of 13nm trenches filled with a void-free, advanced PVD Ti + PVD Al fill, taken after CMP. Figure 3b illustrates the extendible conductance of PVD Ti-Al and WF fill.

Low WFM for NMOS is more prone to oxidization than are the high WF PMOS films, such as TiN. It has also been reported that air exposure affects V_{th} control.[6] In addition, the present work revealed degradation of conductance curves from air exposure, as shown in Figure 4a. The exposed sample shows a large offset of the conductance curve to the right while differential resistivity (slope) remains constant. The transmission electron microscope (TEM) image in Figure 4b shows an additional layer between TiN barrier and nWFM. Scanning transmission electron microscope electron energy loss spectroscopy analysis confirmed high oxygen concentration in the white interface. In-situ nWFM processing is therefore crucial for maintaining conductivity at the 10nm node.

Figure 2

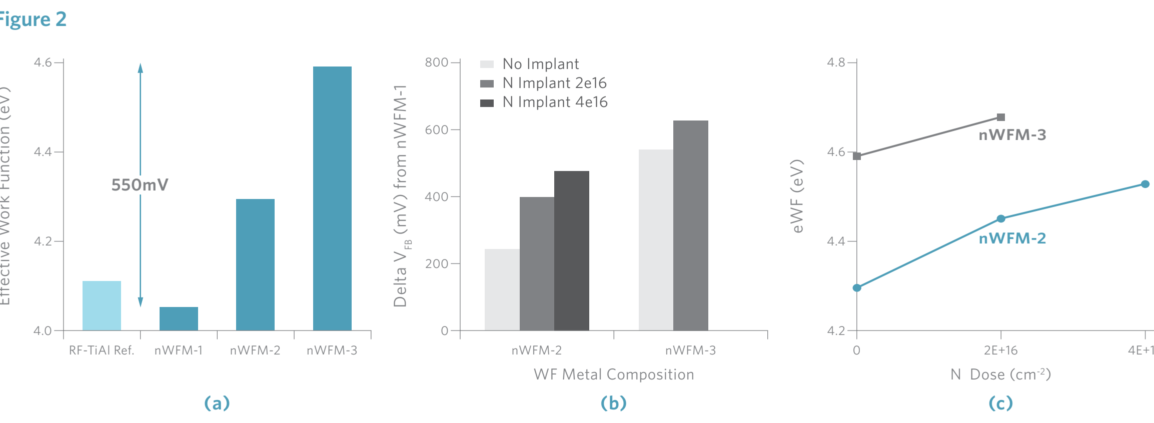


Figure 2. (a) Effect of binary metal composition on eWF. **(b)** Effect of nitrogen implant on eWF. **(c)** Correlation of eWF with implant dose.

Figure 3

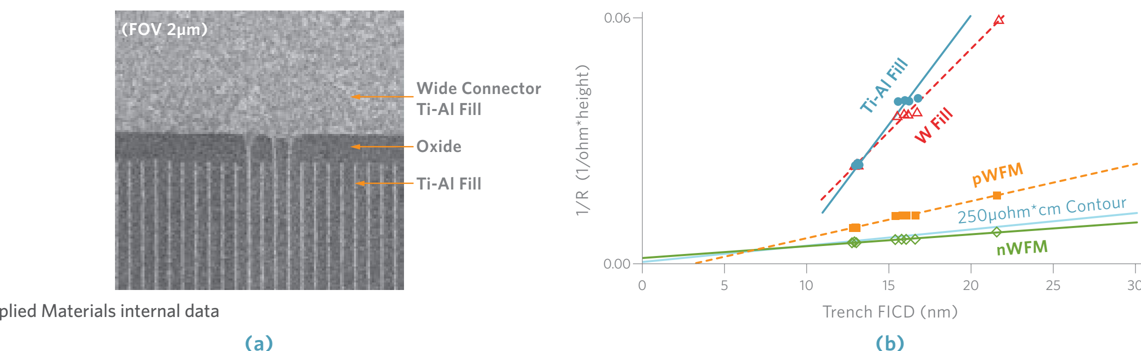
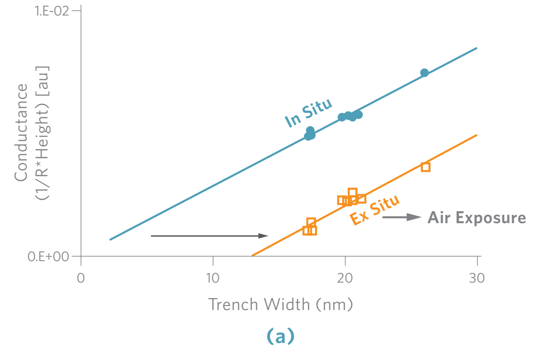


Figure 3. (a) Void-free Ti-Al fill of 13nm trenches. **(b)** Extendible conductance of PVD Ti-Al and WFM fill.

Figure 4



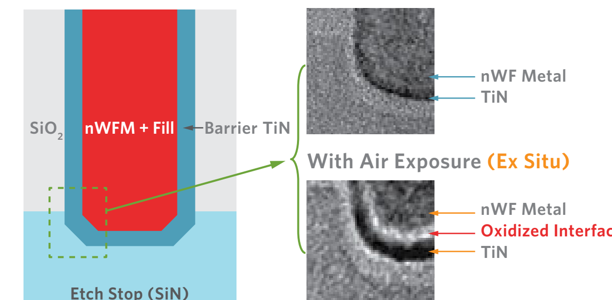


Figure 4. (a) Effect of air exposure between TiN barrier and nWFM on conductance in trenches narrower than 30nm. **(b)** Comparison of TiN barrier and nWFM interface showing oxidation resulting from exposure to air.

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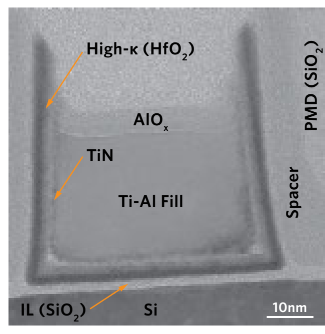
Threshold Voltage Tuning

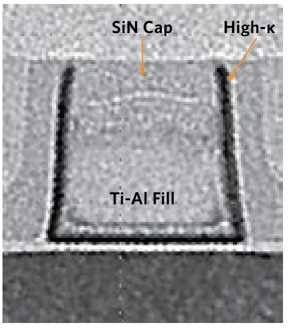
SAC Compatibility and CMOS V_{th} Tuning

At the 22nm technology node, metal gate SAC is necessary to scale the contacted gate pitch.[1] This requires a well-controlled etchback of the metal gate and subsequent capping with etch stop material, such as SiN, to prevent contact-to-gate shorts. Controlled recess etch can be achieved with Ti-Al fill, as shown in Figures 5a-b. Figure 5c illustrates successful formation of the post-CMP SAC cap of high-density plasma SiN.

Multiple WFM must be integrated for CMOS V_{th} tuning in NMOS and PMOS. Figure 6a shows an example CMOS WFM flow to achieve four V_{th} values. The work described here suggests that barrier TiN and nWFM be deposited under continuous vacuum (i.e., using cluster processing) following deposition of the high-κ and etch stop layers. (Some areas can be masked by photoresist and modified by implant of the exposed area.) The first nWF layer (N-2 in Figure 6a) can then be etched from the PMOS areas after which the second WFM (N-3) and barrier can be deposited. Following this, the second implant can be carried out to shift the WF of the third device. Finally, the nWFM is again etched away from the PMOS area WFM (TiN) and the remaining gap filled with W or Al. The final TiN serves as the highest WF as well as the barrier layer for the W or Al. This flow produces four V_{th} values and metal fill with a clustered nWFM film stack. Figure 6b plots V_{th} of planar MOSFETs consisting of two different nWFM combinations, while Figure 6c shows that V_{th} varies by approximately 100mV without affecting variability.

Figure 5



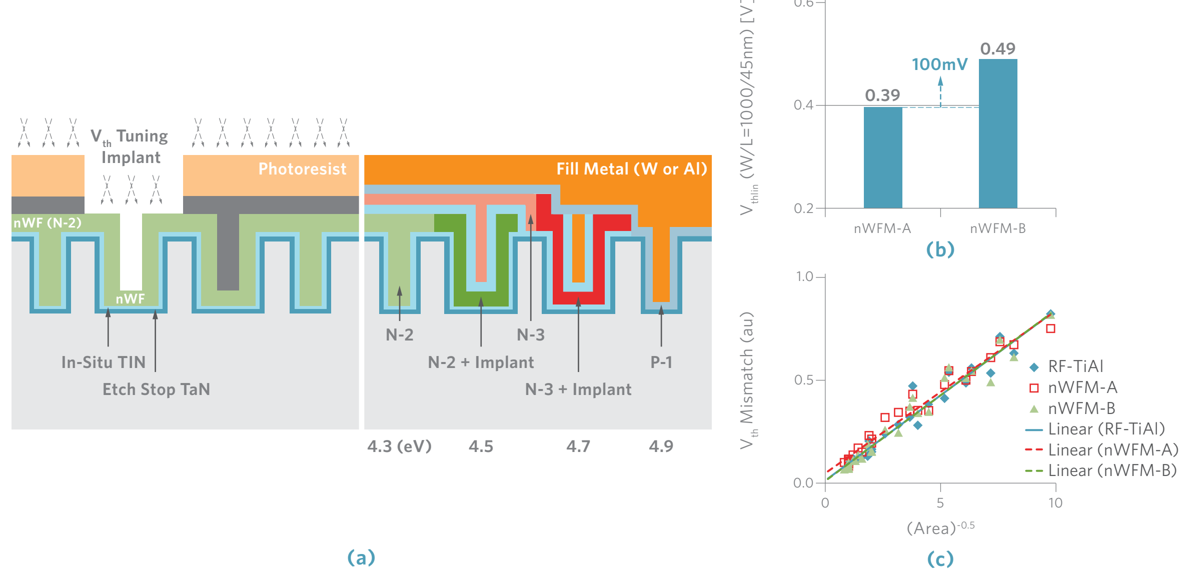


Applied Materials internal data

(a) (b) (c)

Figure 5. (a,b) Cross-sectional TEMs show controlled etchback of Ti-Al fill for SAC integration. **(c)** Cross-sectional TEM after SiN cap deposition and CMP.

Figure 6



(a) (b) (c)

Figure 6. (a) Process steps from implant to nWFM and final four-V_{th} gate series after WFM tuning. **(b)** 100mV shift in V_{th} achieved by changing composition of nWFM. **(c)** Two combinations of nWFM show comparable V_{th} variability.

CONCLUSION

Metal WF modulation for V_{th} tuning was successfully demonstrated for 10nm CMOS integration with a new scheme tunable over a range of 600mV. Ion implantation dose control enabled continuous WF tuning for multiple V_{th} targets. Metal gate conductance data showed the necessity for in-situ processing with a TiN barrier and NMOS WF metal. A CMOS flow with nWFM-first was proposed for multi-V_{th} tuning.

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PROCESS SYSTEM USED IN STUDY

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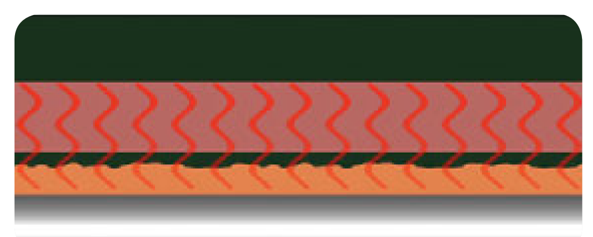
Dry Removal Technology

for Advanced CMOS Devices

KEYWORDS
Dry
FinFET
Oxide
Pattern Collapse
Recess
Removal
Selectivity
Wet Clean



As device dimensions shrink and feature aspect ratios increase in FinFET, floating gate NAND, vertical NAND, and DRAM, stiction-related pattern collapse during wet cleaning and etch processes has become a significant issue. Integration of lower-density dielectrics in response to lower thermal budgets in next-generation logic and memory device flows also drives the need for a more controllable, oxide-density-independent removal process. Dry removal technology is effectively resolving these issues at advanced nodes.

In logic/foundry or memory process flows, the number of oxide removal and recess applications is increasing as the device node shrinks. These applications can be divided into two categories: (1) surface cleaning to remove native oxide before metal, epi, or other material deposition (i.e., integrated clean/deposition) and (2) non surface-cleaning stand-alone applications to enable device performance (uniform and precise oxide recess or removal).

Table 1 highlights various stand-alone dry removal applications, ranging from precision recess to complete oxide removal. The introduction of FinFETs has increased the number of oxide recess steps while adding the new requirement for 3D oxide removal.

Table 1

Device	Applications
Logic	Shallow Trench Isolation (STI) Oxide Deglaze
	Pad Oxide Removal
	Interlayer Dielectric (ILD) Oxide Recess
	Dummy Oxide Removal
	STI Recess
	Sacrificial Oxide Removal
Memory	STI Oxide Recess
	ILD Oxide Recess
	Oxide Recess in Vertical NAND

Table 1. Examples of oxide removal applications in logic/foundry and memory devices.

Non-surface-cleaning applications require: (1) uniform and precise recess; (2) flat profile, no pattern loading, and minimal roughness; (3) removal rate insensitive to oxide deposition method; (4) oxide removal selectivity to Si, nitride, or other films; and (5) preservation of pattern integrity in high aspect ratio features.

WET REMOVAL LIMITATIONS

Wet chemical removal of silicon dioxides typically employs a diluted HF (hydrofluoric acid) or buffered oxide etch solution. Stiction can cause pattern collapse during these wet processes (Figure 1a). This pattern deformation is defined by the following equation,

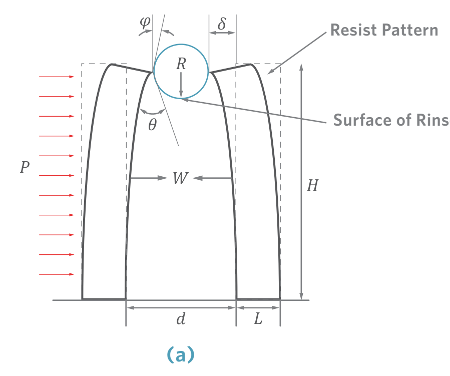
$$\delta \approx \frac{6\sigma \cdot \cos\theta \cdot H^4}{2 \cdot d \cdot E \cdot L^3} \quad [1]$$

where δ is deformation, σ is surface tension, θ is contact angle between liquid and pattern, d is distance between patterns, H is pattern height, E is elastic modulus, and L is the width of line patterns.

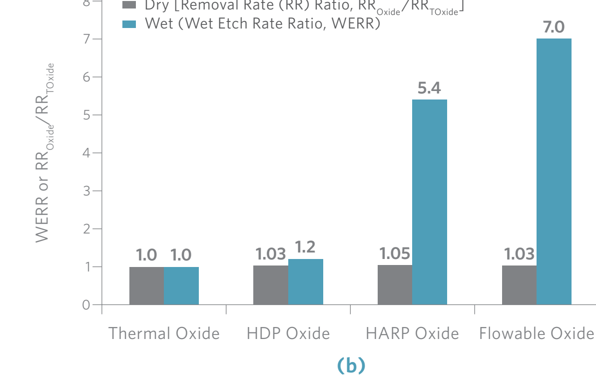
As design rules shrink, d and L decrease while H increases. In addition, adoption of lower κ dielectrics results in lower E. Consequently, pattern deformation from wet chemistry increases significantly, causing pattern collapse. Optimization of wet chemistries to reduce surface tension and contact angle to lessen deformation is reaching its limits, necessitating an alternative process.

Wet removal also poses the challenge of controlling the removal rate of oxides with varying densities (Figure 1b). Device manufacturers must integrate softer dielectrics at advanced nodes. Thermal budgets have decreased substantially in logic, DRAM, and flash; hence, high-temperature steam anneals can no longer be employed to densify the dielectrics. Wet process removal rates are highly correlated with the density of the dielectric material, which results in divot defects or concave-shaped removal profiles in the softer dielectrics. Overcoming these wet chemistry limitations requires a dry process that removes oxides of different densities at a uniform rate without causing pattern collapse or plasma damage.

Figure 1



(a)



(b)

Figure 1. Wet chemistries suffer disadvantages, including **(a)** pattern deformation and **(b)** non-uniform removal rate.

DRY REMOVAL ALTERNATIVE

An in-situ dry oxide removal process has been developed as detailed below. First, etchants (NH_4F or $NH_4F{\cdot}HF$) react with the dielectrics to form a solid by-product [$(NH_4)_2SiF_6$]. This is then sublimated, exposing the dielectric surface. The etchants are generated by the reaction of NF_3 and NH_3/H_2 in a remote plasma configuration. A low wafer temperature is maintained during the etch process to condense the etchants on the dielectric surface. The wafer temperature is then elevated above 100°C to sublimate the by-products.

Typical reactions are:

Etchant Generation:

$NF_3 + NH_3 \rightarrow NH_4F + NH_4F{\cdot}HF$

$NF_3 + H_2 \rightarrow HF + NH_4F$

Etch Step:

$NH_4F + SiO_2 \rightarrow (NH_4)_2SiF_6 + H_2O$

$NH_4F{\cdot}HF + Si_3N_4 \rightarrow (NH_4)_2SiF_6 + H_2O$

By-Product Sublimation:

$(NH_4)_2SiF_6\ (solid) \rightarrow SiF_4(g) + NH_3(g) + HF(g)$

The etch and sublimation steps can be repeated as many times as necessary. Process parameters (chemistry, gas flows, pressure, temperature, plasma power) can be varied to modulate the etch rate and the saturation regime (Figure 2). The etch rate can be varied from ~1Å/sec to >10Å/sec to achieve the degree of removal precision appropriate for the target application.

The dry process etches oxides of differing densities at a similar rate (Figure 1b) to produce divot-free results. Figure 3 shows a near-parity oxide removal rate ratio between pad oxide and STI fill oxide, resulting in divot-free removal and minimal STI opening. The dry removal chemistry etches oxide with >150:1 selectivity to Si and to new materials, such as SiGe and high κ (HfO_x, $HfSiO_x$) used in advanced devices. Selectivity of oxide to nitride removal can be varied by process modulation.

Figure 2

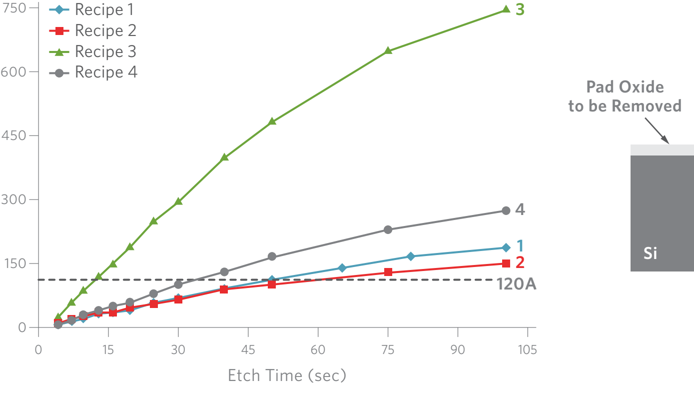


Figure 2. Dry removal process modulation.

Figure 3

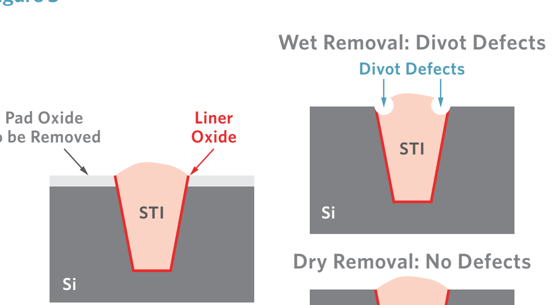


Figure 3. Wet vs. dry pad oxide removal.

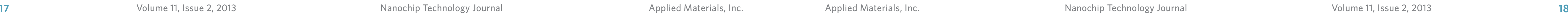


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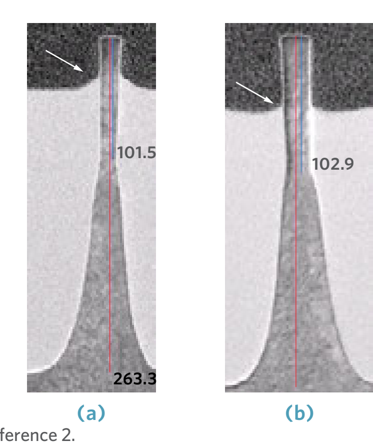
Figure 4 compares wet and dry removal processes in a FinFET STI application. The wet chemistry process results in the formation of an oxide foot at the base of the electrical part of the fin; this can degrade performance of the final device. The dry process leaves no foot and recess control is significantly improved by the iterative nature of the etch-sublimation process.

Figure 4



Source: Reference 2.

Figure 4. STI oxide recess comparison. **(a)** Wet etch leaves foot at base of fin. **(b)** Dry removal eliminates foot and improves recess control.

Pattern loading can also be achieved by modulating the dry removal reactant gases. An NF_3-NH_3 chemistry results in an etch that is faster in wide features than in narrow features. Conversely, an NF_3-H_2 chemistry etches narrow features faster than wide features. A combination of the two chemistries achieves a uniform removal rate (Figure 5).

Figure 5

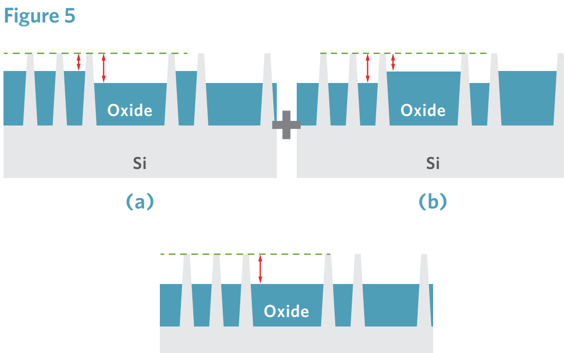


Figure 5. Pattern loading modulation: **(a)** faster etch on wide trenches, **(b)** faster etch on narrow features, and **(c)** no pattern loading with a combination of the two chemistries.

CONCLUSION

As device scaling continues, wet oxide removal chemistry is reaching its limits. A single-chamber, dry removal process consisting of alternating etch and sublimation steps has been developed that removes oxides at a similar rate, independent of their densities or selectivity to Si, nitride, and new materials. Dry removal delivers a flat profile and can be tuned to eliminate pattern loading between narrow and wide features. This process is being widely adopted across the industry as advanced applications requiring an alternative to wet chemistry have proliferated.

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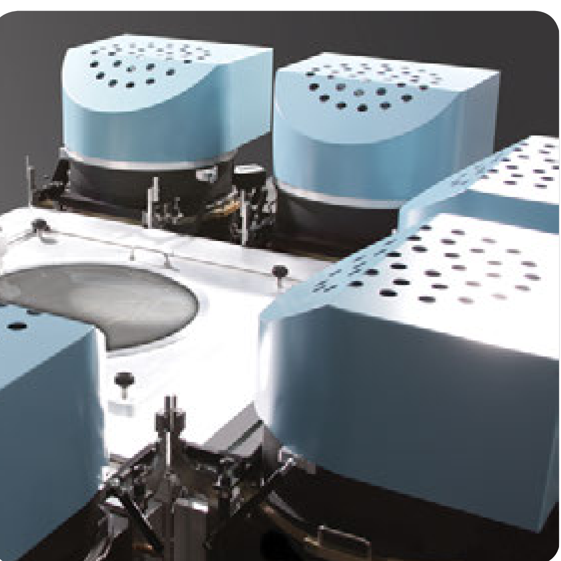
Reducing Etch Defectivity

With High-Performance Chamber Materials

KEYWORDS
Chamber
Coating
Defects
Erosion
Etch



The size of killer defects is shrinking along with feature critical dimensions. New materials and chemistries that make possible continued scaling or 3D architectures are also subjecting chamber surfaces to process environments not previously encountered. Both factors are driving advances in fortifying erosion resistance and microstructural stability of chamber components. A new high-performance plasma coating material is demonstrating benchmark low defectivity in a wide range of plasma chemistry environments.

With every device node as Moore's Law progresses, the dimensions of so-called killer defects decrease. At the 2xnm node, the killer defect size has shrunk to 45nm and these smaller defects are beginning to cause yield loss. Compounding this challenge is the employment of new materials (films) on the wafer, prompting use of new etch chemistries that are attacking chamber materials in ways not previously seen. In particular, hydrogen-based chemistries and new aggressive chamber cleaning chemistries can attack chamber components, leading to an increase in the number of defects over time.

Materials used in dry etch chambers have evolved significantly over the last two decades. Liners used in both inductively coupled plasma (ICP) and capacitively coupled plasma (CCP) etch chambers have progressed from bare aluminum to anodized aluminum (which produces an Al_2O_3 coating) to aluminum with specialized rare earth oxide coatings [e.g., yttrium oxide (Y_2O_3)], typically applied using plasma spray technology.

In addition, a dielectric lid is used in ICP etch chambers to separate the radio frequency (RF) source from the vacuum chamber. More than a decade ago, the lid was made from bulk alumina (Al_2O_3). However, this material reacts with fluorine-based chemistry to form AlF_x, which produces such on-wafer defects as particles and metal contamination. In turn, these defects resulted in short mean time between cleans (or MTBC) that reduced chamber up time and productivity. Alumina lids were replaced with bulk rare earth oxide materials that have much improved halogen plasma erosion resistance and microstructural stability.

These rare earth oxide materials, however, are not compatible with reducing chemistries, such as carbon monoxide, hydrogen, and methane, etc. In their place, new high-performance materials (or HPMs) have been developed (Figure 1) and successfully used in a wide range of plasma chemistry environments.

Figure 1

Figure 1. Advanced coatings are used on process kits, chamber sidewalls, and chamber lids.

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HPM DEVELOPMENT

Research and development on etch-resistant coating materials based on rare-earth oxides has been evolving over the past ten years. Materials design employs rigorous analysis and understanding of phase diagrams of various metal oxide systems to optimize critical deposition parameters. Plasma spray deposition has been advanced though extensive use of multi-factorial design-of-experiment (DOE) methodology. Iterative DOEs have enabled optimization of coating process parameters to improve etch resistance, porosity, roughness, and other material characteristics for improved performance and component lifetime. Current research is also examining suspension-plasma spray using nano-particles to reduce coating porosity and roughness. Besides plasma spray techniques, research is being conducted into other advanced coatings, such as ion-assisted deposition, plasma-enhanced CVD, and PVD.

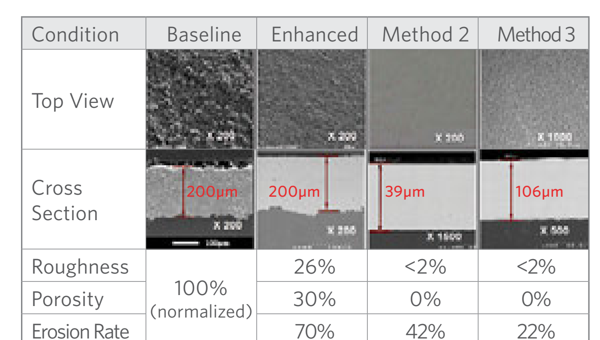
HPMs are Y_2O_3-based ceramic composites developed to meet a wide array of property requirements, such as porosity and roughness, breakdown voltage, and resistance to erosion and corrosion, for critical chamber components exposed to plasma. HPMs can be used either in the bulk form or as a coating. Investigations encompassed diverse material compositions and deposition techniques. Figure 2 shows selected results illustrating improved properties of HPM coatings.

Erosion resistance is one of the first considerations in selecting chamber materials as it is highly correlated to component lifetime and defect performance. When testing materials for this property, the most representative conditions are obtained by mounting sample coupons in working etch chambers and subjecting them to prolonged plasma exposures, typically on the order of 100RF hours. As shown in Figure 3, the newly developed HPMs show the lowest erosion rates in both reducing and non-reducing plasma environments.

Composition has a significant impact on inherent microstructural defects in the coatings that contribute to elevated on-wafer particle counts. Figures 4a and b show a SEM and transmission electron micrograph (TEM) of commonly used rare earth oxide coatings. The images show micro- and nano-scale cracks and pores in the coatings; these lead to on-wafer particle defects in a corrosive plasma environment.

Such cracks and pores are the result of complex crystal phase change (and associated volume change) during rapid melting and solidification of the rare earth oxide during plasma coating. They can be significantly reduced by carefully controlling the composition of the coating material and coating process parameters. In Figure 4c, the TEM of a new HPM coating shows much improved microstructure and little or no nano-scale cracking.

Figure 2



Condition	Baseline	Enhanced	Method 2	Method 3
Top View				
Cross Section	200µm	200µm	39µm	106µm
Roughness	100% (normalized)	26%	<2%	<2%
Porosity		30%	0%	0%
Erosion Rate		70%	42%	22%

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Figure 2. HPM coatings with improved properties (normalized).

Figure 3

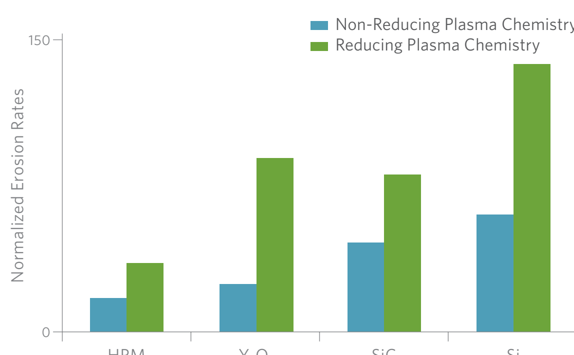
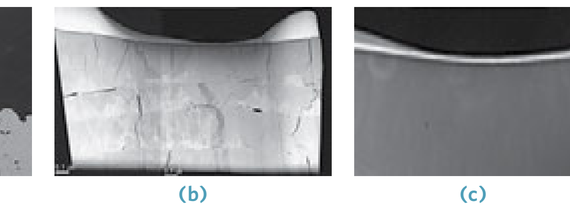


Figure 3. Erosion rate of various materials in reducing and non-reducing plasma chemistries.

Figure 4



(a) (b) (c)

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Figure 4. Coating comparison: **(a)** SEM of rare earth oxide shows partially dislodged nodule of a coated chamber component. **(b)** TEM of rare earth oxide reveals high density of nano-scale micro-cracks. **(c)** TEM displays no visible cracks or pores in HPM.

Figure 5

Standard (Y-O) Liners
HPM-Coated Liners
Particle Count (≥45nm Size)
RF Hours

Figure 5. On-wafer particle (greater than or equal to 45nm) counts in reducing chemistry confirm dramatic reduction with HPM-coated liners.

IMPLICATIONS FOR ADVANCED ETCH

Chamber components protected with the new HPM coatings demonstrate significant improvement in on-wafer defect performance, both in-house and at customer manufacturing lines for 2xnm node devices. Figure 5 shows side-by-side comparison of a standard rare earth oxide coating and HPM measured over 100RF hours under reducing chemistry. Upon installation, particle defects are nearly an order of magnitude lower for the HPM-coated components and remain consistently low over extended chamber exposure.

As shown in Figure 6, advanced materials development for plasma etch chambers has required an understanding of the interactions of materials with the plasma chemistry and detailed knowledge of coating technology. Systematic investigations have identified the important reaction mechanisms, determined defect release and transport modes, and characterized the effects of numerous etch processes. The accompanying materials engineering involves extensive understanding of material behavior and requirements and advanced deposition techniques. It also requires identifying new metrology techniques for future device nodes.

CONCLUSION

Chamber material selection and coating technology development are crucial to ensure plasma compatibility, erosion resistance, and microstructural stability to meet the most stringent wafer-level defect requirements for advanced node applications in the semiconductor industry. New material developed for plasma coating application has successfully demonstrated benchmark low defectivity.

Figure 6

Material Interaction With Chemistry/Plasma

- Plasma Chemistry Reaction Mechanism
- Process Window Characterization
- Etch By-Product Management
- Hardware Configuration Sensitivity
- Defect Transport Mechanism

Material and Coating Technology

- Advanced Materials Development—Formulation and Grain Boundary Engineering
- Material Processing and Fabrication— Microstructure and Surface Morphology Control
- Metrology and Materials Characterization
- Advanced Coating Process Technology Development
- Advanced Coating Process Control Methodology—In-Situ Monitoring
- Wet Clean Chemistry, Process, and Vendor Development—End Point Driven

Figure 6. Key components of materials development program.

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PROCESS SYSTEMS USED IN STUDY

Applied Centura® AdvantEdge™ Mesa™ Etch
Applied Producer® Etch

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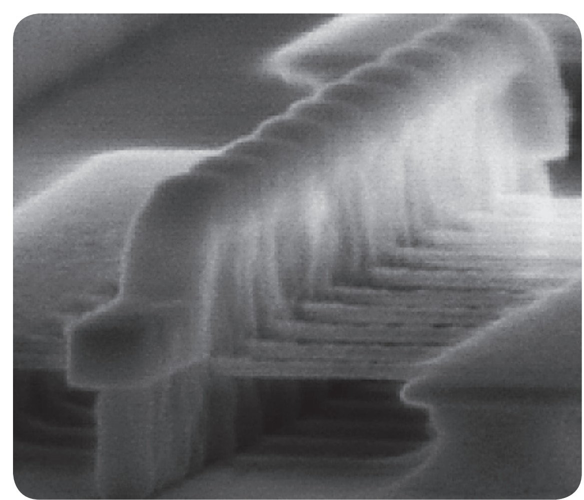
Characterizing GAAS Nanowire Buckling

by Height Map Reconstruction

KEYWORDS
Buckling
GAASiNW
Height Map
Metrology
Nanowire
Transistor



Silicon nanowire (SiNW) devices, particularly the gate-all-around (GAA) CMOS architecture, demonstrate superior gate control and immunity to short-channel effects. This allows gate length to be reduced, positioning GAASiNW devices as a suitable candidate for future scaled technologies. Thin suspended SiNWs tend to buckle between source and drain, degrading device performance. Characterizing buckling is a significant challenge for CDSEM metrology. A new height map reconstruction technique has been developed, making it possible to obtain the buckling vector gradient along the wire in three dimensions.

As the industry transitions from exclusively planar transistors, numerous variations of 3D architectures are being investigated in anticipation of lowering power consumption and boosting performance of future-generation devices. Presently, the strongest industry focus is on FinFET transistors for logic and vertical NAND transistors for memory. However, research is also aimed at fabricating, characterizing, and testing more futuristic solutions, such as GAA field effect transistors (FETs). These are similar to FinFETs, except that the gate material entirely surrounds the channel region. GAASiNWs are among the advanced designs currently being researched. Their design poses new challenges in fabrication and procedures such as metrology.

GAASiNW FET fabrication requires suspending the SiNWs that serve as the device channel so that the gate stack (typically high-κ and metal) can be deposited around the SiNW channel. Thin suspended SiNWs are prone to buckling. Variations in NW dimensions can significantly degrade the charge transport characteristics of the device.

Measuring this buckling using standard metrology poses a considerable challenge: SiNWs are typically 3-10nm in diameter and the buckling (deviation from straight line) is on the same scale. Furthermore, buckling is a 3D phenomenon; in-line CDSEM metrology tools typically measure feature size in the X-Y plane. Measuring SiNW buckling in three dimensions requires the CDSEM to quantify dimension in the Z-axis as well. To make this possible, thereby enabling buckling characterization, we developed a height map reconstruction technique.

BUCKLING IN X, Y DIMENSIONS

Buckling in suspended SiNWs was measured as a function of wire diameter (3-12nm) and length (130, 180, 230, and 280nm). The wires were clamped on both ends to silicon pads.[1] Figure 1 clearly shows the dependence of buckling on the SiNW's width and length.

Results suggest that the onset of buckling in the investigated SiNWs can be estimated using Euler's theory. Transmission electron microscope (TEM) images confirm the estimation of a cylindrical shape, but top-view measurements can measure variations of the SiNW diameter only in the horizontal plane. In addition, the SiNW is covered with native oxide. These factors were not taken into account in our calculations. The origin of the force that induces buckling could be the silicon-on-insulator (SOI)/buried oxide interface, although it could also be partially induced by the scanning electron beam.

HEIGHT MAP RECONSTRUCTION

Height map reconstruction employs a system of side detectors on the SEM that capture the secondary electrons (SE) generated on a specimen in response to primary electron beams (Figure 2). SE distribution between the detectors depends on the local tilt of the specimen, which in turn defines the gradient of the height map.

The following basic assumptions underlie this method:

- Known dependency on tilt angle of relative SE yield $y = y(cos\varphi)$
- Lambertian angular distribution of SE velocity vectors
- Known distribution of SE energy around (unknown) central energy
- SE capture by split detectors or top detector depends mainly on the lateral component of its initial velocity

The signal of each detector depends largely on topography (local slope and azimuth), material, working point, and gain of electronic path. The overall signal of a detector can be stated as

$$E_i = k_i \cdot Y_0 \cdot R_i(\bar{g})$$

where E_i is the signal of the i-th detector

k_i is the gain of the SEM's electronic path

Y_0 is the yield of the horizontal surface of the specimen at the given working point

R_i is the relative signal of the i-th detector, depending only on topography

$\bar{g}$ is a vector of topographical gradient

We suppose that capturing a SE by split detectors or top detector depends mainly on the lateral component of its initial velocity. This means a probability $\Phi(\phi)$ that an SE will be captured by some split detector as a function of the elevation of its velocity vector. Which of two split detectors captures the SE depends only on the azimuth of its velocity vector. Our analysis shows that under such assumptions

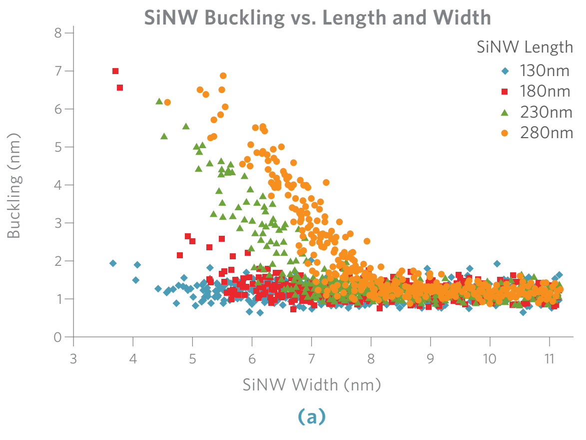
$$R_i = y(\cos\varphi) \cdot \eta_i(\varphi, \theta)$$

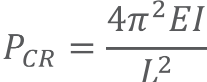
where η_i is the capture rate of the the i-th detector

φ is the elevation of vector of topographical gradient

θ is the azimuth of vector of topographical gradient

Figure 1





Critical Load Calculations (N)

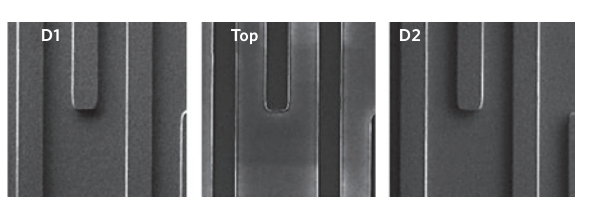
SiNW Length (nm)	Measured SiNW Diameter (nm) 5.2	6.1	6.9	7.6
130	1.42E-0.8	2.69E-0.8	4.41E-0.8	6.49E-0.8
180	7.42E-0.9	1.41E-0.8	2.30E-0.8	3.39E-0.8
230	4.55E-0.9	8.61E-0.9	1.41E-0.8	2.07E-0.8
280	3.07E-0.9	5.81E-0.9	9.51E-0.9	1.40E-0.8

(b)

Figure 1. (a) SiNW CDSEM buckling measurement as a function of the wire diameter for various wire lengths. Buckling is measured from fitted line to the SiNW maxima. **(b)** Results of critical load calculations.

Figure 2

Detector SEM Images



Height Map

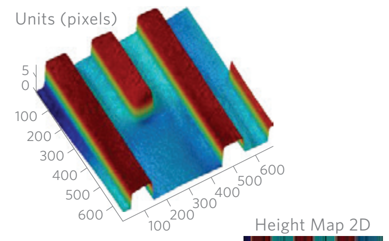


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Figure 2. Height map reconstruction synthesizes data from several detectors to produce a 3D representation of the features under examination.

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Nanowire Buckling

A detector's capture rate can be obtained by integrating angular and energy distributions of SEs within limits that guarantee them reaching that detector. Evaluating the above assumptions leads to the following formula for η_i:

$$\eta_i = \int_0^{\frac{\pi}{2}} \Phi(\phi) \int_{\psi_i}^{\psi_i+\pi} L(\phi,\psi,\varphi,\theta)d\psi \cdot d\phi$$

where $L(\phi,\psi,\varphi,\theta)$ is Lambertian from the surface with vector of topographical gradient with elevation φ and azimuth θ
ψ_i is azimuthal position of the i-th detector.

Elevation angle is limited from below by 0, as almost all SEs directed down will be absorbed by the wafer surface.

Further analysis reveals that η_i can be presented as

$$\eta_1 = G(cos\varphi)\cdot\left(\frac{1}{2} + F(cos\varphi)\cdot cos(\theta-\psi_1)\right)$$

$$\eta_2 = G(cos\varphi)\cdot\left(\frac{1}{2} - F(cos\varphi)\cdot cos(\theta-\psi_1)\right)$$

where F and G are monotonic functions, depending on working point.

Therefore,

$$R_1 + R_2 = y(cos\varphi)\cdot G(cos\varphi) \equiv S(cos\varphi)$$

where S is a monotonic function, depending on working point.

$$\frac{R_1}{R_1+R_2} = \frac{1}{2} + F(cos\varphi)\cdot cos(\theta-\psi_1)$$

Extracting local elevation of the surface:

$$cos\varphi = S^{-1}(R_1+R_2)$$

where S^{-1} can be pre-computed for each working point.

Local azimuth of the surface can be derived from the above equations.

Using the equation below as a starting point, R_i can be extracted from available signals of detector E_i.

$$E_i = k_i\cdot Y_0\cdot R_i(\bar{g})$$

The irrelevant factor $k_i\cdot Y_0$ can be eliminated using signals E_{iH} from flat horizontal areas with zero gradients. For such areas $cos\varphi = 1$, and

$$y(1)=1,\ \ F(1)=0,\ \ \eta_i=\eta_H=\frac{G(1)}{2}$$

which yields

$$E_{iH} = k_i\cdot Y_0\frac{G(1)}{2}$$

and

$$R_i = \frac{E_i}{E_{iH}}\cdot\frac{G(1)}{2}$$

Thus, by using the horizontal plane as the reference, irrelevant factors of the SEM images are eliminated and a vector map of estimated topographical gradients of the wafer can be obtained.

The next problem is restoring the height map from gradients. Here, the problem is that the components of gradient are obtained from different sources (detectors and electronic paths) each one with its own noise and imperfections. Therefore, one cannot be guaranteed that the obtained vector map is integrable (i.e., there exists a scalar map, whose gradients are identical to the given vector map). The solution is to use a scalar map, whose gradient matches the given vector map as closely as possible. This work followed the approach used by Frankot and Chellappa[2] in which the height map is constructed from the following equation:

$$F_H(\omega) = \frac{-j\omega_x F_{gx} - j\omega_y F_{gy}}{\omega_x^2 - \omega_y^2}$$

where F_{gx}, F_{gy} are Fourier transforms of corresponding x- and y- components of gradient
F_H is the Fourier transform of the height map

From the specimen height map, measurement algorithms for different 3D parameters, e.g., curvature of the nanowire, its roughness, etc., were built as detailed below.

SAMPLE PLAN

SiNW samples were fabricated using SOI wafers. Fabrication included lithography, followed by reactive ion etching to define the wires, etching of the buried oxide to suspend the wires, and additional thinning and smoothing of the wires by H_2 annealing and oxidation.[1] The width of the samples varied from 3 to 12nm; length was 280nm.

To improve measurement accuracy, SEM-TEM correlation was performed by measuring SiNWs that were fabricated on wafers from the same batch. The results confirmed CDSEM capability to accurately measure SiNWs approximately 5nm in diameter (Figure 3).

BUCKLING ANALYSIS

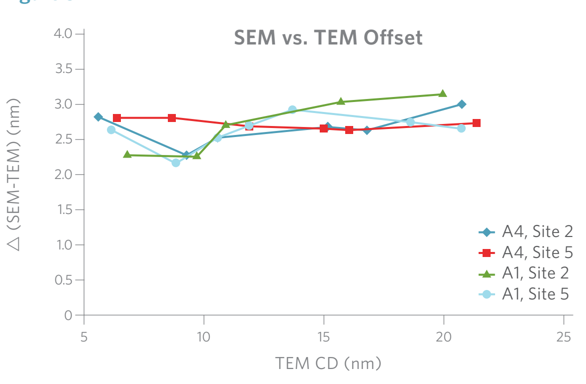
Figure 4a compares the signal obtained from two side detectors viewing the same structure. The variance presented shows a clear shift caused by the detector's perspective, confirming that the height map can be reconstructed for these structures (Figure 4b).

Height map reconstruction measurements demonstrate height variation along the SiNW. To quantify the results, a statistically significant number of wires were measured.

Results indicated that the SiNWs sagged mostly along the Z-axis. Along the X-axis, the distribution was symmetrical on both sides. Using X, Y, and Z per pixel, it was possible to calculate how the wire buckled in three dimensions.

Comparing the buckling gradient maxima module vs. SiNW CD (Figure 5) shows that buckling lessens as the wires thicken. Plotting the buckling vector maxima in the X direction vs. CD shows that buckling increases as CD decreases. These results correspond with the two-dimensional buckling measurements.

Figure 3



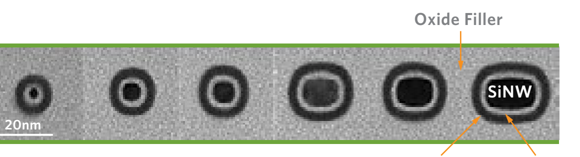


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Figure 3. Correlation between CDSEM and cross-section TEM measuring the same SiNWs.

Figure 4

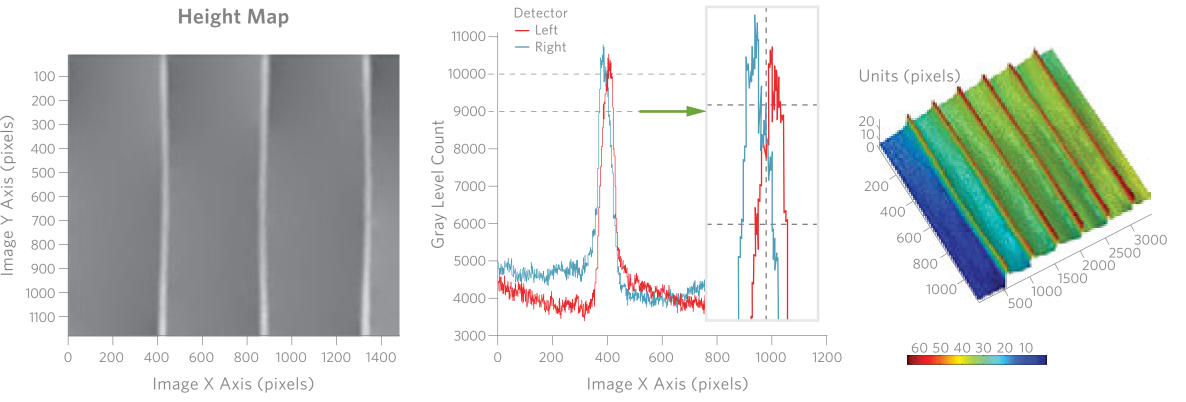

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Figure 4. (a) Signal offset between the two detectors viewing the same SiNWs. **(b)** Height map reconstruction of these structures.

Figure 5

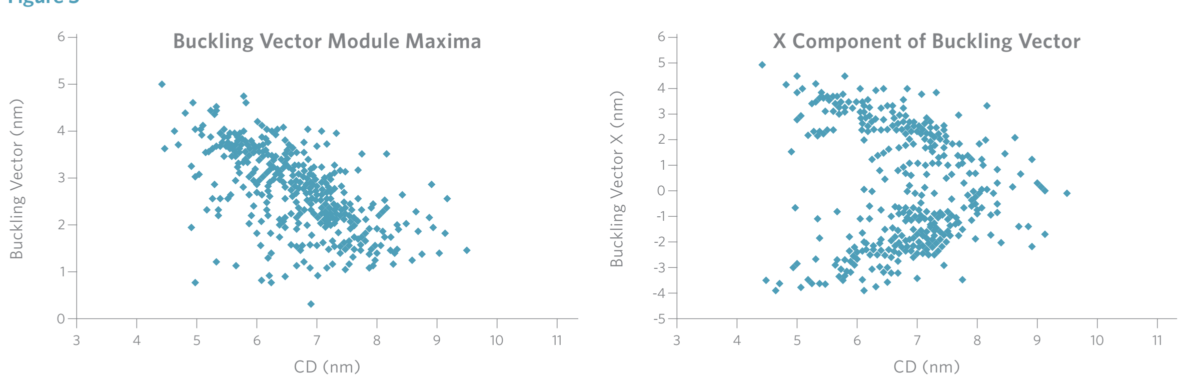

Figure 5. Buckling vector characteristics vs. SiNW CD.

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However, some unexpected results were obtained. One would assume that SiNWs with circular cross-sections would buckle equally in all directions. But measurements indicated that the thinnest SiNWs (CD <5nm) tended to buckle mainly to the left or right, while thicker SiNWs sagged downwards more than the thin wires and buckled at various angles (Figure 6).

The TEM images in Figure 6 suggest the root cause of the different buckling behaviors. SiNWs with diameters less than 5nm display an oval cross-section, with the longer axis oriented in the Z direction. Such wires have a lower critical load threshold for buckling in the X-Y direction than in the Z direction, which agreed with our observations.

To verify repeatability of the results, the sample plan was measured twice and the first run compared with the second. Buckling measurements were repeatable for both X-Y and Z. But the correlation was not perfect; the deviance possibly derives from carbonization added to the wires' surfaces as they were scanned.

Figure 6

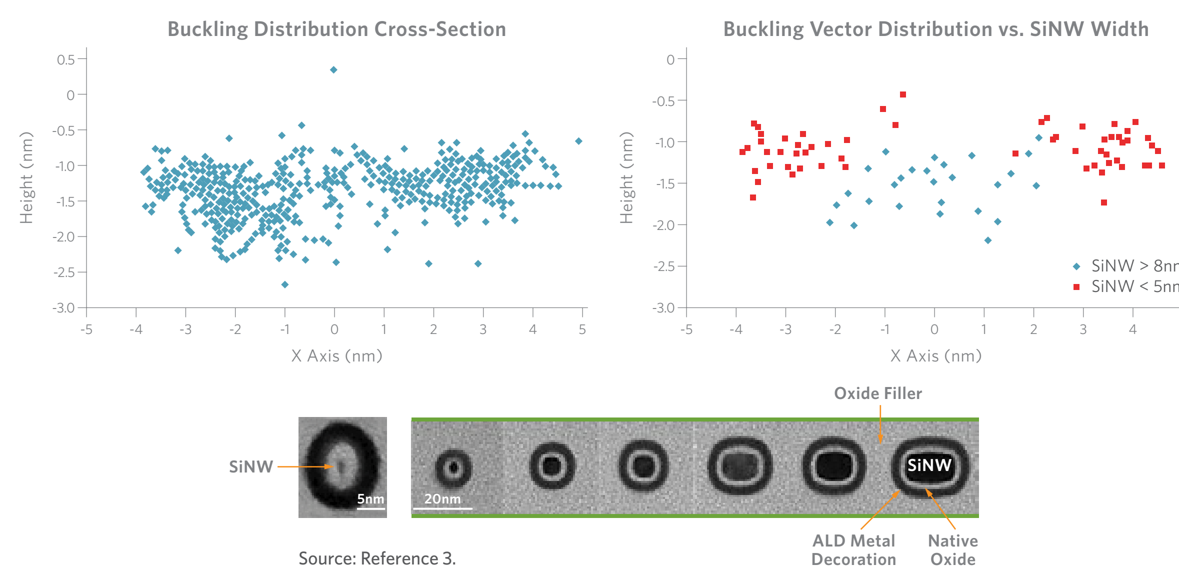

Figure 6. Buckling vector Z (height) vs. X (horizontal) reveals clear differences among SiNWs. TEM images suggest different cross-sectional shape as the likely root cause.[3]

Figure 7

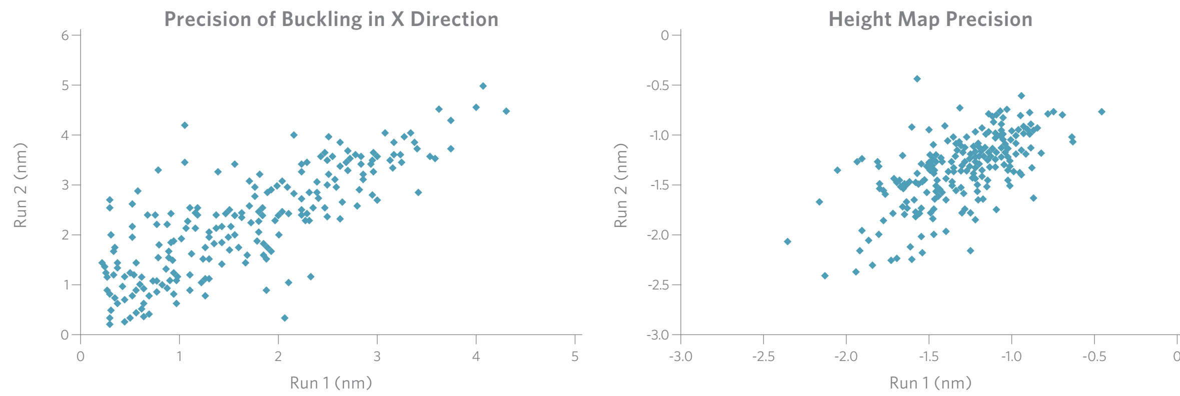

Figure 7. Results from two measurement runs correlated reasonably well.

CONCLUSION

This study was the first 3D characterization of buckling in suspended SiNWs using a height map reconstruction technique. It also presented a method of calculating and predicting the onset of buckling in suspended SiNWs of different lengths and widths. Results demonstrated the capability of measuring SiNWs less than 5nm in diameter with sensitivity to sub-nanometer variations in all three dimensions.

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