# A SIGNAL ACQUISITION INTERFACE FOR A DSP BOARD

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by

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## ABSTRACT

*Many applications involving DSP require handling of multiple input/output analog signals. Sampling causes aliasing at the input and spectrum repetition at the output. Therefore, anti-aliasing filter for inputs before A/D converter, and smoothing filter for outputs after D/A converter are required. Further the choice of sampling frequency is often application specific.*

*The aim of the project is to develop a system which would extend the I/O handling of a PC bus-based DSP board having single analog I/O channel, with appropriate signal conditioning of input and output channels, for variable sampling rates.*

*An I/O expansion unit for the DSP board PCL-DSP25, based on TMS 320C25 DSP processor, has been developed which enhances the analog I/O handling of the DSP board from single analog I/O channel to four analog I/O channels.*

*An eighth order elliptic low-pass filter and Bessel low-pass filter have been implemented. Both the filters can serve as anti-aliasing filter for the input signals and smoothing filter for the output signals. Also a second order elliptic notch filter has been implemented to reduce any possible power-line interference at the input. The filters are implemented using switched capacitor circuits to achieve clock-controlled cut-off frequency. This feature makes the filters useful for variable sampling rates. A programmable timer/counter has been interfaced with the DSP board to make the cut-off frequency of the filters programmable by the DSP board.*

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CONTENTS

## LIST OF ABBREVIATIONS

| | | |
|---|---|---|
| DSP | – | Digital signal processing |
| DAS | – | Data acquisition system |
| ADC | – | Analog-to-digital converter |
| DAC | – | Digital-to-analog converter |
| S/H | – | Sample-and-hold |
| SCU | – | Signal conditioning unit |
| I/O | – | Input / output |
| I/P | – | Input |
| O/P | – | Output |
| PA | – | Port address |
| AR | – | Auxiliary register |
| DMA | – | data memory address |

## LIST OF NOTATIONS USED

| | | |
|---|---|---|
| (L) | – | Contents of register/memory address 'L' |
| A -> B | – | 'A' Is assigned to 'B' |
| 0x data | – | Data in hex format (in 'C' code) |
| > data | – | Data in hex format (in TMS 320C25 assembly code) |
| 'X' | – | Don't care digit in the binary data |
| SIGNAL* | – | Low acting signal (*e.g.* W* means $\overline{W}$ ) |

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# CHAPTER 1

# INTRODUCTION

## 1.1 OVERVIEW

Digital signal processing (DSP) applications are growing rapidly in speech processing, image processing, adaptive filtering, control systems, bio-signal processing, *etc.* [1 ]. Real time processing can be carried out either by a dedicated hardware or a digital signal processor. In a digital signal processor chip, the architecture and instruction set are designed for high speed arithmetic calculations which increases the execution speed of the DSP algorithms [1 ].

There are several PC bus compatible DSP boards available. Such a DSP board typically includes a DSP chip, program and data memory, an analog I/O interface, and a programmable timer/counter (to run interrupt based programs); and it can be inserted in one of the PC expansion slots. For many applications, the intensive calculations are carried out by the DSP board, while the user interfaces, such as, graphics, mass data storage, etc. are carried out on the PC.

The analog I/O interface of the DSP board typically consists of an ADC, a DAC, and a sample/hold, and can handle one analog input-output at a time. However, many of the typical DSP applications such as adaptive noise cancellation in speech processing, adaptive filtering, multi-channel bio-signal processing, require multiple analog I/O handling.

The analog inputs are sampled and digitized and the processing is carried out on these sampled data, the sampling frequency being set by the user program. Sampling causes aliasing effect which is to be reduced by the low-pass filtering of the analog inputs [2, 3 , 4 , 5 , 6 ]. Also the output is discrete data which causes frequency spectrum repetition. Hence a low-pass filter, called as smoothing filter, is required to reconstruct

the analog output [2, 4 , 5 , 6 ].

DSP applications involve handling of input signals of a very few Hz (bio-signal applications) to kHz range (speech applications) and therefore, different applications require different sampling rates. A low-pass filter with programmable cutoff frequency would serve as anti-aliasing filter or smoothing filter for different applications in the programmable range of the filter.

## 1.2 PROJECT OBJECTIVE

The objective of the project is to enhance the I/O handling of a PC bus compatible DSP board, with a single analog I/O channel.

A signal acquisition interface has been developed for such a DSP board to enhance its I/O handling from single I/O to multiple I/O with appropriate signal conditioning for each input-output channel. The I/O expansion is done by I/O expansion unit and the conditioning of the I/O channels by signal conditioning unit.

The design of I/O expansion unit depends on the available DSP board and the DSP processor on which the DSP board is based. The design of the I/O expansion unit should be such that no hardware modifications are required to be done on the DSP board. Also the design should be easily adaptable to other DSP boards with minor modifications. The I/O expansion unit is developed for Dynalog MicroSystem DSP board PCL - DSP25 (based on TMS 320C25 processor from Texas Instruments) which enhances the I/O handling of this DSP board from single analog I/O to four analog I/O.

The signal conditioning unit (SCU) includes an anti-aliasing filter for each input channel so that the need for the prefiltering by the user can be eliminated. It also includes a smoothing filter for each output channel. Both the anti-aliasing and smoothing filter are implemented with such response characteristics that they meet the requirements for most applications.

To make the SCU useful for different applications over a wide range of frequencies, both the anti-aliasing and the smoothing filters are designed to have programmable cutoff frequency, the cutoff frequency being programmable by the DSP board. The programmable cut-off frequency filter is implemented using switched capacitor (SC) filter [ ? ] in which clock input controls the cut-off frequency. For this purpose a programmable timer/counter is interfaced with the DSP board which generates the DSP programmable clock which is applied as the input to the switched capacitor filters. The programmable timer/counter interface with the DSP board is implemented on the I/O expansion unit.

To demonstrate the multiple I/O handling of the DSP board with proper signal conditioning of the I/O channels, a four-channel band-pass filter, has been implemented.

## 1.3 DISSERTATION ORGANIZATION

Chapter 2 provides an overview of the system. A brief review of the DSP processor TMS 320C25 and the DSP board PCL - DSP 25 is presented in this chapter. Each of the system block viz., signal conditioning unit and I/O expansion unit, is then discussed.

Chapter 3 discusses the signal conditioning unit.The chapter discusses the design and implementation of the filter which can serve as both anti-aliasing and smoothing filter. The filters are realized using biquad realization technique and are implemented using switched capacitor filters to achieve programmable cut-off frequency. This chapter presents a study of biquad realization with state variable feedback followed by the working of switched capacitor filter in brief. Then the design of the filter with variable cut-off frequency is discussed. The chapter concludes with tuning and testing of the filters.

Chapter 4 discusses the I/O expansion unit. The chapter provides a review of different schemes for I/O expansion,

selection of a particular scheme, and the design and implementation of this scheme as well as the interface of a timer with the DSP board for generation of programmable clock which controls the the cut-off frequency of the filters.

Chapter 5 discusses some applications of the data acquisition system developed for the DSP board. A four-channel band-pass filter application is first discussed. A cross-correlator technique for system impulse response evaluation, can also be realized using the system developed.

Chapter 6 presents summary of the work done. The achieved specifications of each individual system unit viz., signal conditioning unit and I/O expansion unit, are listed in this chapter.

# CHAPTER 2

# SYSTEM OVERVIEW

## 2.1 INTRODUCTION

A signal acquisition interface has been developed for a PC add-on DSP board. The DSP board has one analog input and one analog output channel. The system is developed to enhance its I/O handling from single I/O channel to four I/O channels with proper signal conditioning for each input-output channel. The signal acquisition interface consists of an I/O expansion unit and a signal conditioning unit, as shown in Fig. 2.1.

The I/O expansion unit (EU) consists of a 4-to-1 multiplexer for analog inputs and 1-to-4 demultiplexer for analog output. The output of the multiplexer is applied as the D/A input to the DSP board. The output from the DSP board is demultiplexed into four analog outputs.

The signal conditioning unit (SCU) consists of an anti-aliasing filter for each analog input, and a smoothing filter for each analog output. The outputs from the anti-aliasing filters are applied as the inputs to the multiplexer and the demultiplexed outputs are filtered by the smoothing filters.

As the sampling rate varies depending on the application, the anti-aliasing and the smoothing filters are designed to have programmable cut-off frequency. These filters have been realized using switched capacitor circuits, and their cut-off frequency can be controlled by the input clock frequency. A programmable clock generator unit generates three programmable clock outputs which can be used for controlling the cut-off frequencies.

The I/O expansion unit is developed for a DSP board PCL-DSP25 from Dynalog MicroSystems. The board is based on the DSP processor TMS 320C25 from Texas Instruments. The chapter first reviews the DSP board PCL - DSP25 and the DSP processor TMS 320C25. Each unit of the system viz. signal conditioning unit and I/O expansion unit

is then reviewed in brief.

## 2.2 DSP BOARD AND PROCESSOR

PCL DSP25, Digital Signal Processor PC plug-in card, from Dynalog MicroSystems, is based on TMS 320C25 DSP processor [1, 2]. This DSP processor has sixteen software ports for interface to external hardware. On the DSP board PCL-DSP25, four of the sixteen available DSP software ports are used by on-board peripherals as shown in Table 2.1. The remaining software ports can be used for I/O expansion and programmable clock generation.

TMS 320C25 is third processor in the TMS320 series, the former two being TMS 32010 and TMS 32020. It is a 16-bit fixed point, CMOS DSP chip, running at 40 MHz CPU clock, with 100 nsec instruction cycle time, and is based on Harvard type architecture [8].

The functional block diagram of TMS 320C25 is shown in Fig. 2.2. The main blocks are 32-bit ALU/Accumulator, 544-word programmable on-chip data RAM, 4K-word programmable on-chip program ROM, 128-K total program/data memory space, 16 X 16-bit parallel multiplier with 32-bit product register, eight auxiliary register with dedicated arithmetic unit and an on-chip timer.

The PCL DSP25 board block diagram is shown in Fig. 2.3. The main blocks are DSP processor TMS 320C25, program and data memory, analog I/O interface unit and IBM PC bus interface unit [9]. The analog I/O unit interface consists of an ADC and a DAC. Hence it can handle only one input-output channel. The analog I/O is accessed either by port 2 or port 3. Further, the board has a 50 pin connector "DSPLINK" for digital I/O expansion (as described in Appendix B).

The analog I/O interface schematic is shown in Fig. 2.4. Software ports 2 and 3 are assigned for analog I/O. The input is sampled and digitized. Either The external clock or the on-board timer can be used as the sampling clock, as selected by the hardware link. The ADC starts the conversion process after

receiving a start-of-conversion pulse, which is provided by the sampling source, or by reading port 2 or port 3. On the end of conversion, the data at the output of ADC is latched. Reading the port 2 or 3 puts this data on the data bus of the DSP processor. Similarly the timing of DAC output can be controlled by sampling source or writing to port 2 or 3.

Software support available for the DSP board DSP-PCL25 includes 'C' interface library developed using Microsoft Language tools of Microsoft C compiler (version 5.0) and the assembler for TMS320C25 assembly language.

To expand I/O, we want to decode read and write of the external ports. Appendix B provides a detailed review of the IN/OUT instructions. From the review of the I/O instructions, the minimum signal set required for I/O expansion is as shown in Table 2.2, and all these signals are available as part of I/O expansion connector DSPLINK.

## 2.3 SIGNAL CONDITIONING UNIT

Signal conditioning unit provides eight low-pass filters that can be used as anti-aliasing filters for analog inputs or as smoothing filters for analog outputs. Further, the unit provides four notch filters for rejecting possible power line interference in the analog inputs. Here, first the need for these filters with variable cut-off is established, and thereafter the filter specifications are worked out.

### 2.3.1 Anti-aliasing and smoothing filters

The analog inputs are sampled and digitized by the DSP board. The condition to recover the original signal from its samples is given by Nyquist criterion [3, 4, 5, 6, 10] which states that,

A base band signal, band limited to $B$ Hz can be exactly reconstructed from its samples when it is periodically sampled at a sampling frequency $f_s \geq 2B$.

A low-pass filter with cut-off frequency of B Hz can reconstruct the original signal by interpolation if the sampling frequency is higher than 2B. This filter is known as smoothing filter.

If the signal has frequency components above $f_s/2$, the shifted frequency spectra overlap and the low frequency component will be added to high frequency component close to $f_s/2$. This undesired components are called aliasing noise and the effect is known as *aliasing*. The effect can be reduced by low-pass filtering, prior to sampling and quantization of the input signal. This filter is called an anti-aliasing filter.

The rate at which the signal is sampled determines the speed of processing and the storage requirements. Hence it is desirable to use the lowest possible sampling rate, acceptable for the given application. If the signal frequency of interest extends up to $B$, then we can use a low-pass filter to eliminate the frequency components above this. However, physically realizable filter has finite transition band between pass-band and stop-band. The pass-band edge ($f_p$) of the filter should be $f_p > B$. If the edge of the stop-band is $f_a$, we can select the sampling rate $f_s > 2f_a$.

The maximum frequency to be retained is application specific. Hence to make the signal conditioning unit useful for a wide range of applications, the anti-aliasing filter and the smoothing filter should have programmable cut-off frequency.

### 2.3.2 Notch filter

For some applications, it may be required to reduce the power-line interference. With the DSP board, the signals are discretized and then processed. Hence the filtering of the input signal can be done digitally. However, due to strong interference waveform at the input of A/D converter, most of its input dynamic range may get wasted. The resolution with the A/D converter can be improved, if the signal is first filtered by a hardware notch filter and then sampled.

To retain the maximum possible signal information in the band around the notch frequency, a notch filter with a narrow bandwidth is required. Since the power-line frequency may vary over a narrow range, it is required that the notch filter with variable notch frequency is required. Such a filter may be used as a power-line tracking filter. A circuit can be developed which tracks the power-line frequency and generates a clock of frequency 100 times this frequency. The clock input which controls the notch frequency may be derived from this power-line tracking circuit.

### 2.3.3 Filter Specifications

Ideal low-pass filter has flat magnitude response in the pass-band, infinite attenuation in the stop-band, and immediate transition from pass-band to stop-band, and a linear phase response in the pass-band. Physically realizable filter has typical magnitude response as shown in Fig. 2.5(a) [11]. The selection of pass-band edge $f_p$ depends on the application. Over the pass-band the filter response exhibits some variation in the pass-band gain, and ratio of maximum gain to minimum is known as ripple in pass-band gain $A_p$ generally specified in dB. Also the attenuation in the stop-band varies with frequency. We generally refer to some minimum attenuation $A_{min}$ in the stop-band. Further, there is a finite transition band between the pass-band and the stop-band, and we define the transition ratio $\Omega_s$ as the ratio of the stop-band edge $f_a$ to pass-band edge $f_p$.

For a particular application, first the filter parameters such as pass-band edge $f_p$, maximum allowable ripple in the pass-band $A_p$, minimum stop-band attenuation $A_{min}$, and transition ratio $\Omega_s$ are decided. Then the order of the filter required for different standard filter functions is calculated, followed by selection of one of the filter function. The transfer function of the selected filter function for the order obtained is then evaluated. Finally the transfer function is implemented using physical devices.

The application we are interested in is designing an anti-aliasing filter. Since we want the cut-off frequency of the filter as variable, pass-band edge $f_p$ is kept variable. So we now need to decide upon maximum allowable pass-band ripple $A_p$, minimum stop-band attenuation $A_{min}$, and transition ratio $\Omega_s$. Specifications for the anti-aliasing filter depend on the resolution of the quantization system (A/D converter) which follows the anti-aliasing filter and the noise (outside signal band) present at the signal input [12].

The resolution of the quantization system, called as quantization step, depends on the number of quantization bits. Since the change in signal level less than the quantization step can not be detected by the A/D converter. Hence the permissible change in the signal amplitude *i.e.* the maximum allowable gain variation, in the pass-band $A_p$ should be half of the quantization step or less and is given as (Appendix A)

$$A_p \text{ (dB)} \leq 20 \log (1 + 2\delta)$$

where,

$$\delta \leq 1/ (2^n - 1)$$

The minimum attenuation in the stop-band depends on the number of quantization bits as well as signal-to-noise ratio (SNR) at the filter input due to noise outside the signal band. The filter should reduce the noise in the stop-band to such a level which is lower than the quantization noise. For number of quantization bits $n$ and SNR of $\rho$ dB, the minimum attenuation required in the stop-band is

$$A_{min} \text{ (dB)} \geq 6n - \rho - 7.26$$

The selection of transition ratio $\Omega_s$ depends upon the application.

The DSP processor TMS 320C25 is a 16 bit processor and the on-board ADC used is a 16-bit ADC. However since the DSP board is used as a PC plug-in card, it has been empirically found that the

maximum resolution achievable is 12-bits due to unavoidable digital noise. Also for most of the applications the resolution up to 10-bits would suffice. Hence filter specifications are calculated using $n$ = 10. For $n$ = 10, $Ap$ was calculated as 0.01 dB (Appendix A). However, such a low value of $A_p$ is physically unrealizable, and hence, $A_p$ was chosen as 0.1 dB, which is maximum allowable pass-band gain variation for $n$ = 7. The signal-to-noise ratio for the input signal is taken as 20 dB. For $n$ = 10, and SNR of 20 dB, $A_{min}$ was calculated as 32.74 dB (Appendix A). $A_{min}$ has been selected as 40 dB which is higher than the required value. To reduce the sampling rate required, a sharp transition from the pass-band to stop-band is desired. For this purpose, we have selected the ratio of stop band edge to pass band edge $\Omega_s$ as, $\Omega_s = f_a/f_p$ = 1.1. Thus the filter specifications are selected as, $A_p \leq 0.1$ dB, $A_{min} \geq 40$ dB, and $\Omega_s$ = 1.1.

Different types of standard filter functions are available, such as, Butterworth filter, Chebyshev filter, elliptic filter, and Bessel filter which are discussed in brief in section 3.2. The minimum filter order required for Butterworth filter, Chebyshev filter and elliptic filter was calculated as 137, 12, 7 respectively (Appendix A). The order required is least for the elliptic filter and hence it is decided to implement an elliptic filter. For the reasons explained later, instead of a seventh order elliptic filter, it has been decided to implement an eighth order elliptic filter. The calculated magnitude and phase response for the elliptic filter of order 8, is shown in the Fig. 2.6. As seen from the figure, the magnitude response satisfies our specifications.

For some applications, where the wave shape of the signal is important, it becomes necessary to have a linear phase up to the pass-band edge [11]. However the phase response with the elliptic filter is highly nonlinear. The Bessel filter provides a good approximation to linear phase response. But with a Bessel filter the magnitude specifications listed above and the linear phase,

both can not be achieved simultaneously, for relatively sharp $\Omega_s$ = 1.1. Hence the specifications for magnitude response are relaxed to the maximum allowable pass-band ripple $A_p$ = 1 dB and transition ratio $\Omega_s$ = 10.

The calculated magnitude and phase response for an eighth order Bessel filter is as shown in Fig. 2.7. From the figure, it can be seen that the phase relationship between input and output is linear up to eight times the 3-dB cut-off frequency. Also the maximum pass-band attenuation is less than 0.9 dB.

Similar specifications can be formulated for the smoothing filter. Hence same filter can serve either as anti-aliasing or smoothing filter. Both the elliptic and Bessel filters can be used as anti-aliasing filter at the input and smoothing filter at the output depending upon the requirements.

Typical magnitude response of a notch filter is as shown in Fig. 2.5(b) [2]. The specifications for the notch filter were selected as $A_p \leq 1$ dB, $A_{min} \geq 24$ dB, pass-band bandwidth with the notch frequency of 50 Hz as 5 Hz, and stop-band bandwidth as 1 Hz. This gives normalized pass-band bandwidth required as 0.1, and normalized stop-band bandwidth as 0.02. The order of the filter required to satisfy the above specifications, is found to be least for the elliptic type notch filter. A second order elliptic notch filter satisfies the specifications. The calculated magnitude and phase response for this filter are as shown in Fig. 2.8. As seen from the figure, the magnitude response satisfies the requirements and hence it is decided to implement a second order elliptic notch filter.

The signal conditioning unit which consists of low-pass elliptic filter, low-pass bessel filter, and an elliptic notch filter, is discussed further in Chapter 3.

## 2.4 I/O EXPANSION UNIT

The DSP board has single analog I/O. The function of the I/O expansion unit is to enhance the I/O handling of this board. A

programmable clock generator has also been implemented on the I/O expansion unit board in order to provide variable clock frequency for controlling the filter cut-off frequency in the signal conditioning unit. Interfacing the I/O expansion and the programmable clock, to the DSP board is through the software ports of the DSP board.

The unit basically consists of a multiplexer for analog inputs and a demultiplexer for analog output. For speech and audio applications, the sampling rate required for each channel is 10 kSa/s. The maximum permissible sampling rate is decided primarily by the ADC conversion time. The on-board ADC can be configured for either 16, 14, or 12 bit conversion, with conversion times of 17, 15, and 13 $\mu$sec respectively. Hence the maximum sampling rate with one analog I/O is in the range of 60-75 kSa/s. With I/O expansion to four I/O channels, the maximum sampling rate for each channel would be in the range of 15-19 kSa/s. Even after accounting for the multiplexer response time, the maximum sampling rate for each of the four channels for 16-bit operation is greater than 10 kSa/s.

The programmable cut-off elliptic low-pass, Bessel low-pass, and elliptic notch filters are realized using SCF IC MF10 (from National Semiconductor). The cut-off frequency of the filters is controlled by clock input to the switched capacitor circuit, the cut-off frequency being 1/100 times the clock frequency. Hence to achieve programmable cut-off, we need to generate clock of frequency 100 times the cut-off frequency desired. These have been achieved by using a programmable interval timer/counter (PIC). For our application, the maximum sampling frequency would be around 10 kSa/s which restricts the maximum cut-off frequency to 5 kHz and hence the maximum clock frequency to 500 kHz. Programmable interval timer, Intel 8253 is used for programmable clock generation which can generate three independent programmable clock frequencies.

The I/O expansion unit is discussed further in Chapter 4.

Table 2.1. TMS 320C25 port assignment on the DSP board, PCL-DSP25

| Port No. | Name | Function |
|---|---|---|
| Port 0 | IBM PC Port | PC Communication Register |
| Port 1 | Interval Timer Port | 16 bit timer arranged to provide sample pulse for ADC and DAC Counter is clocked at 5 MHz. |
| Port 2 | I/O Port | ADC and DAC for I/O of a single analog channel with external clock as sampling source. |
| Port 3 | I/O Port | ADC and DAC for I/O of a single analog channel with external clock as sampling source or immediate sample clock by IN/OUT instructions. |

Table 2.2. Minimum signal set required for I/O expansion

| SIGNAL | IN/OUT | DESCRIPTION |
|---|---|---|
| D0-D15 | I/O | 16 buffered bi-directional data bus. |
| A0-A3 | O | Lower 4 bits of buffered address lines. |
| R/W | O | Line indicating direction of data transfer. |
| IOE | O | Line indicating access to any I/O port. |
| RESET | O | Reset line, same as processor reset. |
| CLK OUT | O | Integral sub multiple of DSP system clock. |
| GND | O | Signal ground and return path for Vcc. |

# CHAPTER 3

# SIGNAL CONDITIONING UNIT

## 3.1 INTRODUCTION

This chapter discusses the signal conditioning unit (SCU) consisting of anti-aliasing and smoothing filters with variable cut-off frequency. Anti-aliasing filter is required at the input before sampling, to reduce the aliasing noise which would be caused during sampling. Also, since the output is sampled data, a smoothing filter is required after D/A, to reduce the aliasing noise caused by the spectral repetition.

To achieve variable cut-off frequency, design technique of frequency response normalization is followed. Designing a filter satisfying certain specifications is essentially a problem of pole-zero placement. However the general approach is to implement the filter as one of the standard transfer functions which satisfies the required specifications with least complexity and order. A higher order filter can be implemented directly or by cascading several lower order filter sections. Generally cascading of biquad active filter sections [2, 11], is preferred, because pole-zero locations of individual section can be easily controlled by circuit components [11]. Further to achieve variable cut-off frequency, the filters are realized using switched capacitor filters (SCFs) in which the cut-off frequency can be controlled by the clock input [7, 13].

The standard filter transfer functions are Butterworth, Chebyshev, inverse Chebyshev, elliptic, and Bessel functions.They differ in the pole-zero location [11]. Butterworth filter is an all-pole network and offers maximally flat magnitude response in the pass-band. Chebyshev filter is also an all-pole network and offers a better characteristics near cut-off at the expense of ripples in the pass-band. Inverse Chebyshev is a pole-zero network which offers a sharper transition at the expense of ripples in the

stop-band. Elliptic filter is a pole-zero network which offers sharp cut-off and infinite rejection at a finite number of frequencies but at the expense of ripples in the pass-band as well as the stop-band. Bessel filter is an all-pole network which offers linear phase response with frequency, but the magnitude response is much less selective.

The specifications of the anti-aliasing filter and the smoothing filter have been listed in Chapter 2. It was decided to implement elliptic filter and Bessel filter to satisfy the requirements. Also a notch filter with programmable cut-off frequency is to be designed. This chapter first discusses the biquad realization by state variable feedback. The working of the SCF is considered in brief, followed by a review of the SCF IC MF10 (from National Semiconductor). The design of eighth order elliptic filter and eighth order Bessel filter, based on switched capacitor biquad, using normalization technique to achieve clock controlled cut-off frequency, is discussed. This is followed by the design of the notch filter. The implementation of these filters based on switched capacitor filter IC MF10 is presented. The chapter concludes with the tuning of the filters and the response characteristics obtained for both the filters.

## 3.2 BIQUAD REALIZATION BY STATE VARIABLE FEEDBACK

Transfer function of a general biquad i.e. a second order section is,

$$H(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + (\omega_0/Q)s + \omega_0^2} \qquad (3.1)$$

where, $\omega_0$ - resonant frequency

$Q$ - quality factor (frequency selectivity)

The numerator coefficients determine the transition zeros and

thus the type of the filter, LP, HP, BP, etc (Appendix A). One way of realizing the biquad form is by state variable feedback as shown in Fig. 3.1. Selecting the state variables $x_1$, $x_2$ as,

$$x_1 = v_o$$
$$x_2 = \dot{x}_1$$

we get,

$$\dot{x}_2 = -\omega_o^2 x_1 - (\omega_o/Q)x_2 + v_i$$

and therefore,

$$\ddot{v}_o = -\omega_o^2 v_o - (\omega_o/Q)\dot{v}_o + v_i$$

Hence the transfer function between $v_o$ and $v_i$ is,

$$\frac{V_o}{V_i} = \frac{1}{s^2 + (\omega_o/Q)s + \omega_o^2} \qquad (3.2)$$

By varying the gains of the feedback paths, $\omega_o/Q$ and $\omega_o^2$, we can vary the characteristic equation,

$$s^2 + (\omega_o^2/Q) + \omega_o^2 = 0,$$

and hence the roots of the characteristic equation which are the poles of the filter. The desired zeros can be incorporated in the transfer function by modifying the biquad of Fig. 3.1, by adding feed forward loops to it as shown in Fig. 3.2. By varying the gains of the feedback loops, the location of the poles can be adjusted while by varying the gains of the feed forward loops, the location of the zeros can be adjusted. One of the major advantage of the biquad form is this independent adjustment of the locations of the poles and the zeros. The transfer function between $v_o$ and $v_i$ is then,

$$H(s) = \frac{V_o}{V_i} = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + (\omega_0/Q)s + \omega_0^2} \qquad (3.3)$$

This is the general biquad form, also known as universal biquad [7]. There are special biquad sections which give different filter transfer functions depending upon the values of the numerator coefficients as shown in Table 3.1.

## 3.3 SWITCHED CAPACITOR FILTER (SCF)

Programmable cut-off frequency is a feature difficult to achieve, because the relative positions of all poles and zeros need to be altered simultaneously. One possible solution is automatic gain control of the feedback and the feed forward loops of Fig. 3.2. D/A converter can be used for such an application [14]. However to achieve the programmable cut-off frequency, the gains of the different loops have to be changed in a correlated fashion which is difficult to achieve with a DAC. A possible solution to this problem is to implement the filter with switched capacitor filter (SCF).

The motivation for the development of SC filter was provided by the difficulties in implementation of active RC filter in monolithic form due to difficulties in implementing large value capacitors and achieving accurate RC time constants [7], [15].

The working of the switched capacitor filter is illustrated in Fig. 3.3. The basic element is a switched capacitor integrator made up of a switch, a pair of capacitors (one sampling and feedback), and an op-amp. The switch, actually a pair of MOS transistors, periodically connects the sampling capacitor to input and to op amp. These two MOS transistors are driven by a non-overlapping two phase clock.

During the high state of phase $\phi_1$, capacitor $C_1$ charges to the voltage $v_i$ .

$$q_{c1} = C_1 v_i$$

During high state of phase $\phi_2$ charge $Q_{c1}$ is transferred to $C_2$. Thus during each clock period $T_c$, an amount of charge $C_1$ is extracted from the input source and supplied to the capacitor $C_2$. Hence the average current flowing between the input and virtual ground is,

$$i_{av} = C_1 v_i / T_c$$

If sampling period is sufficiently small, then the charge transfer can be thought to be continuous. Then the output voltage can be written as,

$$v_o = - \frac{1}{C_2} \int i_{av}(t)\, dt$$

$$= - \frac{C_1}{C_2 T_c} \int v_i\, dt$$

As a result the equivalent time constant for the inverting integrator is,

$$T = T_c(C_2/C_1)$$

Thus the time constant of the integrator is determined by the switching frequency and the ratio of the sampling capacitor to feedback capacitor, not by the actual value of either capacitor.

The working of the non-inverting integrator is similar, as shown in Fig. 3.4. The output voltage $v_o$ for the non-inverting integrator is obtained as,

$$v_o = \frac{C_1}{C_2 T_c} \int v_i\, dt$$

The time constant for the non-inverting integrator is $T_c(C_2/C_1)$.

Using MOS technology to implement SCF filter brings advantages of accuracy and compactness. Hence the switched capacitor ICs are implemented in the monolithic form using the MOS technology. Various switched capacitor filter ICs are commercially available, some of which are listed in Table 3.2. National

Semiconductor IC MF10 which consists of two universal biquad sections has been chosen for implementing the filter functions.

## 3.4 SWITCHED CAPACITOR FILTER IC MF10

IC MF10, from National Semiconductor provides two independent universal biquad sections [16]. The simplified block diagram of one biquad section of the chip is shown in Fig. 3.5. Each section consists of one op-amp and two non-inverting SC integrators. The chip includes capacitors and analog switches for the integrators. The integrators are applied two non-overlapping clock phases, which are derived from the external applied clock. The working of the two-integrator block has been already explained in section 3.3. All the filter outputs such as, low-pass, high-pass, band-pass, all-pass, are available at output pins of the chip. More information about the chip can be obtained from the data sheet included in Appendix D.

The input clock frequency controls the cut-off frequency. A pin $S_{AB}$ sets the clock-to-cutoff-frequency ratio as 50:1 or 100:1. The ratio 100:1 will reduce aliasing problems and hence the ratio 100:1 is selected.

The clock frequency should be in the range of 10 Hz to 1 MHz. Also the product of center frequency ($f_{\emptyset}$) and quality factor $Q$ should be less than 200 kHz.

A biquad realization to achieve different filter functions with IC MF10 is as shown in Fig. 3.6. One biquad can be implemented with one section. There are two biquads on one chip, and hence up to fourth order filter section can be realized with one chip and some external components. The transfer function between the input and output can be obtained as follows.
Let,

$$\lambda = 2\pi f_{clk.}/100$$

As shown in Fig. 3.6.,

$$V_2 = (\lambda/s)\, V_1$$

$$V_3 = (\lambda/s)\, V_2$$

$$V_1 = -\frac{R_2}{R_1} V_i - \frac{R_2}{R_3} V_2 - \frac{R_2}{R_4} V_3$$

$$V_\emptyset = -\frac{R_7}{R_5} V_1 - \frac{R_7}{R_6} V_3$$

From above relations, one can obtain the transfer functions for each of $V_1$, $V_2$, $V_3$, and $V_o$ with $V_i$.

$$H_{Hp}(s) = \frac{V_1}{V_i} = -\frac{R_2}{R_1} \frac{\lambda^2 s^2}{s^2 + (R_2/R_3)\lambda s + (R_2/R_4)\lambda^2} \qquad (3.4)$$

$$H_{Bp}(s) = \frac{V_2}{V_i} = -\frac{R_2}{R_1} \frac{\lambda s}{s^2 + (R_2/R_3)\lambda s + (R_2/R_4)\lambda^2} \qquad (3.5)$$

$$H_{Lp}(s) = \frac{V_3}{V_i} = -\frac{R_2}{R_1} \frac{1}{s^2 + (R_2/R_3)\lambda s + (R_2/R_4)\lambda^2} \qquad (3.6)$$

$$H_{No}(s) = \frac{V_o}{V_i} = \frac{R_2}{R_1} \frac{(R_7/R_5)\, s^2 + (R_7/R_6)\lambda^2}{s^2 + (R_2/R_3)\lambda s + (R_2/R_4)\lambda^2} \qquad (3.7)$$

From Eqns. 3.4, 3.5, 3.6, 3.7, it can be seen that $V_1$, $V_2$, $V_3$, and $V_o$ are high-pass, band-pass, low-pass, and notch outputs respectively.

Comparing with the general biquad form of Eqn. 3.3, it can be seen that each of the biquad parameter viz. $\omega_\emptyset$ , $Q$, $\omega_n$ , and gain, can be adjusted independently by varying the corresponding resistance ratio. The resonant frequency $\omega_\emptyset$ can be adjusted by ratio $R_2/R_4$ , $Q$ by $R_2/R_3$ , the notch frequency $\omega_n$ by $R_5/R_6$ , and

the gain by $R_2/R_1$. Thus for tuning of the filters, $\omega_0$ can be tuned by $R_4$, Q by $R_3$, $\omega_n$ by $R_7$, and gain by $R_1$. The parameters $\omega_o$, Q, $\omega_n$, and gain depends on the required transfer function. Hence first the transfer functions for each of the elliptic low-pass filter, Bessel low-pass filter and elliptic notch filter, which satisfy the specifications listed earlier in chapter 2, are obtained as shown in the next section. The transfer functions are obtained in the cascaded biquad stages. Each biquad is implemented as shown in Fig. 3.6. The resistance ratios for each biquad are obtained from the parameters for that biquad, which are derived from the transfer function for that biquad section.

## 3.5 FILTER DESIGN

In this section, the design technique to derive the transfer functions for each of the elliptic low-pass filter, Bessel low-pass filter, and elliptic notch filter, is explained. The transfer functions for each of the filters which satisfy the specifications listed earlier in section 2.3, are derived in the subsequent sections. The transfer functions are derived keeping in mind that the filters are to be realized using switched capacitor circuits.

To achieve variable cut-off frequency, frequency-response normalization design technique is followed [2, 11]. In this method, the required specifications are transformed to normalized low-pass specifications having a cut-off of 1 rad/s. This technique offers an advantage in case of the circuits with SC filters, that the frequency denormalization can be done by the external clock which controls the cut-off frequency. The transfer functions are obtained in the cascaded biquad form, so that they can be implemented with the SCF IC MF 10, and each of the filter parameter can be tuned independently.

The required filter type viz. low-pass, high-pass, band-pass, band-reject, etc. can be then obtained from the normalized low-pass transfer function by appropriate substitution for the

normalized frequency parameter $\bar{s}$. The transfer function obtained after the frequency denormalization, satisfy the required specifications. As we want to implement low-pass elliptic, low-pass Bessel and a elliptic notch filters, the denormalization for the low-pass filter and notch filter are included in this section.

For low pass filter the denormalized transformation is simply a scaling of s,

$$H_{Lp}(\bar{s}) = H_N(s)\Big|_{s = k\bar{s}} \qquad (3.8)$$

where, $k = \omega_c$

As seen in section 3.4, the frequency variable in the transfer function obtained with the switched capacitor filter, is scaled by a factor $\lambda = 2\pi f_{clk}/100$. Hence by selecting $k = \lambda$, the denormalization can be achieved. The normalized low-pass transfer function is implemented using IC MF10. The denormalization is then done by clock frequency with denormalized cut-off frequency $f_c$ as $f_{clk}/100$.

The design procedure for the notch filter is similar to that of the low-pass filter. First the normalized specifications are obtained. The normalized low-pass transfer function which satisfies these specifications is obtained [2]. The denormalized notch filter transfer function is then obtained by substituting for s as shown in Eqn. 3.10.

$$H_{No}(\bar{s}) = H_N(s)\left|\; s = \frac{B\,\bar{s}}{\bar{s}^2 + \omega_n^2}\right. \qquad (3.9)$$

where B depends on the bandwidth and $\omega_n$ is the notch frequency. To achieve clock controlled notch frequency, the denormalization is done by selecting $\omega_c = \lambda$. The denormalized notch transfer function with $\omega_c = \lambda$, is implemented using switched capacitor filter IC MF

10. The notch frequency is denormalized by the external clock frequency with $f_c = f_{clk}/100$ or $f_{clk}/50$.

## 3.6 ELLIPTIC LOW-PASS FILTER

The required specifications are listed in section 2.3. As the filter is required to have a variable cut-off, the specifications are in the normalized form. A filter of order $\geq 7$ is required to meet the listed specifications (as shown in Appendix A). Since SCF is based on the biquad design, it is easier to build second order filter section with programmability. Hence it is decided to implement an eighth order filter. The normalized low-pass transfer functions for various filter specifications are available [2, 11, 17]. However, for the specifications decided, the transfer function is not tabulated. Hence the mathematical approximations for the elliptic filter design adopted in [2], are followed to get the transfer function for the required specifications.

For elliptic filter, the cut-off frequency is given by [8],

$$\omega_c = \sqrt{\omega_p \times \omega_a} \quad , \tag{3.10}$$

where, $\omega_p$ is pass-band edge and $\omega_a$ is the stop-band edge.

Following the procedure available in [8], the normalized transfer function (dc gain = 1, $\omega_c$ = 1 rad/sec.) obtained in the cascaded biquad form is,

$$H_N(s) = 2.876332 \times 10^{-3} \; H_1(s) \; H_2(s) \; H_3(s) \; H_4(s) \tag{3.11}$$

where,

$$H_1(s) = \frac{s^2 + 14.3482}{s^2 + 0.8712s + 0.2915}$$

$$H_2(s) = \frac{s^2 + 2.231643}{s^2 + 0.4729\,s + 0.6124}$$

$$H_3(s) = \frac{s^2 + 1.3204}{s^2 + 0.1825s + 0.8397}$$

$$H_4(s) = \frac{s^2 + 1.1288}{s^2 + 0.0447s + 0.92646}$$

The transfer functions are in the form of notch function. The parameters for each stage such as the resonance frequency ($\omega_0$), quality factor ($Q$), attenuation, and notch frequency ($\omega_n$) are given in Table 3.3. The calculated magnitude and phase response of this filter is as shown in Fig. 2.6.

Comparing the notch filter transfer function,

$$H_{No}(s) = \frac{s^2 + \omega_n^2}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

with,

$$H_{No}(s) = \frac{V_o}{V_i} = \frac{R_2}{R_1} \frac{(R_7/R_5)\, s^2 + (R_7/R_6)\lambda^2}{s^2 + (R_2/R_3)\lambda s + (R_2/R_4)\lambda^2}$$

it can be seen that the denormalization is done by the clock frequency, the denormalization factor being $\lambda = 2\pi f_{clk}/100$. For $\Omega_s = 1.1$, the denormalized pass-band edge $f_p$, 3-dB cut-off frequency $f_c$, and stop-band edge $f_a$ are,

$$f_p = 0.00953 f_{clk},\ f_c = 0.01\ f_{clk},\ \text{and}\ f_a = 0.01048 f_{clk}$$

Each filter parameter $\omega_0$, $Q$, $\omega_n$ and gain can be adjusted independently. This is a significant feature of state variable feedback realization. The circuit components are selected so as to facilitate the independent adjustment of each of the circuit parameters by adjusting the value of a single resistor. Hence the

components for each biquad are selected as,

1) Select $R_2$

2) Take $R_5 = R_7$ and select the value of $R_5$

3) Take $R_3 = (Q/\omega_0)R_2$

4) Take $R_4 = (1/\omega_0^2)R_2$

5) Take $R_6 = (1/\omega_n^2)R_7$

The circuit components for the four biquad sections are obtained in the above manner. The frequency response of each biquad is simulated and the attenuation of $2.8768332 \times 10^{-3}$ is distributed among the four sections. The attenuation for each section is selected such that at resonance and for maximum possible input amplitude, any of the op-amp or the integrator outputs do not reach the saturation limit. The value of $R_1$ for each stage is then chosen so as to give the required attenuation for that stage. The calculated resistance ratios and resistance values for each biquad, are given in Table 3.4. However since all the resistances can not be obtained as the standard values, the resistors $R_3$, $R_4$, $R_6$ are kept variable with which the resistance ratios can be accurately adjusted.

The circuit schematic of the eighth order elliptic filter based on SCF IC MF 10, with the actual component values, is shown in Fig. 3.7. The circuit consists of an input section followed by two fourth order filter sections. The input section provides an input over-voltage protection and the buffering of the input signal as shown in Fig. 3.7(b). Filter section I, shown in Fig. 3.7(c), provides the filter sections $H_1(s)$ and $H_2(s)$ with one IC MF 10, two op-amps, and fourteen resistances. As the attenuation selected for the biquad section 1 and 2 is 25 and 3.3 respectively, the filter section I provides an attenuation of 82.5, a gain of $12.12 \times 10^{-3}$. Similarly filter section II, shown in Fig. 3.7(d), provides $H_3(s)$ and $H_4(s)$ with one IC MF 10, two op-amps, and fourteen resistances. As the attenuation selected for

biquad sections 3 and 4, is 1.5 and 2.81 respectively, the filter section II provides an attenuation of 4.21, a gain of 0.23. The cascaded gain of the two filter sections is then $2.78 \times 10^{-9}$ which is the required gain factor in Eqn. 3.11.

## 3.7 BESSEL LOW-PASS FILTER

The required specifications are listed in section 2.3. As the filter is required to have a variable cut-off, the specifications are in the normalized form. It has been decided to implement an eighth order Bessel filter.

The design procedure adopted is similar to elliptic filter. The normalized low-pass transfer function is first obtained [2]. The denormalization is then done by the clock frequency which gives the pass-band edge $f_p$ as $f_{clk}/100$. For Bessel filter, the normalized transfer function is obtained by normalizing the pass-band edge. The normalized low-pass transfer function (dc gain = 1, $\omega_p$ = 1 rad/sec.) obtained in the cascaded biquad form is,

$$H_N(s) = 2.0270 \times 10^{6}\ H_1(s)\ H_2(s)\ H_3(s)\ H_4(s) \qquad (3.12)$$

where,

$$H_1(s) = \frac{1}{s^2 + 5.678s + 48.43}$$

$$H_2(s) = \frac{1}{s^2 + 8.7366s + 38.56}$$

$$H_3(s) = \frac{1}{s^2 + 10.409s + 33.93}$$

$$H_4(s) = \frac{1}{s^2 + 11.175s + 31.977}$$

Each biquad is in the form of low-pass filter transfer function. The parameters for each biquad $\omega_0$, $Q$, and gain are

tabulated in Table 3.4. The simulated magnitude and phase response is as shown in Fig. 2.7. The phase response is linear up to nearly eight times the cut-off frequency and the maximum pass-band attenuation is 0.9 dB.

Comparing low pass filter transfer function,

$$H_{Lp}(s) = \frac{1}{s^2 + (\omega_0/Q)s + \omega_0^2}, \text{ with}$$

$$H_{Lp}(s) = \frac{V_3}{V_i} = \frac{R_2}{R_1} \frac{1}{s^2 + (R_2/R_3)\lambda s + (R_2/R_4)\lambda^2}$$

it can be seen that the denormalization is done by the clock frequency, the denormalizing factor being $\lambda = 2\pi f_{clk}/100$. For $\Omega_s = 10$, the denormalized pass-band edge $f_p$, 3-dB cut-off frequency $f_c$, and stop-band edge $f_a$ are,

$$f_p = 0.01 f_{clk},\ f_c = 0.0316\ f_{clk},\ \text{and}\ f_a = 0.1 f_{clk}$$

Each section the parameters $\omega_0$, $Q$, and gain can be adjusted independently. The circuit components are selected so as to facilitate the independent adjustment of each of the circuit parameters by adjusting the value of a single resistor. Hence the components for each biquad are selected as,

1) Select $R_2$
2) Take $R_3 = (Q/\omega_0)R_2$
3) Take $R_4 = (1/\omega_0^2)R_2$

The circuit components for the four biquad sections are obtained in the above manner. The frequency response for each stage is simulated and the gain of $2.027025 \times 10^6$ is distributed among the four sections. The gain for each section is selected such that at resonance and for maximum allowable input amplitude,

any of the op-amp or the integrator outputs, does not reach saturation limit. The calculated resistance values for each biquad, are as shown in the Table 3.5. However since all the resistances can not be obtained as the standard values, the resistors $R_3$ and $R_4$ are kept variable with which the resistance ratios can be accurately adjusted.

The circuit schematic of the eighth order Bessel filter based on SCF IC MF 10, with the actual component values, is as shown in the Fig. 3.8. The circuit consists of an input section followed by two fourth order filter sections. The input section provides an input over voltage protection and the buffering of the input signal as shown in Fig. 3.8(b). Filter section I, shown in Fig. 3.8(c), provides the filter sections $H_1(s)$ and $H_2(s)$ with one IC MF 10, two op-amps, and fourteen resistances. As the gain selected for the biquad section 1 and 2, is 2 and 3.3 respectively, the filter section I provides a gain of 200. Similarly filter section II, shown in Fig. 3.8(d), provides $H_3(s)$ and $H_4(s)$ with one IC MF 10, two op-amps, and fourteen resistances. As the attenuation selected for biquad sections 3 and 4, is 100 and 101 respectively, the filter section II provides a gain of 10100. The cascaded gain of the two filter sections is then $2.02 \times 10^6$ which is the required gain factor in Eqn. 3.12.

## 3.8 ELLIPTIC NOTCH FILTER

The design procedure is similar to the elliptic low-pass filter. First the normalized low-pass transfer function which satisfies the required specifications is obtained [2]. The normalized notch filter transfer function (dc gain = 1, $\omega_c = 1$) is then obtained by substituting for s as shown in (3.10).

$$H_{No}(\bar{s}) = H_N(s) \Big|_{s = \frac{B\,\bar{s}}{\bar{s}^2 + \omega_n^2}} \qquad (3.13)$$

The second order notch filter satisfies the specifications. The

normalized transfer function obtained in the biquad form is,

$$H_{No}(s) = \frac{s^2 + 0.9975}{s^2 + 0.0509s + 0.9975} \qquad (3.14)$$

The biquad is in the form of a notch-filter transfer function. The parameters $\omega_0$, $Q$, attenuation, and $\omega_n$ are as shown in Table 3.7. The calculated magnitude and phase response of this filter is as shown in Fig. 2.8.

Comparing the notch filter transfer function,

$$H_{No}(s) = \frac{s^2 + \omega_n^2}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

with,

$$H_{No}(s) = \frac{V_o}{V_i} = \frac{R_2}{R_1} \frac{(R_7/R_5)\, s^2 + (R_7/R_6)\lambda^2}{s^2 + (R_2/R_3)\lambda s + (R_2/R_4)\lambda^2}$$

it can be seen that the denormalization is done by the clock frequency, the denormalization factor being $\lambda = 2\pi f_{clk}/100$. The denormalized pass-band edges $f_{p1}$, $f_{p2}$, notch frequency $f_n$, and 3-dB cut-off frequency $f_c$, are,

$$f_{p1} = 0.00953 f_{clk},\ f_{p2} = 0.01048 f_{clk},\ f_n = 0.0099\ f_c = 0.01\ f_{clk}$$

Each filter parameter $\omega_0$, $Q$, $\omega_n$ and gain can be adjusted independently. The circuit components are selected so as to facilitate the independent adjustment of each of the circuit parameters by adjusting the value of a single resistor. Hence the components are selected as,

1) Select $R_2$

2) Take $R_5 = R_7$ and select the value of $R_5$

3) Take $R_3 = (Q/\omega_0)R_2$

4) Take $R_4 = (1/\omega_0^2)R_2$

5) Take $R_6 = (1/\omega_n^2)R_7$

The calculated resistance ratios and resistance values for each biquad, are as shown in the Table 3.8. However since all the resistances can not be obtained as the standard values, the resistors $R_3$, $R_4$, $R_6$ are kept variable with which the resistance ratios can be accurately adjusted.

The circuit schematic of the second order elliptic notch filter based on SCF IC MF 10, with the actual component values, is as shown in the Fig. 3.9. The input over voltage protection is provided followed by the buffering of the input signal source. The filter is implemented as one biquad, using one section of the IC Mf 10, one op-amp, and seven resistors. Hence two notch filters can be implemented with one IC MF 10.

## 3.9 TUNING OF THE FILTERS

As seen earlier, the resistor ratios determine the coefficients of the filter transfer function and hence the filter response. The resistor values are taken so as to get resistance ratios $R_2/R_3$, $R_2/R_4$, and $R_7/R_6$ accurately. However the circuit parameters need to be tuned accurately by adjustment of the resistance ratios. Each parameter can be independently tuned by the tuning procedure for the elliptic, and Bessel low-pass filters and elliptic notch filter [11].

1. Adjust $R_4$ to get resonance at the frequency $\omega_0$. At resonance, the phase shift between input and band-pass output is 180°.
2. Adjust $R_3$ to get the desired $Q$, which is obtained by adjusting the gain of the band-pass output at resonance frequency to unity.
3. Adjust $R_6$ to get notch at frequency $\omega_n$, i.e. the frequency where maximum attenuation occurs.

## 3.7 Test Results

The eighth order elliptic and Bessel low-pass filters with SCF IC MF10 were implemented on PCBs, each filter was implemented on a double sided PCB of size 185 mm X 110 mm. The second order notch filter is also implemented on the PCB with four filter units implemented on a double sided PCB of size 185 mm X 110 mm. The cut-off frequency is clock controlled, the cut-off being $1/100^{th}$ times the clock frequency.

The actual magnitude and phase response of the eighth order elliptic filter with cut-off frequency at 1 kHz (clock frequency = 100 kHz) are shown in Fig. 3.10. The pass-band edge $f_p$ is 0.95 kHz and the stop-band edge $f_a$ is 1.05 kHz. The observed pass-band ripple is $A_p$ is 1 dB, which is higher than the designed value of 0.1 dB. This is because of the tuning limitations due to adjustment of the resistance ratios beyond a certain accuracy is not possible even with the ten-turn trim-pots. The stop-band attenuation within the limitation of the measuring instrument, is 50 dB, which meets the specified value. The transition ratio has been found to be equal to 1.1, as specified.

The actual magnitude and phase response of the eighth order Bessel filter with pass-band edge at 1 kHz (clock frequency at 100 kHz) are shown in Fig. 3.11. The 3-dB cut-off frequency is 3.16 kHz, and the stop-band edge is 10 kHz. The pass-band ripple $A_p$ is found to be less than 1 dB. Also the phase shift between the input and the output is linear up to eight times the pass-band edge. The transition ratio is found to be 10, as specified. Also the stop-band attenuation within the limitations of the measuring instrument is 40 dB, as specified.

The actual magnitude response of the notch filter with cut-off frequency at 50 Hz (clock frequency at 5 kHz) are shown in Fig. 3.12. The notch is obtained at 49 Hz. The pass band ripple is found to be 1 dB, pass-band bandwidth at 50 Hz is 5 Hz, and stop-band bandwidth is 1 Hz as specified.

Table 3.1. Values of the numerator coefficients $a_2$, $a_1$, and $a_0$ in Eqn. 3.1 for different filter types.

| Numerator coefficients | | | Filter type |
|---|---|---|---|
| $a_2$ | $a_1$ | $a_0$ | |
| 0 | 0 | $a_0$ | Low-pass filter with pass-band gain $a_0/\omega_0^2$ |
| $a_2$ | 0 | 0 | High-pass filter with pass-band gain $a_2$ |
| 0 | $a_1$ | 0 | Band-pass filter with pass-band gain $a_1 Q/\omega_0$ |
| 1 | $-\omega_0/Q$ | $\omega_0^2$ | All-pass filter with unity gain |

Table 3.2. List of some switched capacitor ICs. (Source [13])

| Manufacturer | IC | Function |
|---|---|---|
| National Semi. | MF 4 | 4th order Butterworth low-pass. |
| | MF 5 | Universal biquad. |
| | MF 6 | 6th order Butterworth low-pass. |
| | MF 8 | 4th order band-pass. |
| | MF 10 | Dual universal biquads. |
| Exar | XR-2402 | Universal biquad. |
| Trig-Tek | | 7th order low-pass Chebyshev. |

Table 3.3 Filter parameters for each biquad stage of the eighth order elliptic filter of Fig. 3.7.

| Stage | $\omega_o$ | $Q$ | $\omega_n$ | Attenuation |
|---|---|---|---|---|
| 1 | 0.5398 | 0.6196 | 3.7879 | 25 |
| 2 | 0.7823 | 1.654 | 1.4938 | 3.3 |
| 3 | 0.9163 | 5.021 | 1.1491 | 1.5 |
| 4 | 0.9624 | 21.52 | 1.0624 | 2.81 |

Table 3.4 Calculated resistance ratios for the eighth order elliptic filter given by Eqn. 3.11.

| Stage | $R_2/R_3$ | $R_2/R_4$ | $R_7/R_6$ | $R_1/R_2$ |
|---|---|---|---|---|
| 1 | 0.8711 | 0.2915 | 14.3482 | 25 |
| 2 | 0.4729 | 0.6123 | 2.2316 | 3.3 |
| 3 | 0.1825 | 0.8397 | 1.3204 | 1.5 |
| 4 | 0.0447 | 0.9264 | 1.1288 | 2.81 |

Table 3.4.a. Designed resistance values (in kΩ) for the resistor ratios given in Table 3.4.

| Stage | $R_1$ | $R_2$ | $R_3$ | $R_4$ | $R_5$ | $R_6$ | $R_7$ |
|---|---|---|---|---|---|---|---|
| 1 | 25 | 1 | 1.14 | 3.43 | 100 | 6.96 | 100 |
| 2 | 3.3 | 1 | 2.11 | 1.63 | 10 | 4.48 | 10 |
| 3 | 1.5 | 1 | 5.75 | 1.19 | 10 | 7.57 | 10 |
| 4 | 2.81 | 1 | 22.36 | 1.08 | 10 | 8.86 | 10 |

Table 3.5 Filter parameters of each biquad stage of the eighth order Bessel filter of Fig. 3.8.

| Stage | $\omega_0$ | $Q$ | Gain |
|---|---|---|---|
| 1 | 6.959 | 1.225 | 2 |
| 2 | 6.210 | 0.710 | 100 |
| 3 | 5.824 | 0.559 | 100 |
| 4 | 5.654 | 0.505 | 101 |

Table 3.6 Calculated resistance ratios for the eighth order Bessel filter as given in Eqn. 3.12.

| Stage | $R_2/R_3$ | $R_2/R_4$ | $R_2/R_1$ |
|---|---|---|---|
| 1 | 5.678 | 48.430 | 2 |
| 2 | 8.736 | 38.568 | 100 |
| 3 | 10.409 | 33.930 | 100 |
| 4 | 11.175 | 31.977 | 101 |

Table 3.6.a Designed resistance values (in kΩ) for resistor ratios in Table 3.6.

| Stage | $R_1$ | $R_2$ | $R_3$ | $R_4$ |
|---|---|---|---|---|
| 1 | 50 | 100 | 17.60 | 2.06 |
| 2 | 1 | 100 | 11.44 | 2.59 |
| 3 | 1 | 100 | 9.60 | 2.94 |
| 4 | 0.99 | 100 | 8.90 | 3.12 |

Table 3.7 Filter parameters for the notch filter of Fig. 3.9.

| $\omega_o$ | $Q$ | $\omega_n$ | Gain |
|---|---|---|---|
| 0.9987 | 19.62 | 0.9987 | 1 |

Table 3.8 Calculated resistance ratios for the notch filter, as given in Eqn. 3.14.

| $R_2/R_3$ | $R_2/R_4$ | $R_7/R_6$ | $R_2/R_1$ |
|---|---|---|---|
| 0.0509 | 0.9975 | 0.9975 | 1 |

Table 3.8.a Designed resistance values (in kΩ) for the resistor ratios in Table 3.6.

| $R_1$ | $R_2$ | $R_3$ | $R_4$ | $R_5$ | $R_6$ | $R_7$ |
|---|---|---|---|---|---|---|
| 100 | 1 | 27.77 | 1 | 1 | 1 | 100 |

# CHAPTER 4

# I/O EXPANSION UNIT

## 4.1 INTRODUCTION

I/O expansion unit enhances the I/O handling of the DSP board, PCL-DSP25, from single analog I/O channel to four analog I/O channels. The unit also provides a programmable timer/counter to generate three clock outputs with their frequencies being programmable by the DSP board.

The DSP chip TMS 320C25 has sixteen software ports which are accessed by IN and OUT instructions. On the DSP board, PCL-DSP25, out of these sixteen ports, one port is used for analog I/O, one port is used to write terminal count in the programmable timer/counter to run interrupt based programs, and one port is reserved as PC communication register. The ports used by the on-board peripherals on PCL-DSP25, are as shown earlier in Table 2.1. We can use remaining software ports for the I/O expansion and to provide a programmable timer.

Various schemes for I/O expansion are possible. However the scheme should be such that the maximum sampling rate for each channel after the I/O expansion should not be less than 10 kSa/s. This criterion is set so that even after the I/O expansion, most of the audio range applications can be served. Also the scheme should be such that no hardware modifications are required on the DSP board.

As discussed in the previous chapter, the elliptic and Bessel filters, with programmable cut-off frequency, are realized using SCF IC MF 10. The cut-off frequency of the switched capacitor filters is controlled by clock input to the respective filter board, the cut-off frequency being $1/100^{th}$ times the clock frequency. Hence to achieve programmable cut-off, we need to generate clock of frequency 100 times the cut-off frequency desired. For this purpose programmable interval timer/counter

is interfaced with the DSP board.

This chapter first discusses the I/O expansion block of the I/O expansion unit. The chapter reviews two possible schemes for I/O expansion. To>make the system cost-effective, the scheme with multiplexer and demultiplexer is selected. Design and implementation of this scheme is then presented. The chapter then discusses the programmable clock generation block of the I/O expansion unit. First some features of reviews the programmable timer/counter chip Intel 8253, are reviewed and this is followed by the design and implementation of the interface between, the DSP board and 8253. The chapter concludes with the assignment of the DSP ports as used by the board PCL-DSP25 and I/O expansion unit developed for this board.

## 4.2 I/O ENHANCEMENT SCHEMES

Two schemes for I/O expansion which satisfy the guidelines set in the previous section are surveyed here.

### Scheme A

This scheme makes use of one ADC, One DAC, and a sample/hold for each channel. This would mean that to have four analog I/O, we should have three external ADC, DAC and S/H, considering that one analog I/O is already available on the DSP board. We can assign one software port with each analog I/O channel as, channel 1 with Port 2 or port 3, channel 2 with Port 4, channel 3 with Port 5, and channel 4 with Port 6. The scheme requires a decoding logic to decode read and write instructions for each of the ports, port 4, port 5, and port 6. Also one external ADC, DAC, and a sample/hold is required for each of the three channels. This would essentially mean replicating the on-board analog I/O interface as shown earlier in Fig. 2.4., by replacing port 2 in Fig. 2.4., with port 4, port 5, and port 6 respectively.

The advantages of this scheme are,

a. The maximum sampling frequency for each channel would be the same even after I/O expansion.
b. Each of the inputs are sampled at almost the same instant of time which may be required for some critical applications.

However, the major disadvantage is the cost of the I/O expansion unit. The cost may not be justified for most general requirements especially in audio range applications where the maximum sampling frequency of 10 kSa/s would suffice.

Scheme B

This scheme makes use of a multiplexer (MUX) for input channels and a demultiplexer (DEMUX) for the output channels. MUX has a number of analog inputs, one analog output and address lines. The address lines are internally decoded and one of the inputs appear at the output depending on the logic levels on the address lines.

DEMUX has one analog input, number of analog outputs and address lines. Address lines are internally decoded and the input appears at one of the output channels depending on the logic levels on the address lines.

The scheme in the form of the block diagram is as shown in Fig. 4.1. It essentially uses the ADC and DAC of the DSP board for all analog inputs and outputs respectively. The DSP board places the address of the required input channel on the address lines of the multiplexer. The multiplexer, then connects that input channel as the input to the DSP board. Similarly, the DSP output is placed on the required output channel by the demultiplexer. The required output channel is selected by the DSP board by placing the channel address on the address lines of the demultiplexer.

Since one ADC is used for all the channels, the maximum frequency with which each channel can be sampled is reduced. As

seen earlier, with expansion to four I/O channels, the maximum sampling rate is more than 10 kSa/s. Hence we need a 4-1 multiplexer for the input channels and a 1-4 demultiplexer for the output. channels. Considering the cost-effectiveness of this scheme and its potential to fulfill most general requirements of four I/O channels, with maximum sampling frequency for each channel as 10 kSa/s, it is decided to implement this scheme for the I/O expansion.

## 4.3 DESIGN AND IMPLEMENTATION OF I/O EXPANSION BOARD

To assign one software port with one analog I/O channel, we need to decode read and write instructions of the port. Reading of either of these ports should give a start of conversion pulse to the ADC. Similarly, writing to any of these ports should latch the data on the data bus and the data should be given to the DAC. But the hardware on the PCL-DSP25 board decodes the reading and writing of only the port 2 and port 3, and use it for ADC start of conversion and DAC latch. Hence to implement the decoding logic for each of the ports, port 4, port 5, and port 6, hardware modifications are required to be done on the DSP board. Hence it is required that the scheme be modified.

The modified scheme is as shown in Fig. 4.2. Instead of assigning a port to a channel, each input and output channel is assigned an address. One port, called as MUX port, is reserved to which the address of the required input channel is written. Similarly, one port, called as DEMUX port, is reserved to which the address of the output channel to be selected is written. For reading from an analog channel, output that channel address to MUX port which appears on the data lines *D1* and *D0*. The data lines *D1* and *D0* are latched in an external register, MUX address register, at this instant. The output of this register acts as address for the multiplexer. For example, to select input channel 1, output data >0001 to the MUX port followed by reading the I/O port, port 2 or port 3. Similarly before writing a value to an output

channel, first select the required output channel by writing the channel address to DEMUX port. The channel address appears on the data lines *D1* and *D0*, which are latched in an external register, DEMUX address select, at this instant. The output from this register acts as address lines for the demultiplexer.

The port 5 has been selected as the MUX port and port 4 is selected as the DEMUX port. Writing the values, >XXX0, >XXX1, >XXX2, >XXX3, to the MUX port 5, selects input channel 0, channel 1, channel 2, channel 3, respectively. Similarly writing the values, >XXX0, >XXX1, >XXX2, >XXX3, to the DEMUX port 4, selects the output channel 0, channel 1, channel 2, channel 3, respectively. The assigned ports and the input-output channel addresses can be read from Table 4.1.

## Circuit Explanation

The schematic of the circuit developed is as shown in Fig. 4.3. During the OUT instruction, the port address appears on the lower four bits of the address lines *A3-A0*. Also during IN/OUT instructions the pin $IOE^*$ goes low. The pin $W^*/R$ goes low to indicate a write operation during OUT instruction. With the help of *A3-A0*, $IOE^*$, and $W^*/R$ the writing to the ports can be decoded with a 3-to-8 decoder.

1. The decoder U1 decodes the writing to the port 4, i.e. the occurrence of the instruction OUT PORT 4. Data on lines *D1* and *D0*, is latched by MUX address register U3. Outputs Q0 and Q1 of U3 act as address lines for the multiplexer U4, and the multiplexer selects the corresponding input channel as shown in Table 4.1.
2. Similarly U1 decodes the writing to the port 5, i.e. the occurrence of the instruction OUT PORT 5. Data on lines *D1* and *D0*, is latched by DEMUX address register U5. Outputs Q0 and Q1 of U5 act as address lines for the demultiplexer U6 and the demultiplexer U6 selects the corresponding output channel as

shown in Table 4.1.

The timing diagram for decoding the port access is as shown in Fig. 4.4. The low power schottky (LS) TTL ICs with proper loading circuits satisfy the critical timing requirement to decode the port access and to latch the data appearing at the data lines during the execution of the port access instruction. The standard loading circuits for each TTL ICs are as shown in Fig. 4.5. The load resistors are selected so as to give minimum response time possible.

The sample program to illustrate the I/O operation with I/O expansion is included in Appendix C. The maximum sampling frequency is found to be higher than 10 kSa/s.

## 4.4 PROGRAMMABLE TIMER/COUNTER

Intel 8253 and 8254 are widely used programmable interval timer/counter chips [18]. The maximum input clock frequency for 8253 is 2.6 MHz and for 8254 is 8 MHz (10 MHz for 8254-2). For our application, the maximum sampling frequency would be around 10 kSa/s which restricts the maximum cut-off frequency to 5 kHz and hence maximum clock frequency to 500 kHz i.e. 0.5 MHz. Hence 8253 with maximum input clock frequency as 2.6 MHz which is also the maximum possible output frequency would suffice for our application.

8253 has three 16 bit programmable counters which can be programmed and operated independently in several different modes shown in Appendix D. We want to operate all the three counters in mode 3 to obtain three clock frequencies from 8253. Data sheets showing functional block diagram and details of the 8253 timer/counter are included in Appendix D. We consider here some details required for interfacing.

Address decoding logic to select the chip (by asserting $\overline{CS}$ pin low) decides the base address of this programmable peripheral

device. To select a particular counter and its mode of operation, a control word is to be written in the control register. The control word format is as shown in the Appendix D. On writing the control word, a particular counter is selected with its mode of operation (M2, M1, M0), mode of data transfer (*RW1*, *RW0*) and count interpretation (BCD). The count is then loaded in the counter selected. 8253 has 8 data lines and counters are 16 bit, hence 16 bit count is loaded in the sequence specified in the control word.

To access control register, counter 0, counter 1, counter 2, there are two address select lines. The control logic unit selects one of the above for the data transfer. The internal addresses for these are as shown in Table 4.2.

## 4.5 DESIGN AND IMPLEMENTATION OF PROGRAMMABLE TIMER INTERFACE

DSP processor TMS 320C25 run at its full speed of 40 MHz on the PCL-DSP25 board. This clock frequency can be divided by a suitable factor and applied as an input clock to 8253. For 8253, the maximum allowable clock frequency is 2.6 MHz, hence we can provide divide by 8, and divide by 16 options to provide a clock of 2.5 MHz.

We assign a software port for timer/counter operation. To distinguish this port from interval timer port, we will call it as cut-off timer port. During the execution of the OUT instruction, the port address appears on the lower four bits of the address lines which can be used for chip select of 8253. Since 8253 has 8 data lines, *D7-D0* data bus can be used as data lines for 8253. Two lines from the remaining 8 bit data lines *D8-D15* can be used as address lines *A1*, *A0* to 8253.

The port 6 is used as cut-off timer port. Out of the sixteen data lines, lower eight lines *D7-D0*, are used as data lines for 8253. These lines are either LSB or MSB, depending upon the contents of the control register and the order of occurrence. The two data lines, *D9* and *D8*, are used as address select lines *A1*, *A0* of the timer chip. Depending on the status of these two lines, *D9*

and *D8*, either the counter 0, or counter 1, or counter 2, or the control register is selected. The scheme can be more easily understood from Table 4.3.

### Circuit Explanation

The schematic of the circuit developed to interface the DSP board PCL-DSP25 with the programmable time/counter chip 8253, is included in the schematic of the I/O expansion unit shown in Fig. 4.3.

U7 divides the clock out from the DSP board (20 MHz) by a factor of 8 to provide a clock of 2.5 MHz. This is applied to i/p clock of the 8253.

The decoder chip U1 decodes occurrence of OUT Port 6. Either the control register, or counter 0, or counter 1, or counter 2 is selected depending upon *D9*, *D8*. The data, *D7-D0*, is internally latched into the selected register or the counter. Hence no external data latch is required. Gates of the counters are kept at logic level high, which allows the clock generation as soon as the count is loaded.

The DSP assembly language program which does the initialization of 8253 is included in Appendix C. Since the 'C' interface library is available, the 'C' program, which is included in Appendix C, asks the user to enter three cut of frequencies for the filters, and generates the corresponding clock frequency.

## 4.6 SUMMARY

The I/O expansion unit has been developed for the DSP board PCL-DSP25. The unit consists of an I/O expansion block to expand the analog I/O from single channel to four channel, and a programmable timer/counter interface. The I/O expansion unit is implemented on a double sided PCB of size 215 mm X 110 mm.

After the analog I/O expansion, the maximum sampling frequency for each channel is found to be higher than 10 kSa/s.

Also three programmable clocks, each independently programmable by the DSP board are available. The clocks from the I/O expansion unit are applied as the input clock to the SC filter based low-pass filter in the signal conditioning unit.

Table 4.1. DSP port and I/O channel address assignment for I/O expansion.

| Port 5 - MUX port to select i/p channel. | |
|---|---|
| Data output to port 4 | I/P channel address |
| *D1* *DO* | |
| 0 0 | 0 |
| 0 1 | 1 |
| 1 0 | 2 |
| 1 1 | 3 |
| **Port 4 - DEMUX port to select o/p channel** | |
| Data output to port 5 | O/P channel address |
| *D1* *DO* | |
| 0 0 | 0 |
| 0 1 | 1 |
| 1 0 | 2 |
| 1 1 | 3 |

Table 4.2. Address select logic on programmable timer/counter 8253.

| *A1* | *AO* | Selects |
|---|---|---|
| 0 | 0 | Counter 0 |
| 0 | 1 | Counter 1 |
| 1 | 0 | Counter 2 |
| 1 | 1 | CR |

Table 4.3. Assignment of DSP port and data lines for programmable timer interface.

| Port 6 - Cut-off timer/counter port | | |
|---|---|---|
| *D7 - D0* - 8 bit data lines, either LSB or MSB depending upon the R/W operation selected and the order of the loading. | | |
| *D9 -> A1* | *D8 -> A0* | Selects |
| 0 | 0 | Counter 0 |
| 0 | 1 | Counter 1 |
| 1 | 0 | Counter 2 |
| 1 | 1 | CR |

# CHAPTER 5

# APPLICATION EXAMPLES

## 5.1 INTRODUCTION

To illustrate multiple I/O handling of the DSP board with the help of the system developed, it is proposed to develop

(1) band-pass filters for the four analog inputs,

(2) a cross-correlation technique for the system impulse response characterization.

The band-pass filter application makes use of PC for user interface and deriving the filter coefficients, while the filter algorithm is implemented using DSP program.

The cross-correlator calculates the cross-correlation [19, 20] function of two signals which gives information regarding the time or phase relationship between the two signals.

## 5.2 BAND-PASS FILTER FOR FOUR CHANNELS

In this application, all the four inputs will be sampled, band-pass filtered, and output with appropriate signal conditioning. The sampling rate $f_s$ is user-specified and will be the same for all the channels. However, the band-pass filter parameters can be specified for each channel separately. It was decided to provide a second order band-pass filter with user-specified parameters resonant frequency $f_0$, and quality factor $Q$. The filtered outputs are given to respective analog output channels. The analog inputs are sampled at the specified rate, and the filtering is done on these sampled data.

The digital filter for the user-specified parameters is obtained as follows. First the analog band-pass filter transfer function is obtained. From this, the digital filter transfer function is derived by bilinear transformation from s-domain to z-domain [2], while doing this transformation, pre-warping of the

response frequency also has to be done.

The transfer function of the second order analog band-pass filter is

$$H_{Bp}(s) = \frac{\omega_0/Q\ s}{s^2 + (\omega_0/Q)\ s + \omega_0^2} \qquad (5.1)$$

where $\omega_0 = 2\pi f_0$.

The corresponding digital filter transfer function after bilinear transformation with appropriate frequency pre-warping is

$$b_0 y[n] = a_2 x[n-2] + a_0 x[n] - b_2 y[n-2] - b_1 y[n-1] \qquad (5.2)$$

where,

$$b_0 = 1 + (d/Q) + d^2$$
$$b_1 = 2\ (d^2-1)$$
$$b_2 = d^2 - (d/Q) + 1$$
$$a_0 = d/Q$$
$$a_2 = -d/Q$$

where,

$$d = \omega_0/2f_s$$

The digital filter obtained is a second order recursive filter. The coefficients are derived using 'C' program. These coefficients are properly scaled and are stored in the data memory of the DSP chip.

The block diagram of the band-pass filter for four analog inputs is as shown in Fig. 5.1. The DSP program samples each input at the specified rate by writing the input channel address to the MUX port. The digital recursive filter requires the present sample of input and the previous two samples of both input and output. Hence for all the four channels, the previous two samples of both the input and output are stored in the data memory locations and are updated with the recent values. The samples are multiplied with the corresponding coefficients stored in the data memory. The

D/A converter output is then given to the corresponding output channel by writing the address of the output channel to the DEMUX port.

The algorithm developed for this application can be tested by applying four sinusoidal inputs to the four analog channels, and observing the filtered analog outputs for specified values of $f_o$, $f_s$ and $Q$. Also, the effect of aliasing can be observed and the reduction in the aliasing noise with anti-aliasing filter and smoothing filter can be noticed.

## 5.3 SYSTEM CHARACTERIZATION USING CROSS-CORRELATION TECHNIQUE

The cross-correlation function [19, 20] for two signals $x(t)$ and $y(t)$ is defined as

$$r_{xy}(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_0^T x(t-\tau)y(t)\,dt \qquad (5.3)$$

This may be interpreted as the time average of the product of the two signals, with one signal shifted (delayed) in time by $\tau$. Autocorrelation of a signal can be looked upon as cross-correlation of a signal with itself.

$$r_{xx}(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_0^T x(t-\tau)x(t)\,dt \qquad (5.4)$$

For a truly random signal, the autocorrelation function is non-zero only for $\tau = 0$ [19].

The block diagram for the system characterization with cross-correlation technique is as shown if Fig. 5.2. The linear system which is to be characterized is excited with random noise. The cross correlation between the random noise signal and the system output, is calculated by the cross-correlator.

$$r_{xy}(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_0^T x(t-\tau)y(t)\,dt$$

where $\qquad y(t) = x(t) * y(t) \qquad (5.5)$

$$= \int_{-\infty}^{\infty} x(t-u)h(u)\,du$$

Therefore,

$$r_{xy}(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_{0}^{T} [x(t-\tau) \int_{-\infty}^{\infty} x(t-u)h(u)\,du]\,dt$$

$$= \lim_{T\to\infty} \frac{1}{T} \int_{0}^{T} \int_{-\infty}^{\infty} x(t-\tau)\,x(t-u)h(u)\,du\,dt$$

$$= \lim_{T\to\infty} \frac{1}{T} \int_{-\infty}^{\infty} \int_{0}^{T} x(t-\tau)\,x(t-u)h(u)\,du\,dt$$

$$= \lim_{T\to\infty} \frac{1}{T} \int_{-\infty}^{\infty} h(u) [\int_{0}^{T} x(t-\tau)\,x(t-u)\,dt]\,du$$

$$= \int_{-\infty}^{\infty} h(u) [\lim_{T\to\infty} \frac{1}{T} \int_{0}^{T} x(t-\tau)\,x(t-u)\,dt]\,du \qquad (5.6)$$

Let $t - \tau = p$. Then $t - u = p + \tau - u$. With this substituting we get,

$$r_{xy}(\tau) = \int_{-\infty}^{\infty} h(u) [\lim_{T\to\infty} \frac{1}{T} \int_{0}^{T-\tau} x(p)\,x(p+\tau-u)\,dp]\,du$$

$$= \int_{-\infty}^{\infty} h(u)\,r_{xx}(u-\tau)\,du$$

$$= \int_{-\infty}^{\infty} h(t)\,r_{xx}(t-\tau)\,dt \qquad (5.7)$$

If $x(t)$ is random noise, then

$$\int_{-\infty}^{+\infty} r_{xx}(t-\tau) = r_0\,\delta(\tau)$$

i.e. $r_{xx}(\tau) = 0$ if $\tau \neq 0$

and therefore,

$$\int_{-\infty}^{+\infty} r_{xx}(t-\tau) = r_0$$

Hence

$$r_{xy}(\tau) = h(\tau)\ r_{xx}(0)$$

or

$$h(\tau) = r_{xy}(\tau) / r_{xx}(0) \qquad (5.8)$$

Hence cross-correlation of the output of the system excited with the random noise, gives the impulse response of the system. The technique is effective even in the presence of noise [19], since due to cross-correlation operation, the effect of the noise is reduced considerably. The system developed can be used for this application which require two analog input channels with appropriate signal conditioning. The algorithm developed can be tested by evaluating the impulse response for a simple RC low-pass filter.

# CHAPTER 6

# SUMMARY OF WORK DONE

## 6.1 INTRODUCTION

The data acquisition system for the DSP board PCL-DSP25 has been developed. The system consists of the signal conditioning unit and I/O expansion unit. The I/O expansion unit enhances the I/O handling of the DSP board from a single I/O channel to four I/O channels. The signal conditioning unit consists of anti-aliasing filters for conditioning of the input channels and smoothing filters for output conditioning. The filters are designed with their cut-off frequency controlled by the clock frequency. This feature makes the signal conditioning unit useful for a variety of applications. The I/O expansion unit provides the programmable timer interface with the DSP board, so that the cut-off frequencies of the filters can be controlled by the clock signals, the frequency of which is programmable by the DSP board.

The chapter summarizes the performance of the system developed with each unit reviewed separately. followed by application examples.

## 6.2 SIGNAL CONDITIONING UNIT

Signal conditioning unit consists of an anti-aliasing filter for each input channel and a smoothing filter for each output channel and notch filters for input channels. For this purpose, the signal conditioning unit is developed with two units of elliptic low-pass filter, two units of Bessel low-pass filter, and four units of elliptic notch filter. Depending upon the application, either of the low-pass filters can be used as anti-aliasing filter at the input or smoothing filter at the output. Also, to reduce the possible power-line interference at

the input, as may be required for some applications, a notch filter can be used. The specifications for each type of the filter are listed below. All the filters are realized using switched capacitor filter to have programmable cut-off frequency. The cut-off frequency of the filters is 1/100 times the input clock frequency.

### 6.2.1 Elliptic low-pass filter

The specifications of the eighth order elliptic low-pass filter are shown below.

A. Performance characteristics

| | | |
|---|---|---|
| 1. | Ripple in pass-band gain $A_p$ | < 1 dB |
| 2. | Minimum stop-band attenuation $A_{min}$ | 40 dB |
| 3. | Transition ratio = $f_a$ / $f_p$ | 1.1 |
| 4. | Cut-off frequency $f_c$ = clock frequency $f_{clk}/100$ | |
| | Pass-band edge $f_p$ = $0.009534 f_{clk}$ | |
| | Stop-band edge $f_a$ = $0.01048 f_{clk}$ | |

B. Electrical characteristics

| | | |
|---|---|---|
| 1. | Supply voltage $V^+ - V^-$ | ± 4V to ± 7V |
| 2. | Input voltage range (for ± 5V supply) | ± 3 V |
| 3. | Supply current drain | 50 mA tyvical |
| 4. | Clock frequency range | 500 kHz maximum |

### 6.2.2 Bessel low-pass filter

The specifications of the eighth order Bessel low-pass filter are as shown below.

A. Performance characteristics

1. Ripple in pass-band gain $A_p$ < 1 dB
2. Linear phase shift :

   Linearity upto pass-band edge ± 1 %

   Linbearity upto eight times the pass-band edge ± 2 %
3. Pass-band edge $f_p$ = clock frequency $f_{clk}/100$

   Cut-off frequency $f_c = 0.0316 f_{clk}$

   Stop-band edge $f_a = 0.1 f_{clk}$

The electrical characteristics are same as that of the elliptic filter.

### 6.2.3 Elliptic notch filter

The specifications of the second order elliptic notch filter are as shown below.

A. Performance characteristics

1. Ripple in pass-band gain $A_p$ < 1 dB
2. Minimum stop-band attenuation $A_{min}$ > 24 dB
3. Normalized pass-band bandwidth 0.1
4. Normalized stop-band bandwidth 0.02
5. Cut-off frequency $f_c$ = clock frequency $f_{clk}/100$

Notch frequency $f_n = 0.0099\ f_{clk}$

Pass-band edges $f_{p1} = 0.00953 f_{clk}$

$f_{p2} = 0.01048 f_{clk}$

The electrical characteristics are same as that of the elliptic filter.

## 6.3 I/O EXPANSION UNIT

The I/O expansion unit consists of the I/O expansion block and a programmable timer interface block.

The specifications of the I/O expansion unit are as shown below.

A. Performance characteristics

| | | |
|---|---|---|
| 1. | No. of multiplexer input channels | 4 |
| 2. | No. of demultiplexer output channels | 4 |
| 3. | Programmable clock generator : | |
| | No. of channels | 3 |
| | Programmable range | 1 kHz to 500 kHz |
| | Step size | 40 Hz |

B. Electrical characteristics

| | | | |
|---|---|---|---|
| 1. | Operating supply voltage | $V_{DD}$ | + 5 V |
| | | $V_{SS}$ | 0 V |
| | | $V_{EE}$ | - 5 V |
| 2. | Input voltage range | | ± 3 V |
| 3. | Supply current drain | | 200 mA typical |

## 6.4 SUMMARY

The PCBs developed are assembled in an aluminum box of dimensions, width = 30 cms., depth = 27 cms., and height = 15 cms. The I/O expansion unit, two elliptic filters, two Bessel filters, and one notch filter, are assembled as plug-in modules, with separate front-panel for each module.

Some examples, such as band-pass filters for four channels, cross-correlation technique for system impulse response characterization, *etc.* can be worked out using the system developed.

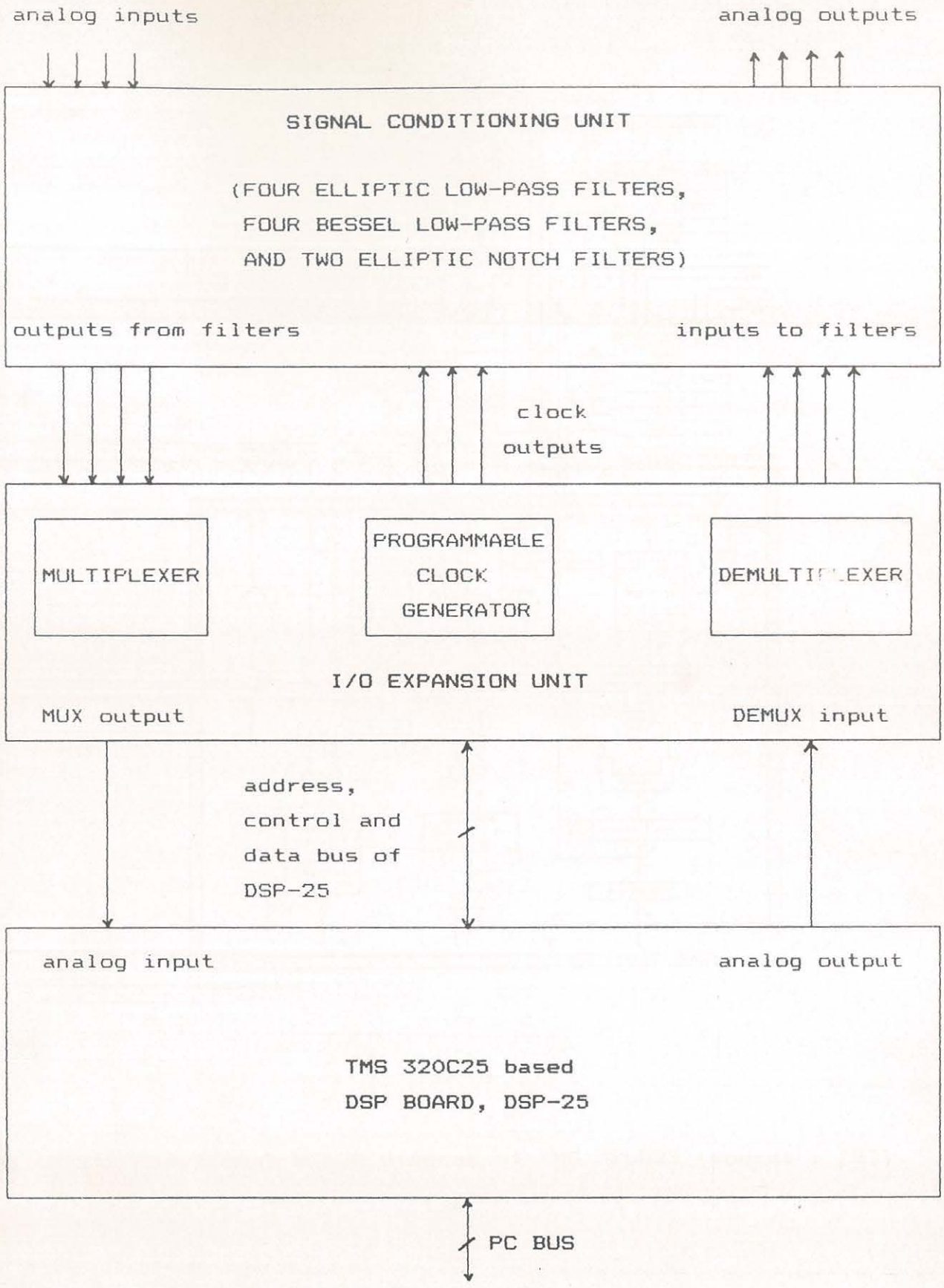



Fig. 2.1 Block diagram of data acquisition system.

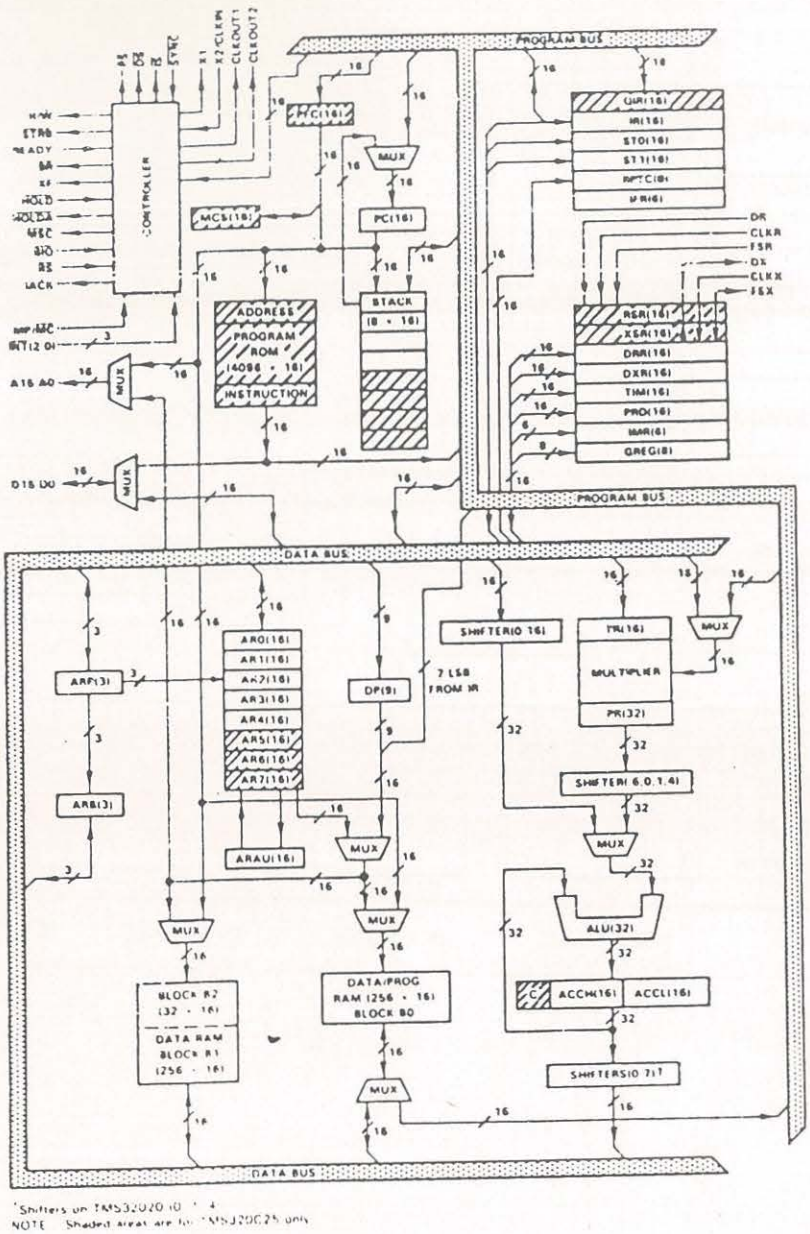



Fig. 2.2. Functional block diagram of TMS 320C25 (source : [8]).

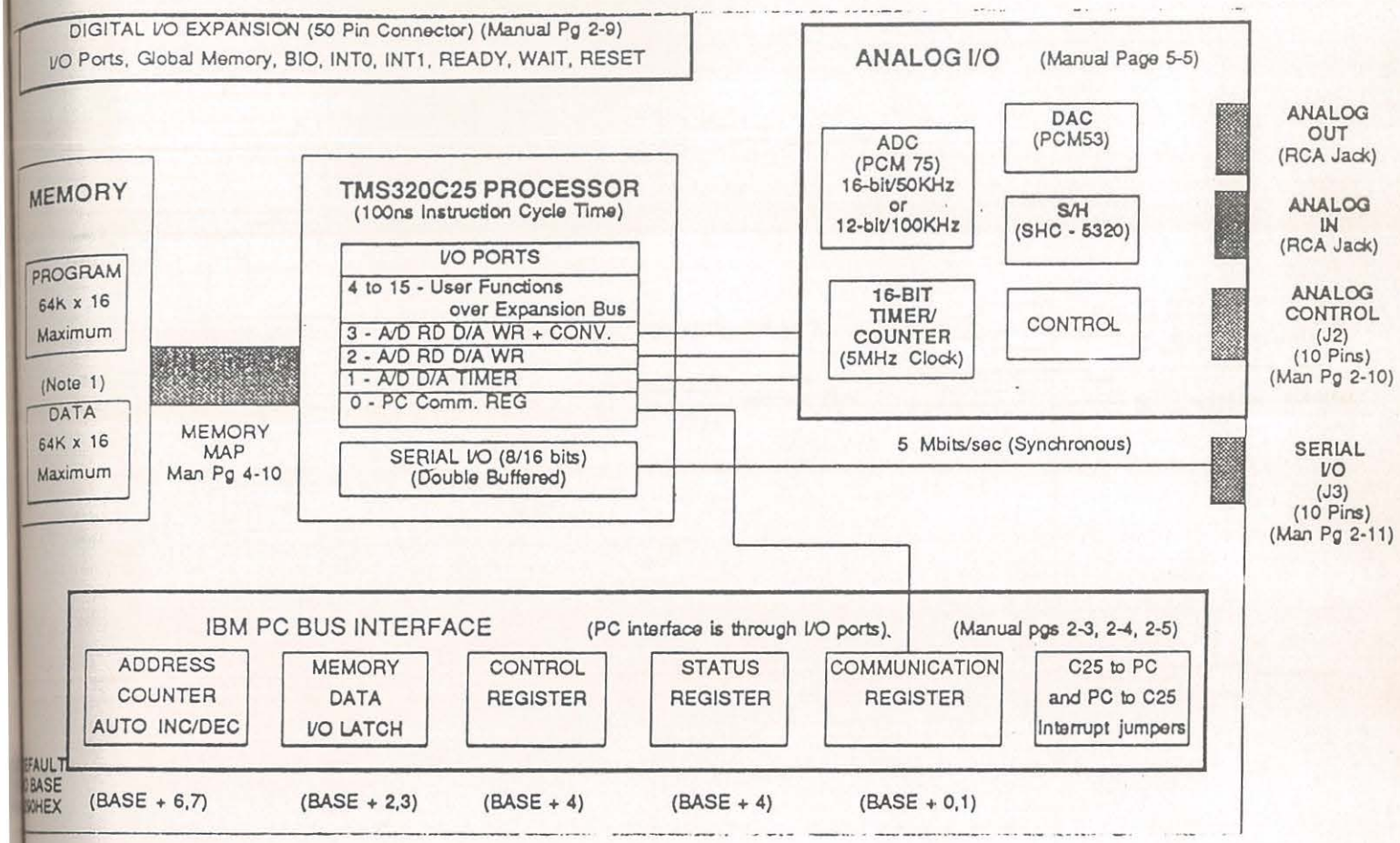



Fig. 2.3. Block diagram of the DSP board PCL-DSP25 (source : [9])

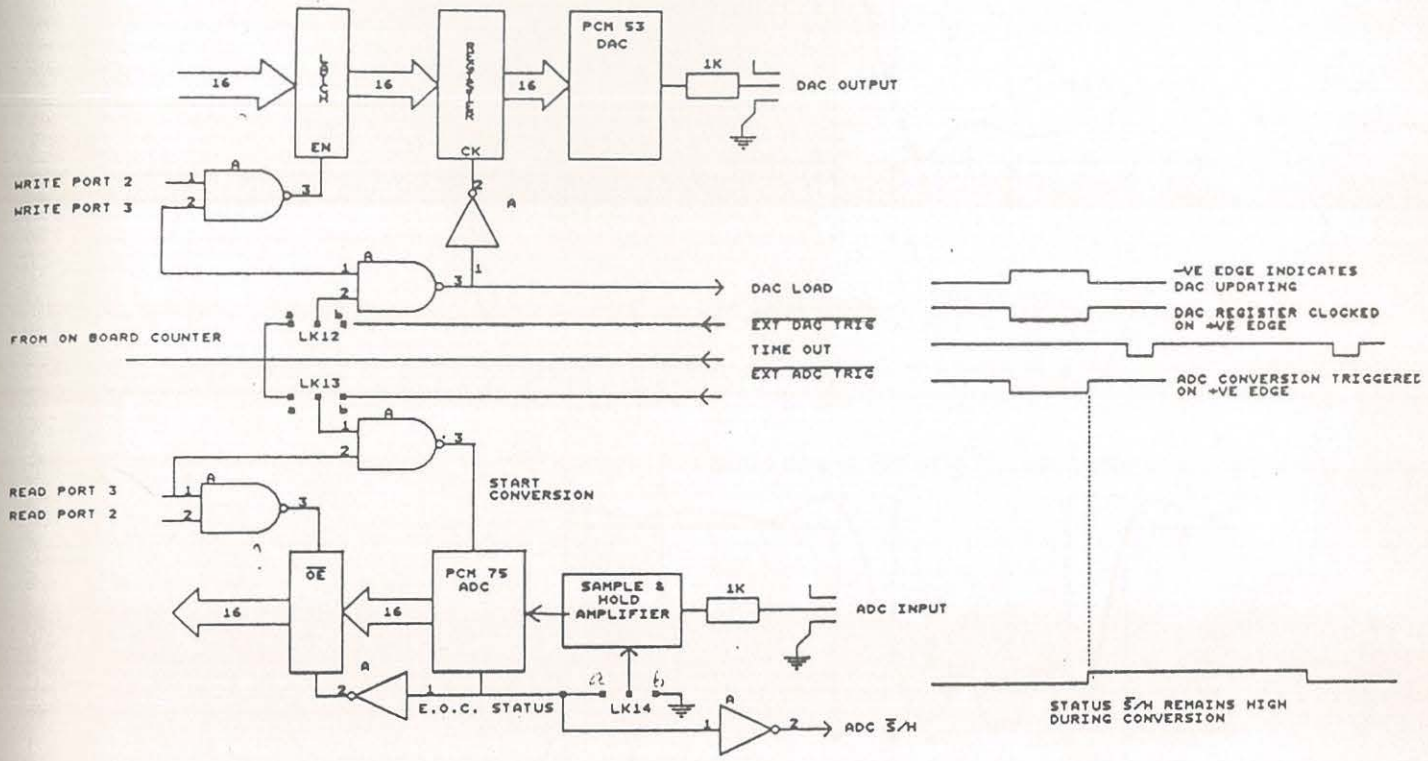
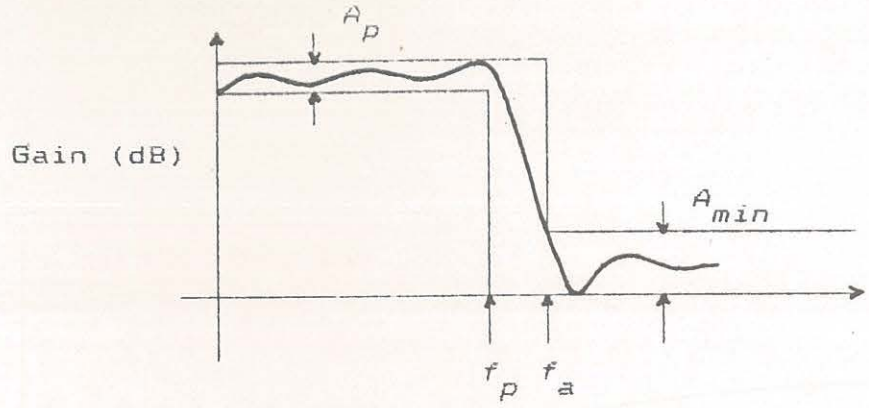
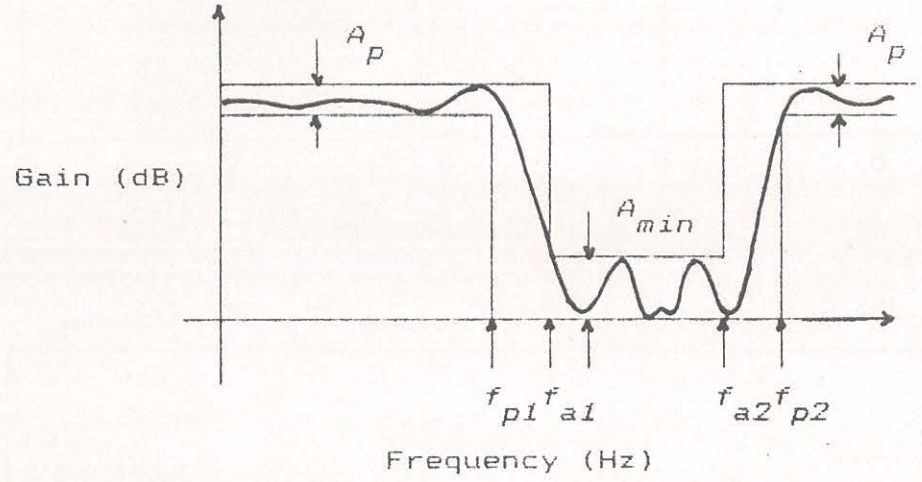



Fig. 2.4. Schematic of analog I/O interface on the DSP board PCL-DSP25 (source : [9]).



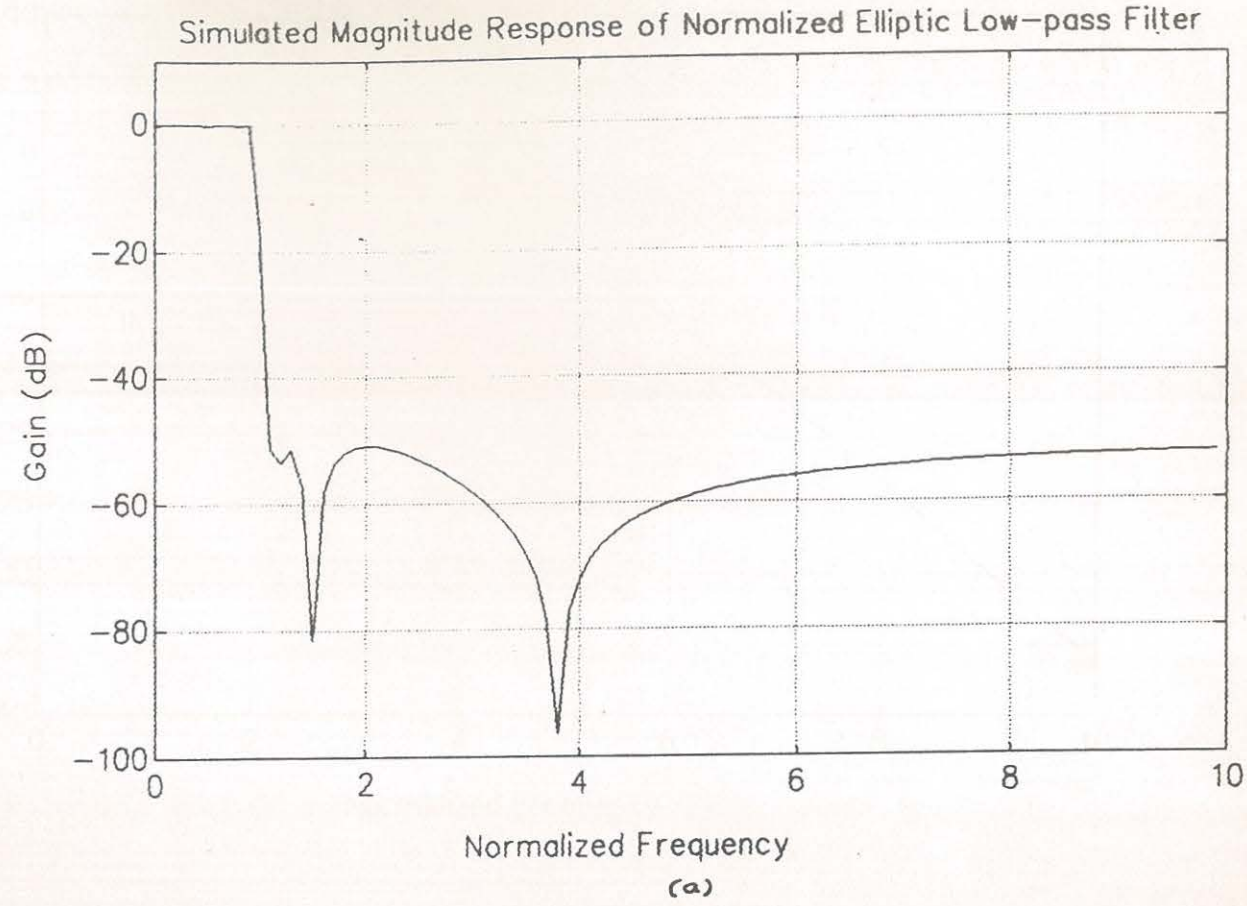

(a)



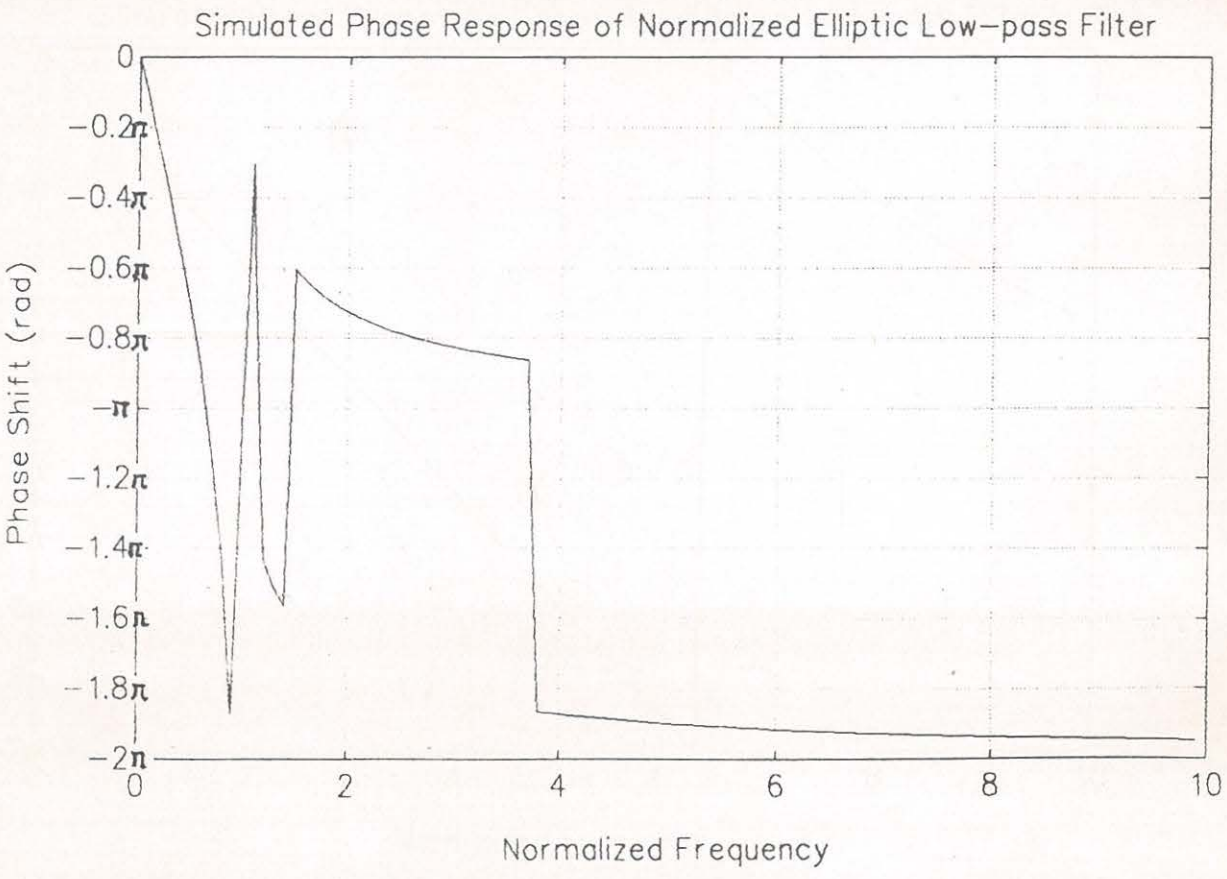

(b)

$A_p$ - Maximum allowable pass-band ripple (dB)
$A_{min}$ - Minimum allowable stop-band attenuation (dB)
$f_p$ - Pass-band edge (Hz) for a low-pass filter
$f_a$ - Stop-band edge (Hz) for a low-pass filter
$f_{p1}$, $f_{p2}$ - Pass-band edges for a notch filter
$f_{a1}$, $f_{a2}$ - Stop-band edges for a notch filter

Fig. 2.5. Magnitude response specifications of : (a) low-pass filter, (b) notch filter.

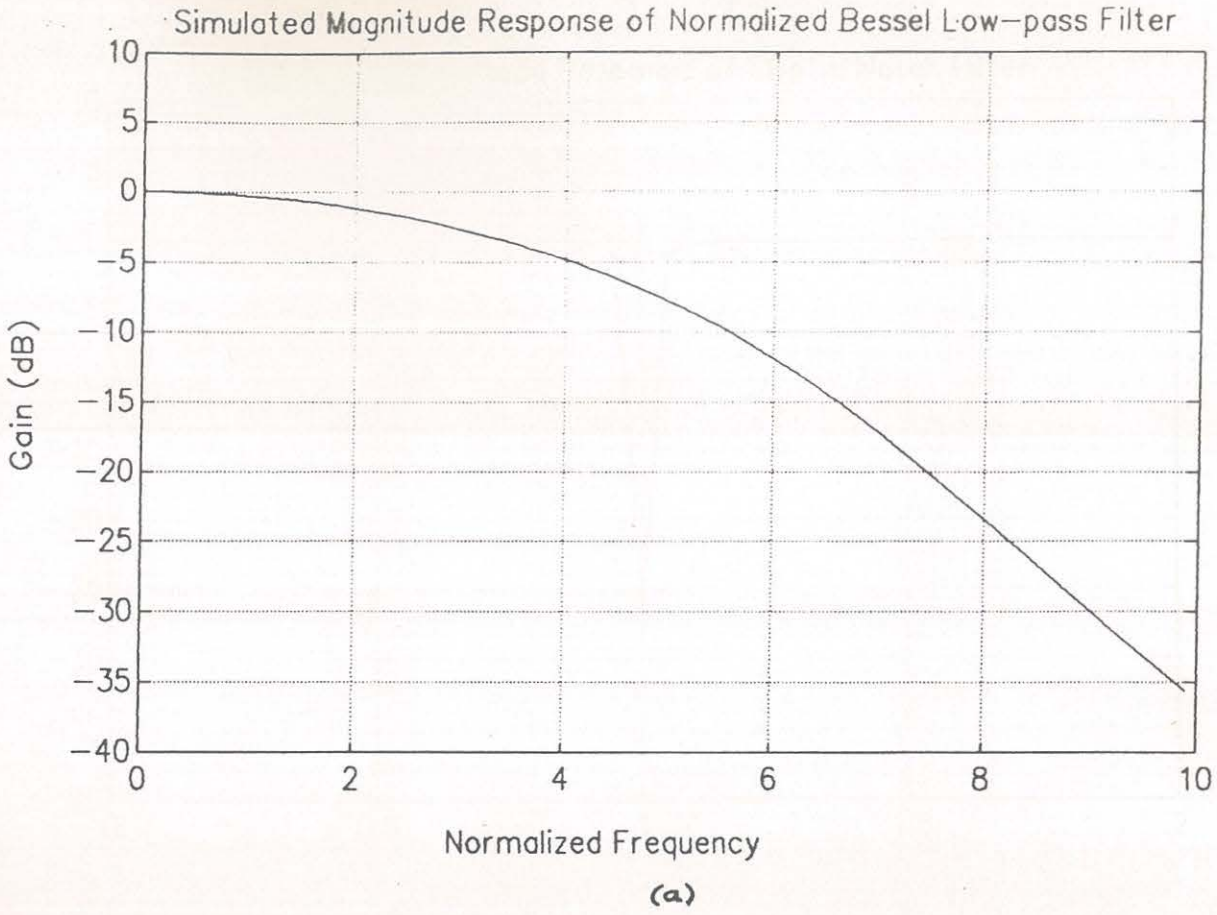



(a)

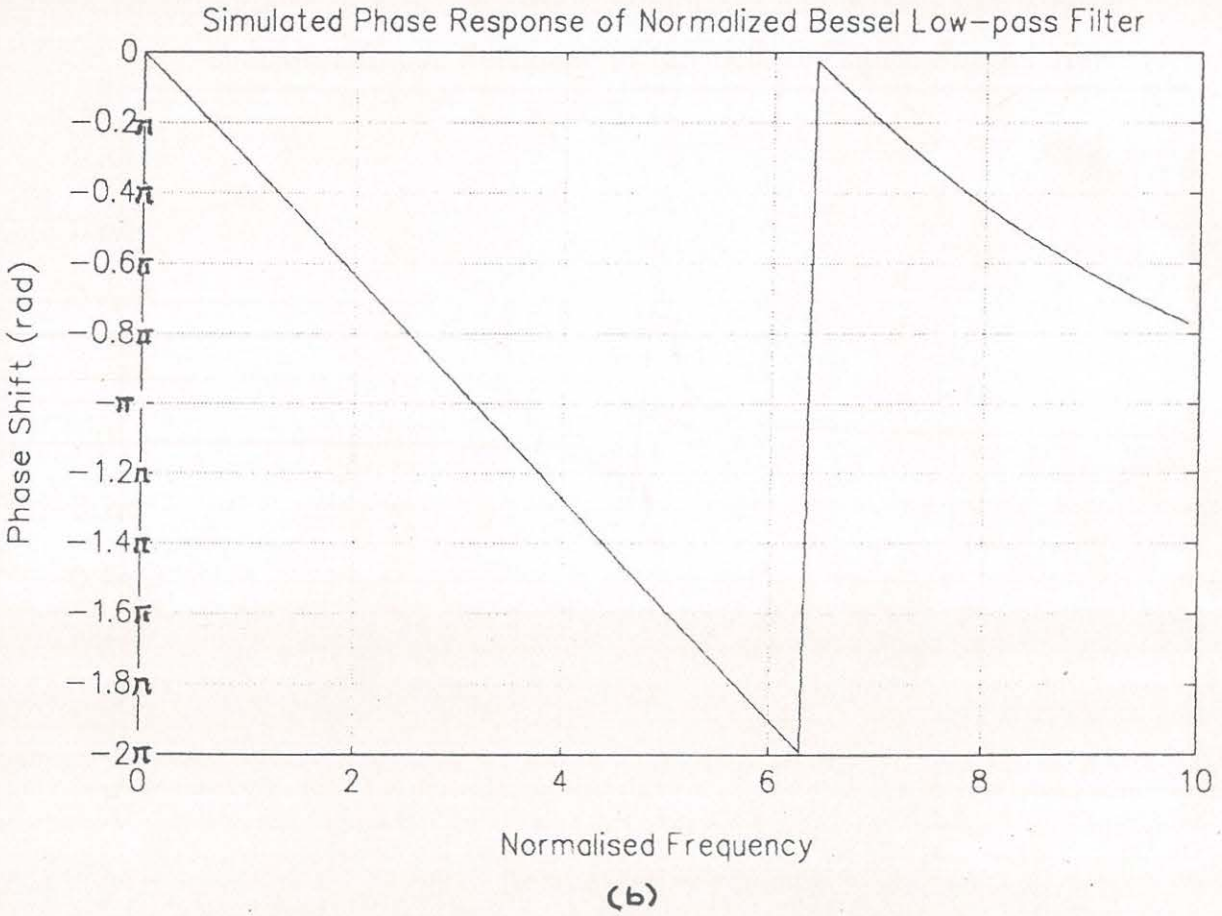



(b)

Fig. 2.6. Frequency response of eighth order elliptic low-pass filter : (a) magnitude response, (b) phase

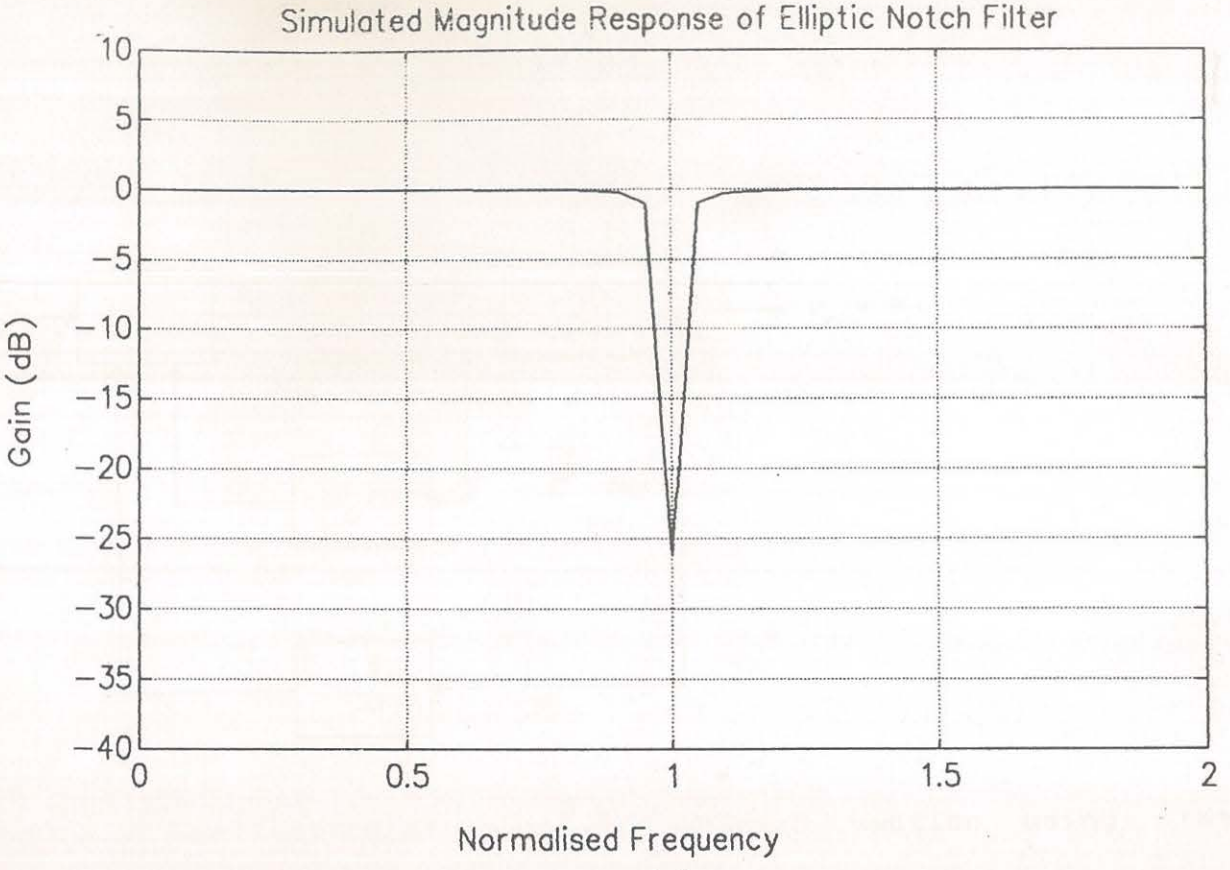



(a)

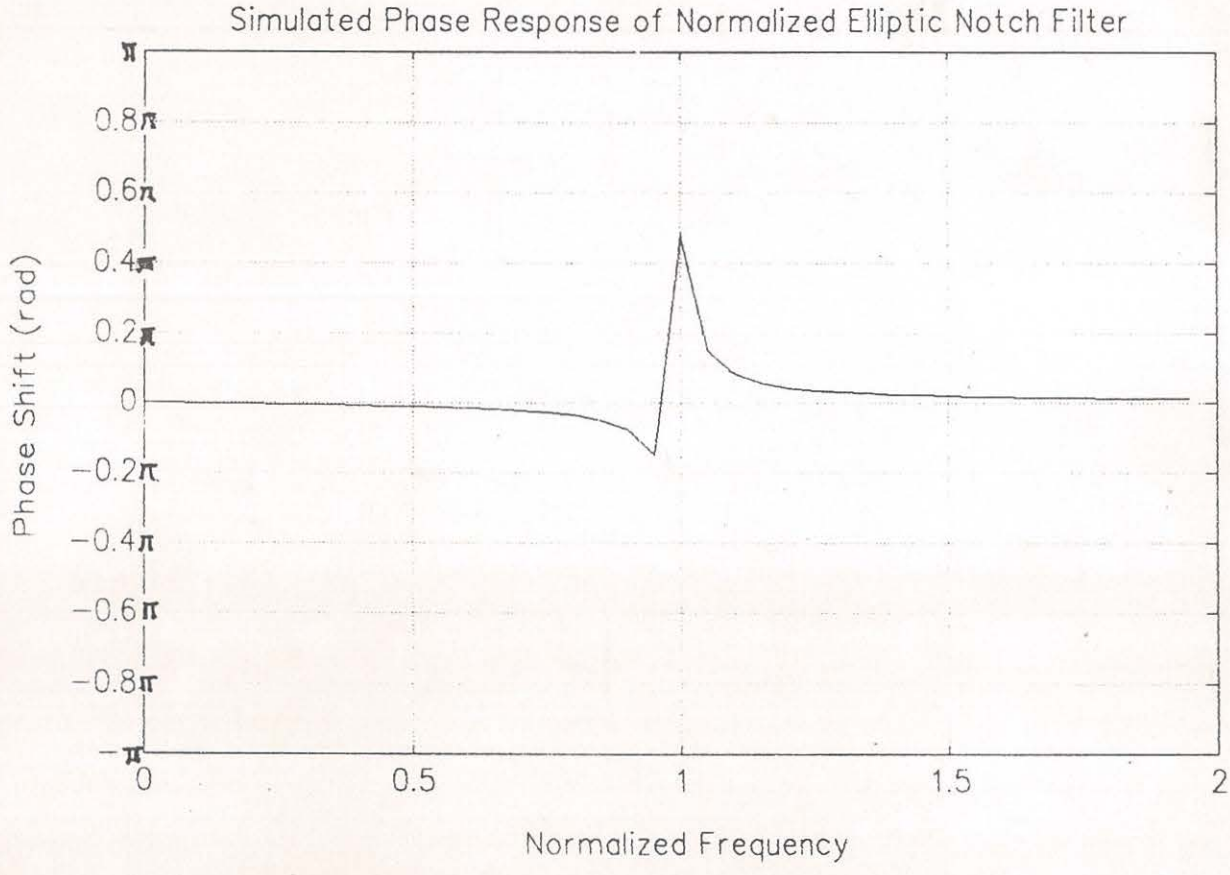



(b)

Fig. 2.7. Frequency response of eighth order Bessel low-pass filter : (a) magnitude response, (b) phase response.




(a)




(b)

Fig. 2.8. Frequency response of second order elliptic notch filter : (a) magnitude response, (b) phase response.

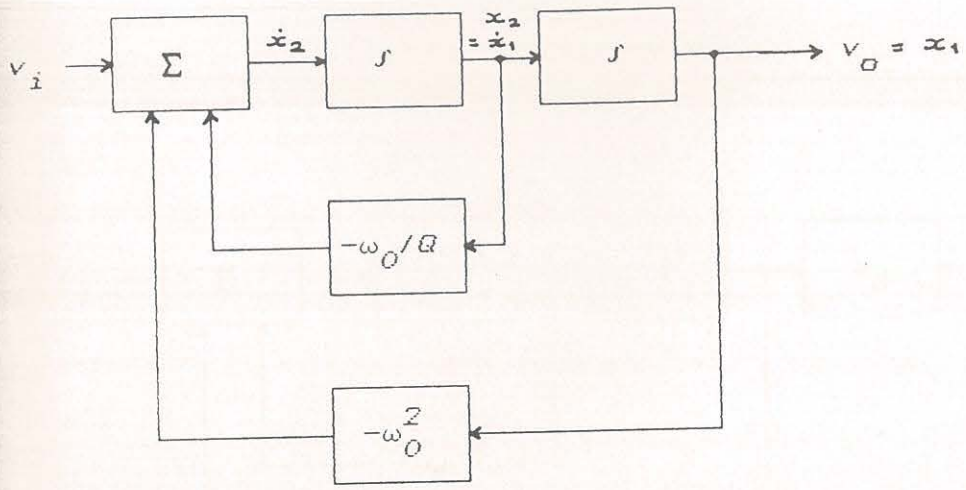



Fig. 3.1 Realization of an all-pole biquad section using state variable feedback.

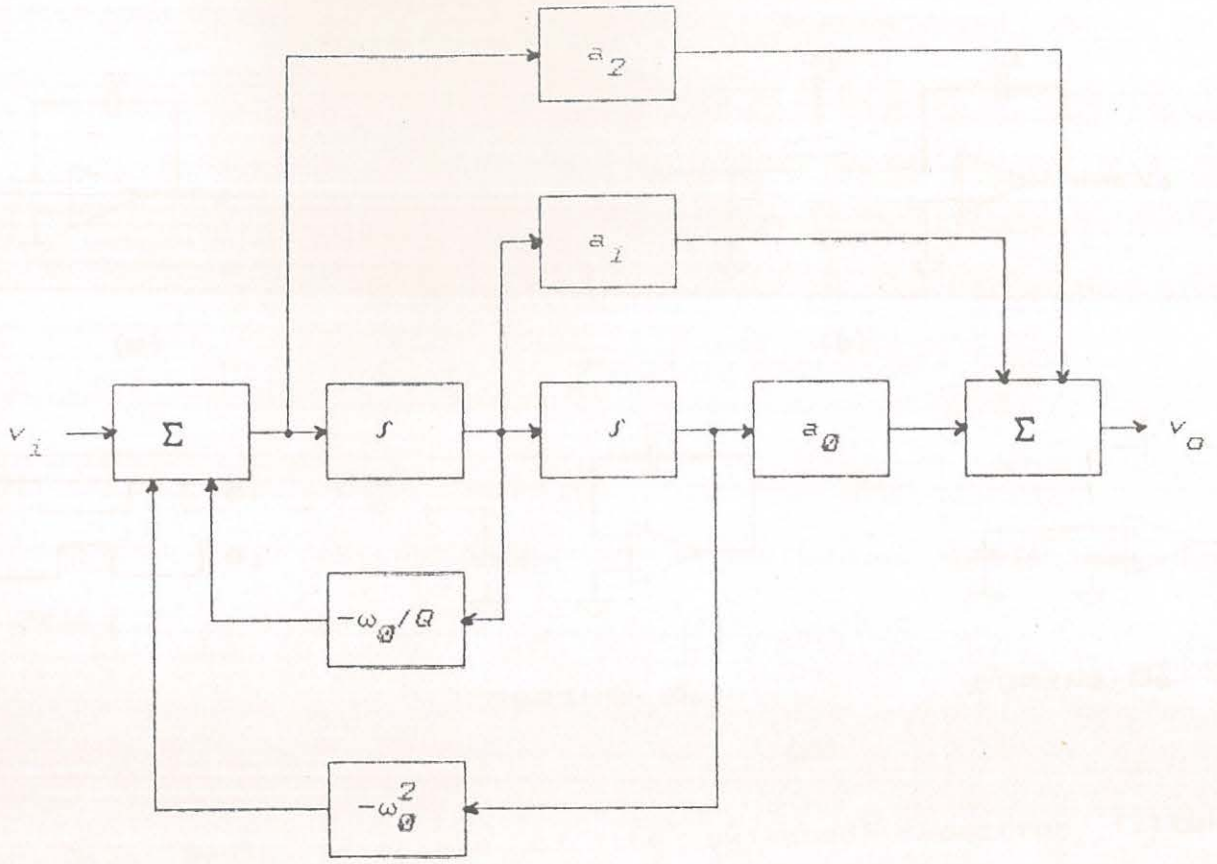



Fig. 3.2. Realization of a pole-zero biquad section using state variable feedback.

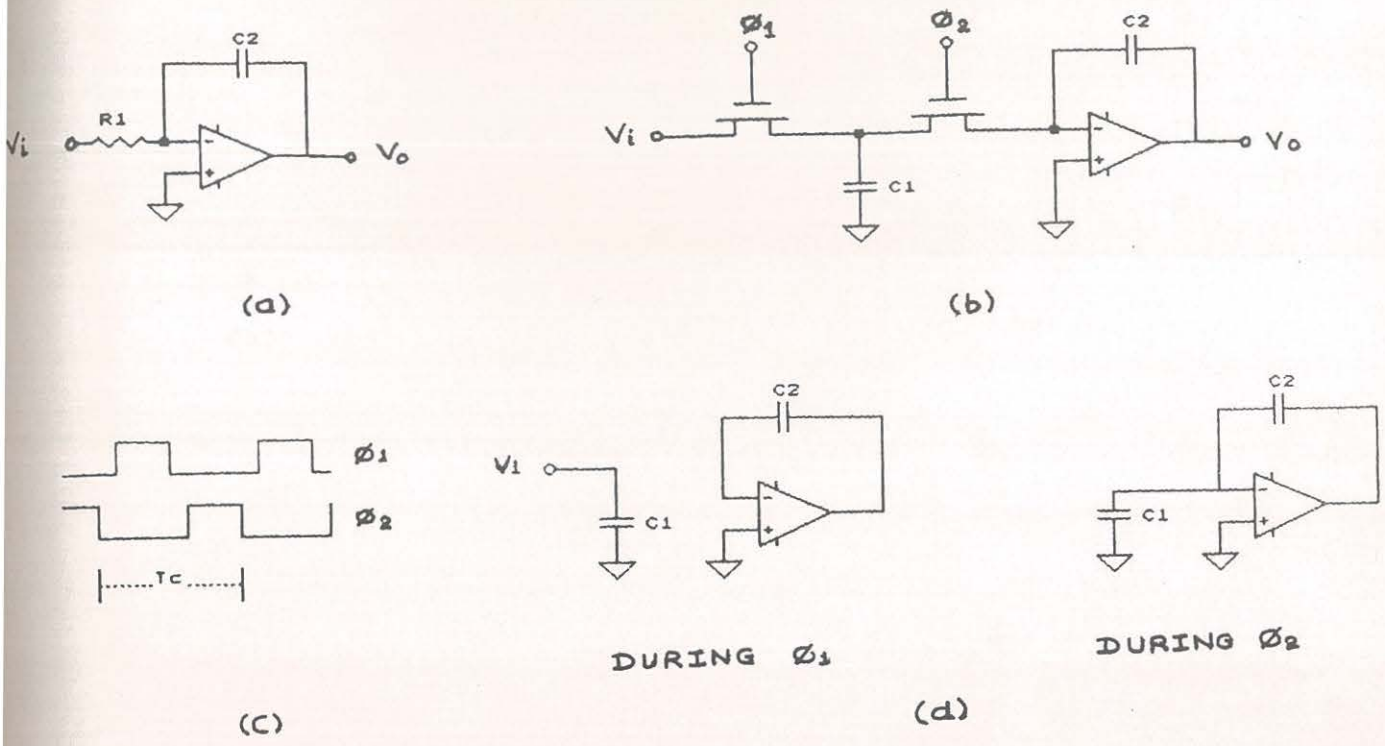



Fig. 3.3. Basic principle of the switched capacitor filter technique for an inverting integrator : (a) active-*RC* integrator, (b) switched capacitor integrator, (c) two-phase clock (nonoverlapping), (d) during $\phi_1$, $C_1$ charges up to the current value of $V_i$ and then, during $\phi_2$, discharges into $C_2$.

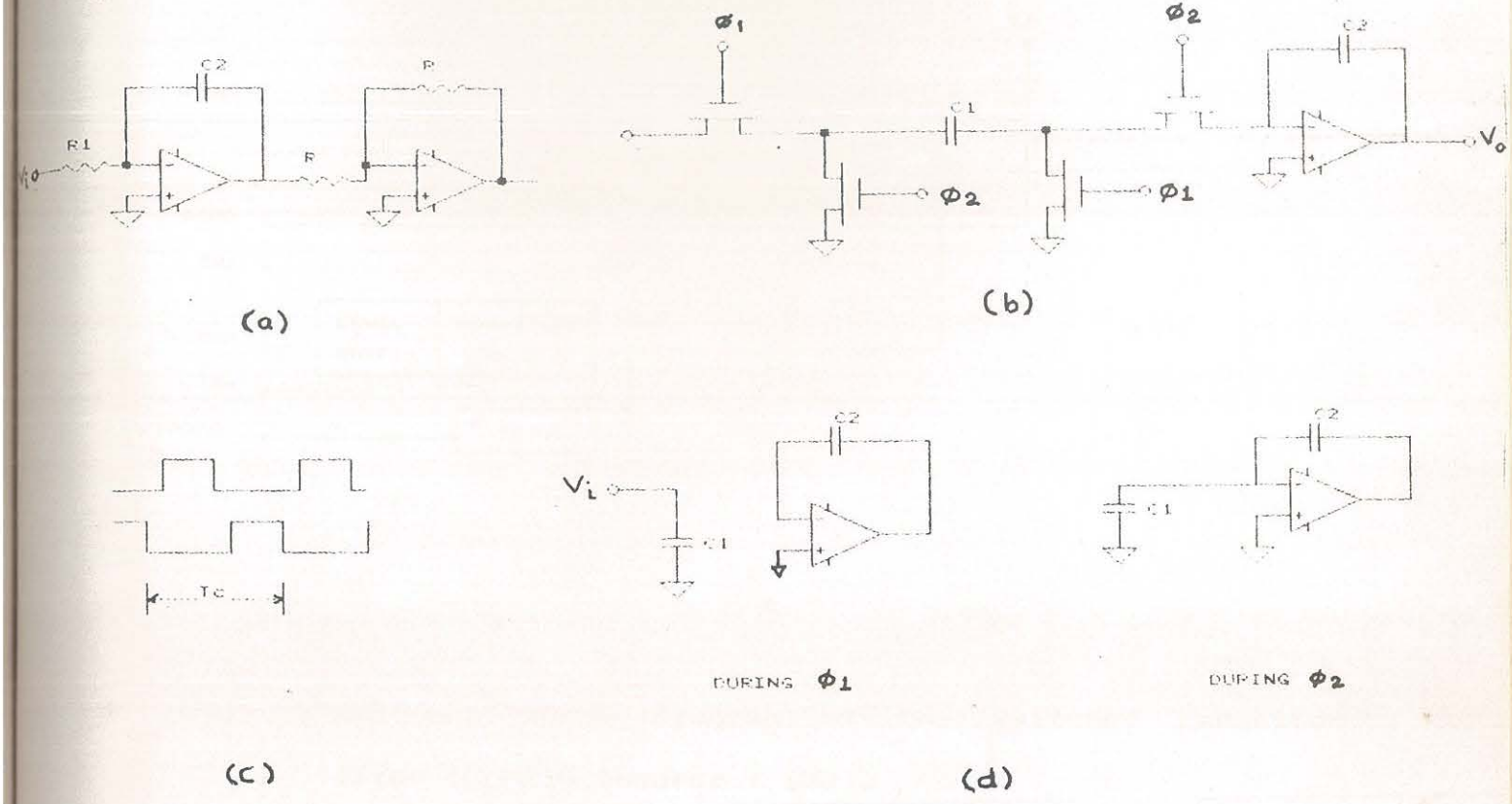



Fig. 3.4. Basic principle of the switched capacitor filter technique for a non-inverting integrator : (a) active-*RC* integrator, (b) switched capacitor integrator, (c) two-phase clock (nonoverlapping), (d) during $\phi_1$, $C_1$ charges up to the current value of $V_i$ and then, during $\phi_2$, discharges into $C_2$.

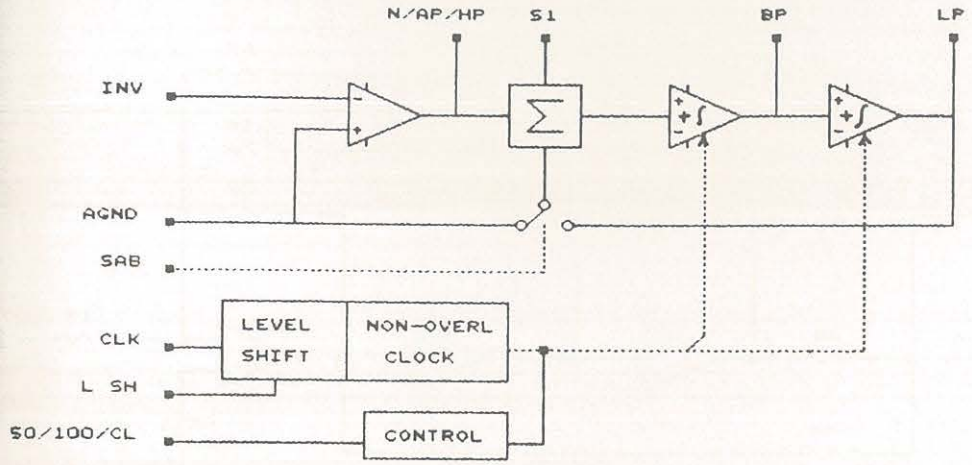



Fig. 3.5. Functional block diagram of the switched capacitor filter IC MF10 (source : [16]).

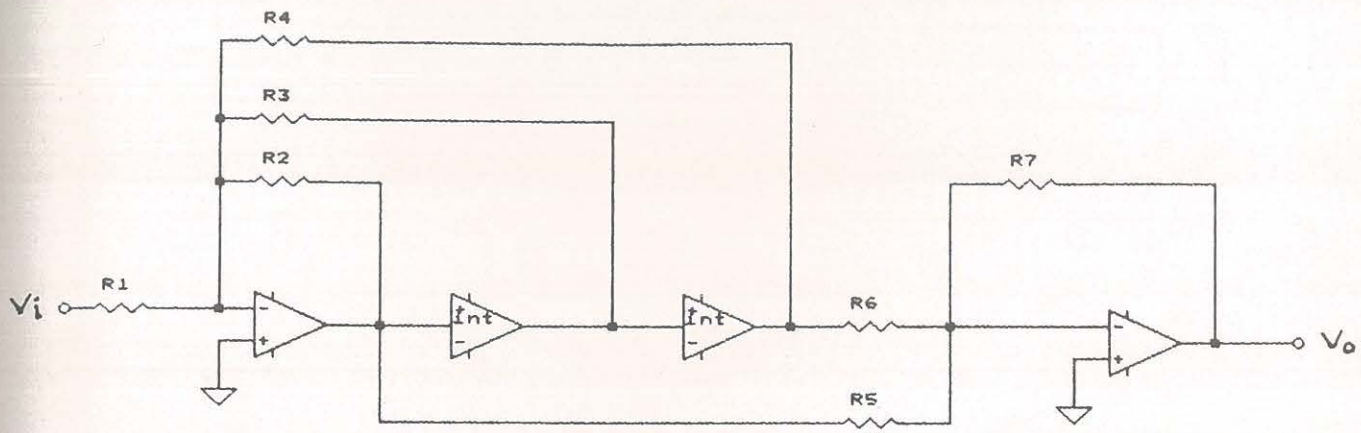
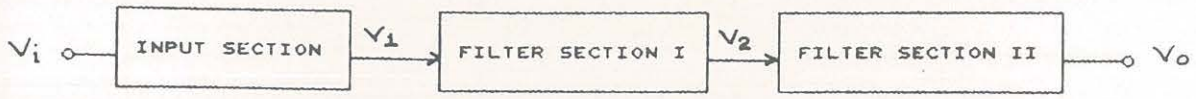
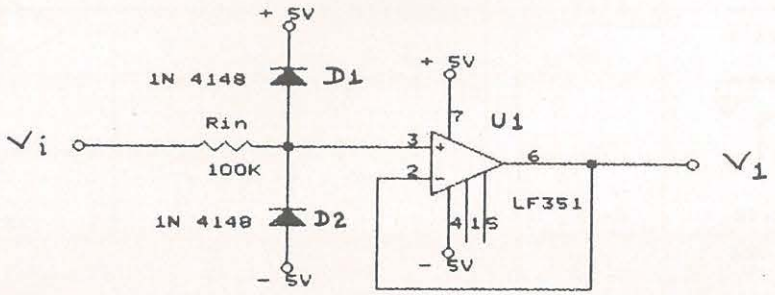



Fig. 3.6. Biquad realization using switched capacitor filter IC MF 10.

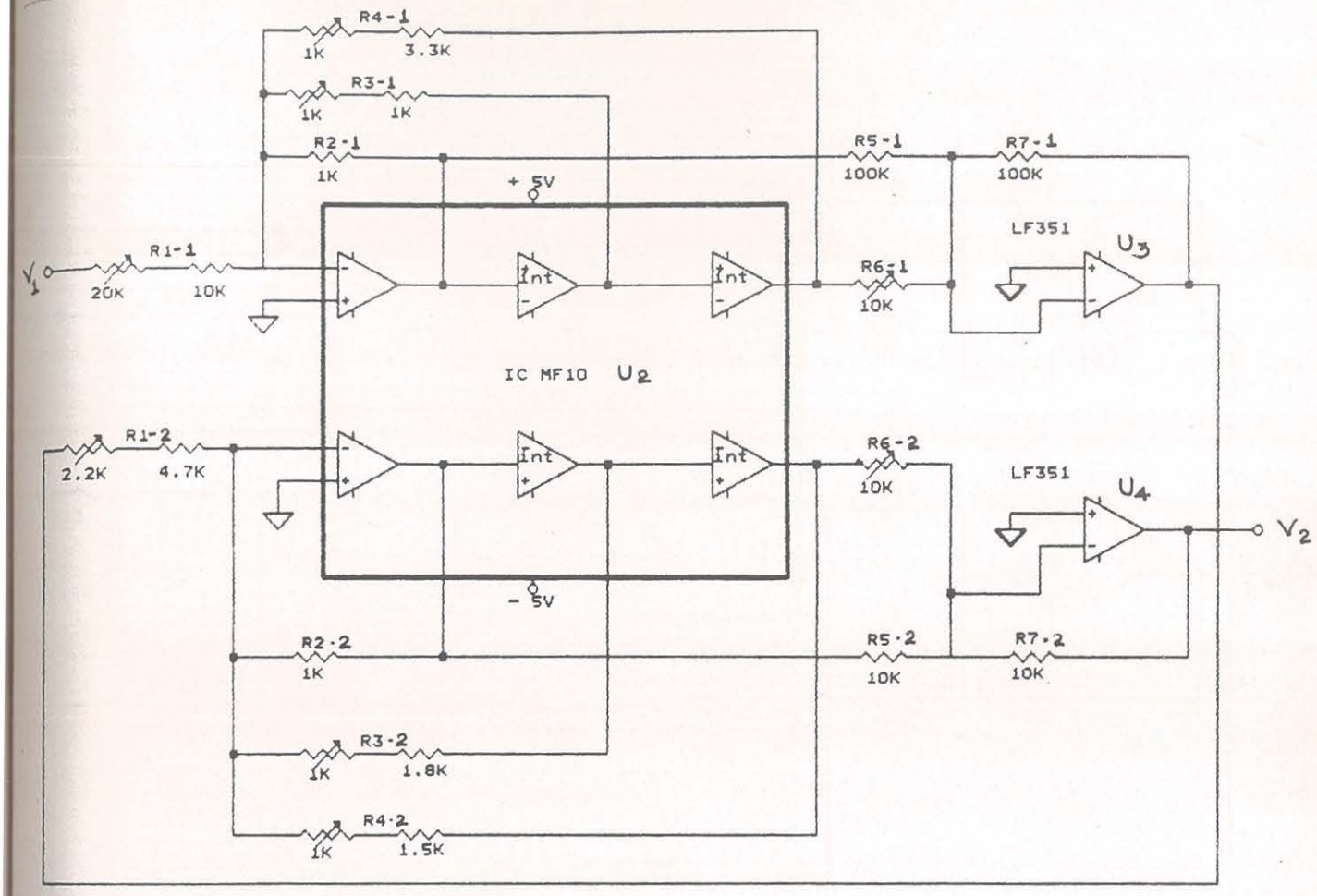



(a)

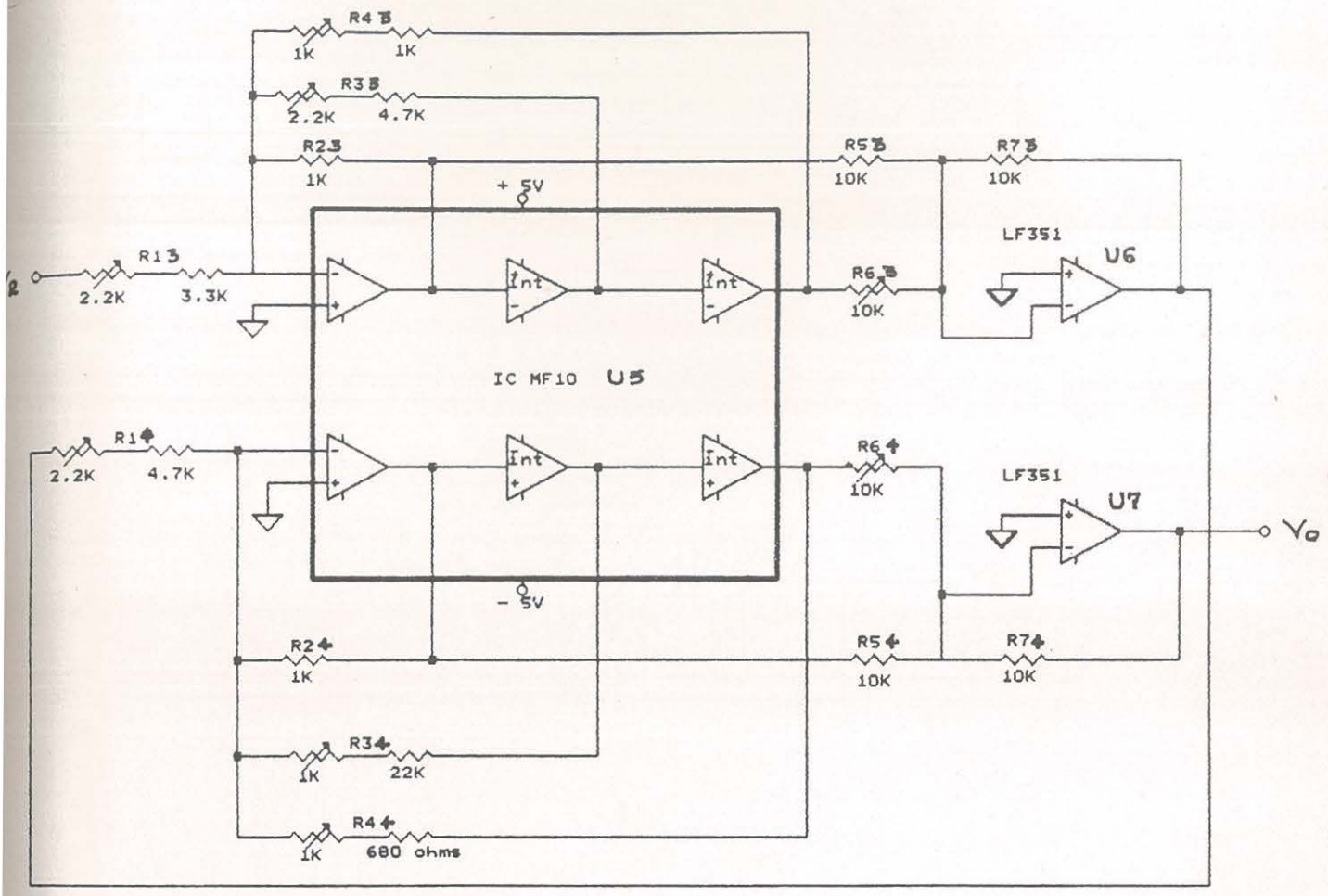



(b)

Fig. 3.7. Circuit schematic of the eighth order elliptic low-pass filter : (a) block diagram, (b) input section, (Contd.)...

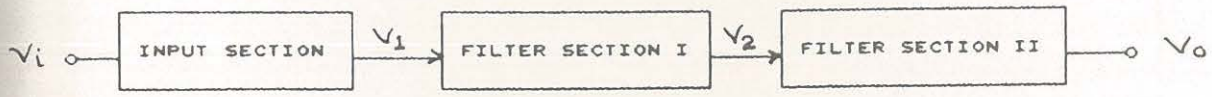

R4-1
1K
3.3K
R3-1
1K
1K
R2-1
1K
+ 5V
R5-1
100K
R7-1
100K
LF351
U3
V1
R1-1
20K
10K
Int
Int
R6-1
10K
IC MF10 U2
R1-2
2.2K
4.7K
Int
Int
R6-2
10K
LF351
U4
V2
- 5V
R2-2
1K
R5-2
10K
R7-2
10K
R3-2
1K
1.8K
R4-2
1K
1.5K

(C)

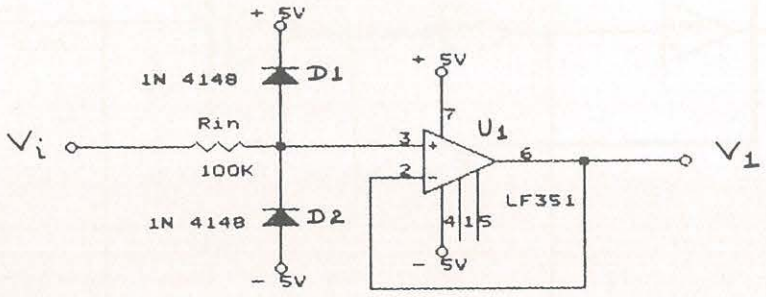



(d)

Fig. 3.7 (c) filter section I, (d) filter section II. (contd.)

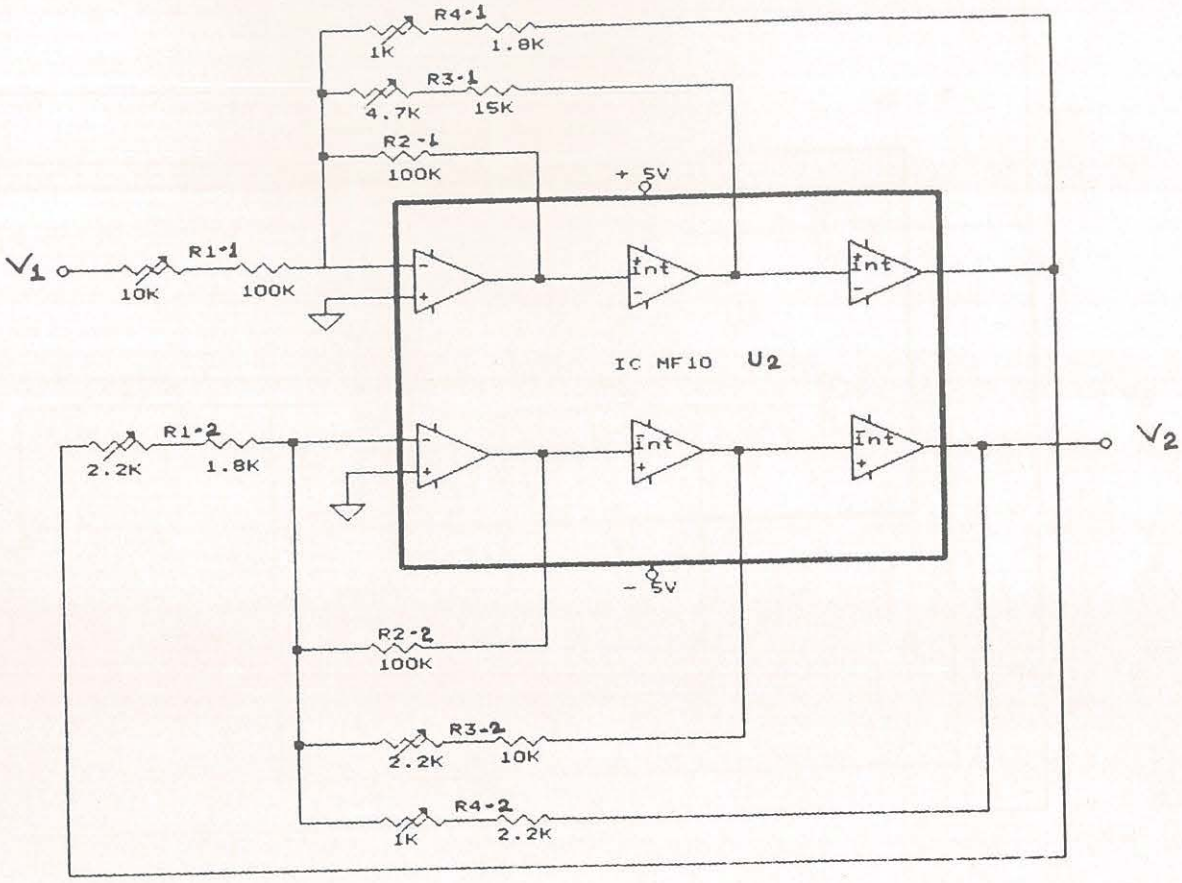



(a)

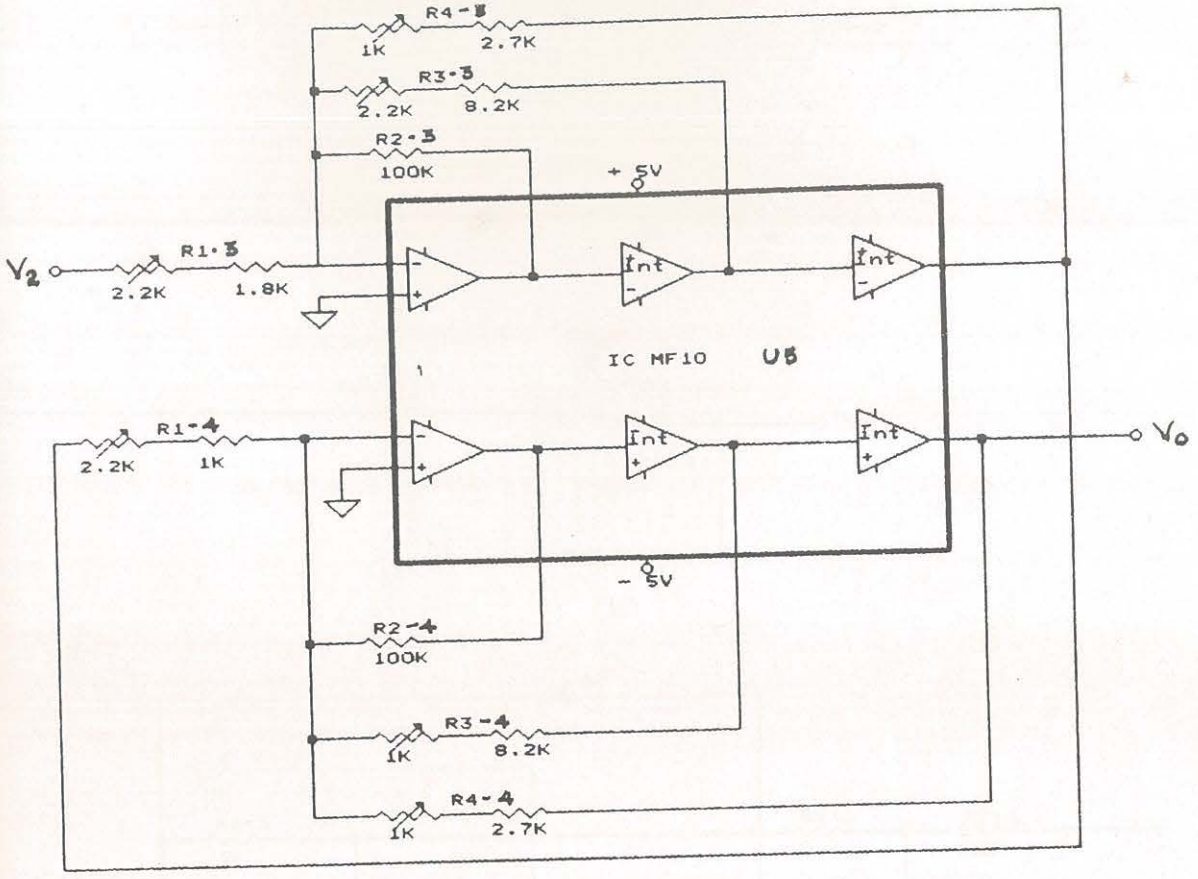



(b)

Fig. 3.8. Circuit schematic of the eighth order Bessel low-pass filter : (a) block diagram, (b) input section, (contd.)...


R4-1
1K
1.8K
R3-1
4.7K
15K
R2-1
100K
+ 5V
V1
R1-1
10K
100K
Int
Int
IC MF10 U2
R1-2
2.2K
1.8K
Int
Int
V2
- 5V
R2-2
100K
R3-2
2.2K
10K
R4-2
1K
2.2K

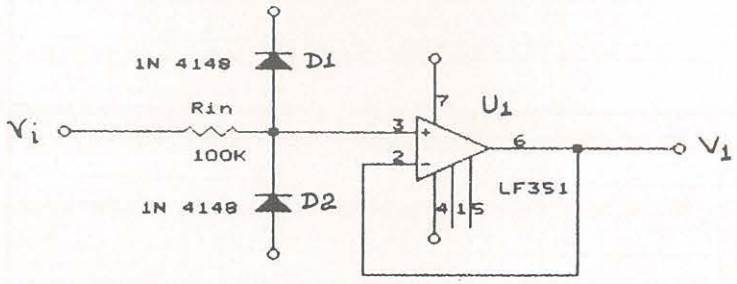
(C)



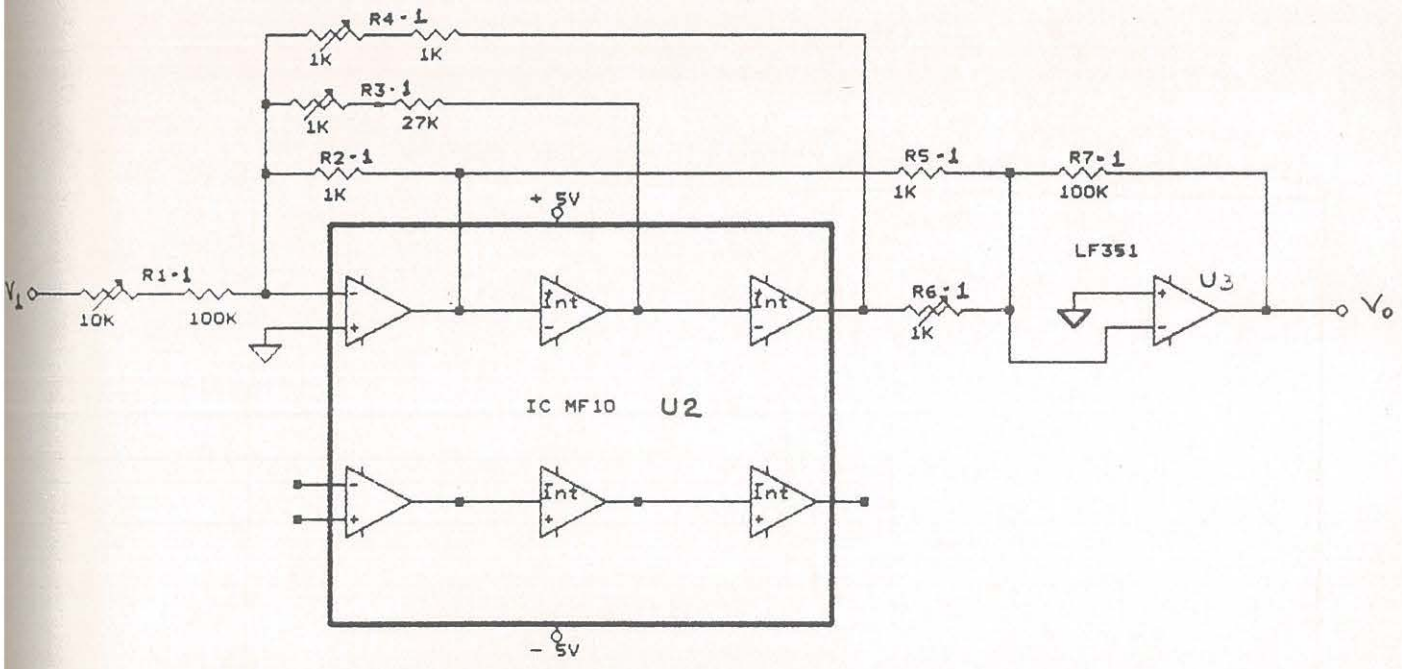

(d)

Fig. 3.8. (c) filter section I (d) filter section II. (contd.)


(a)

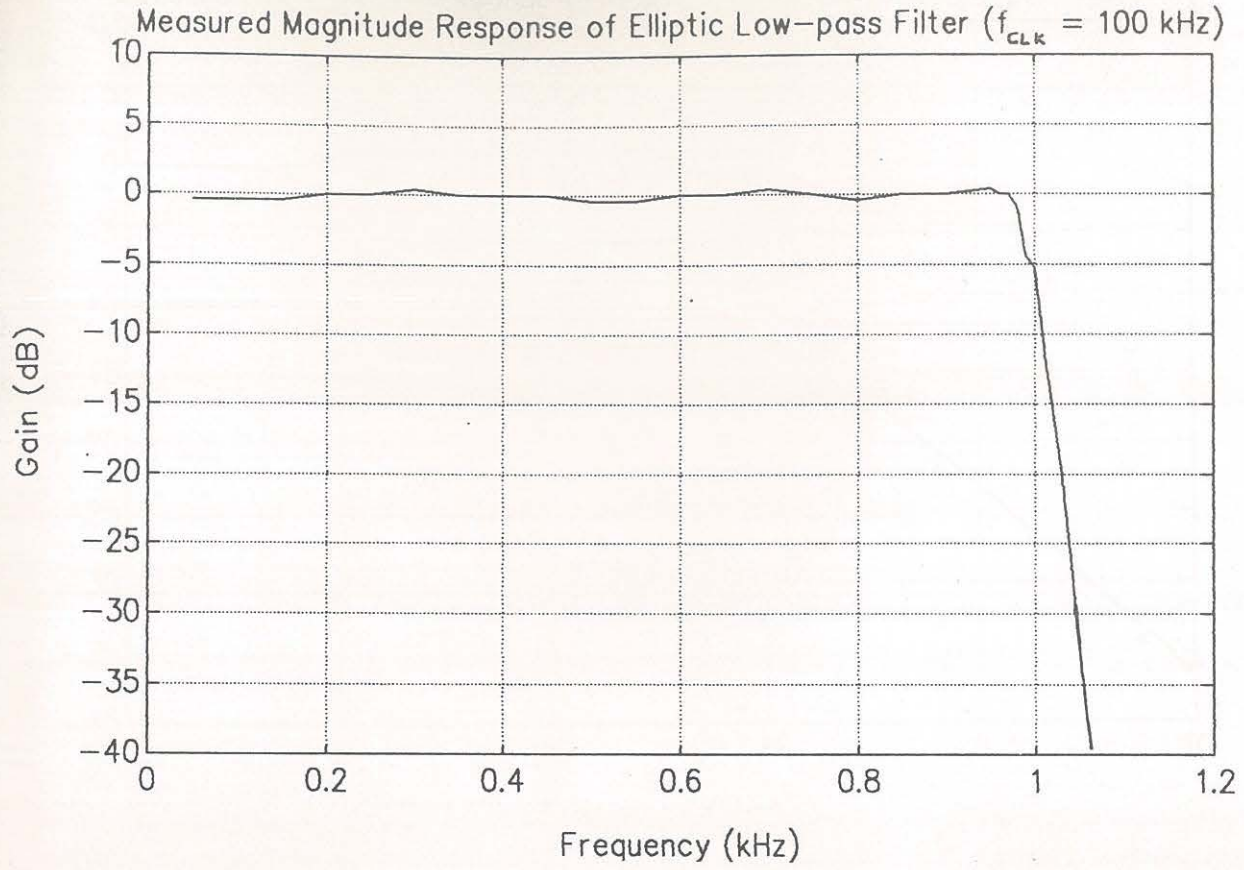



(b)




(c)

Fig. 3.9. Circuit schematic of the second order elliptic notch filter : (a) block diagram, (b) input section, (c) filter section.



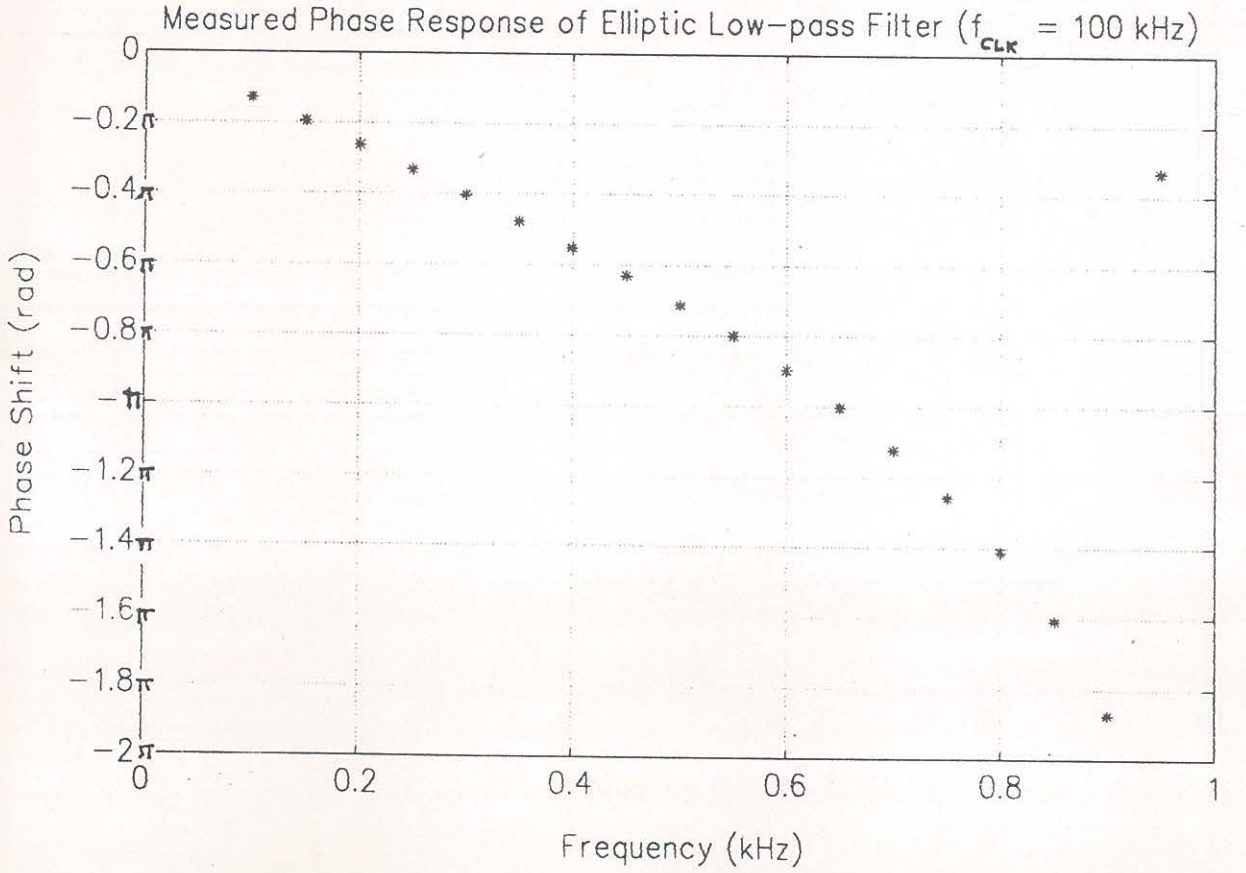
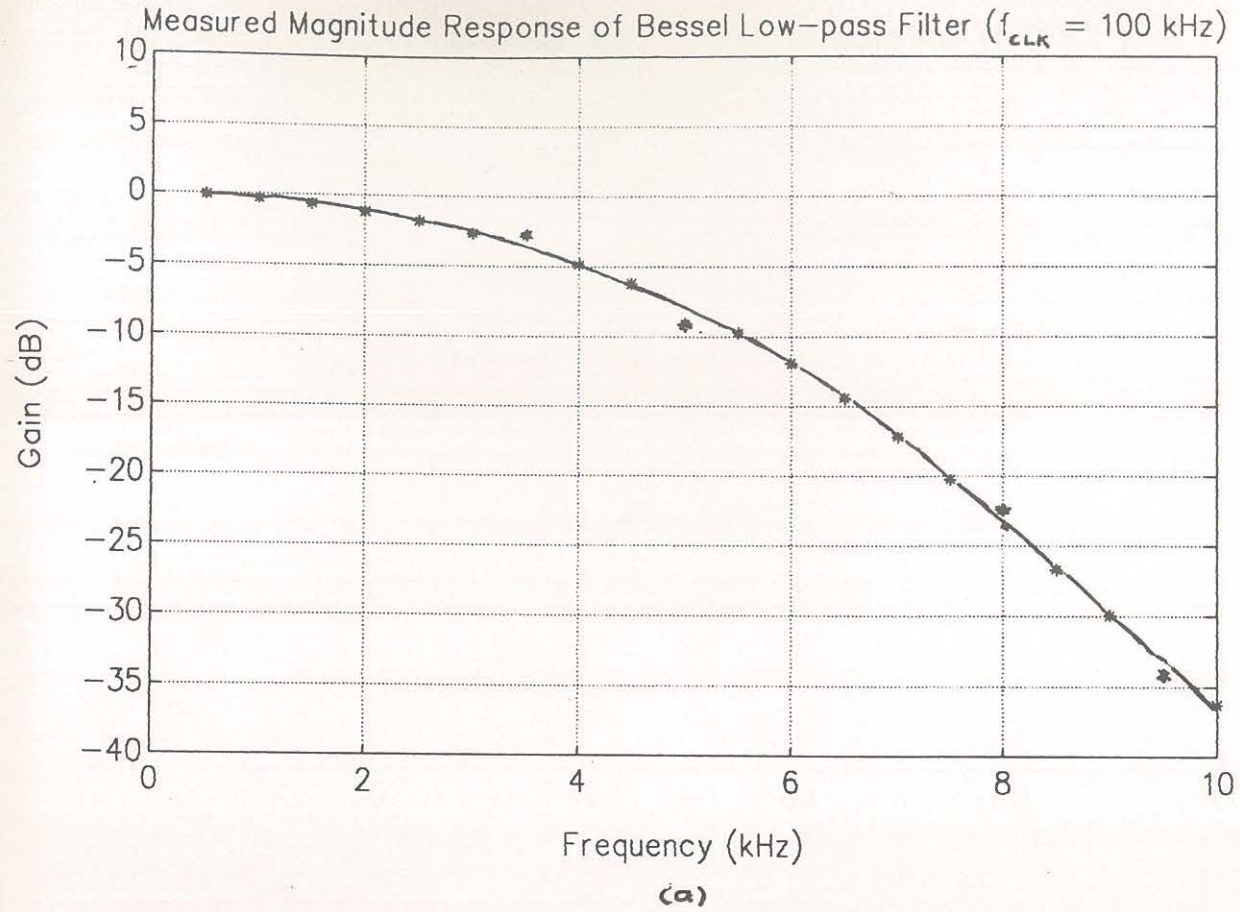
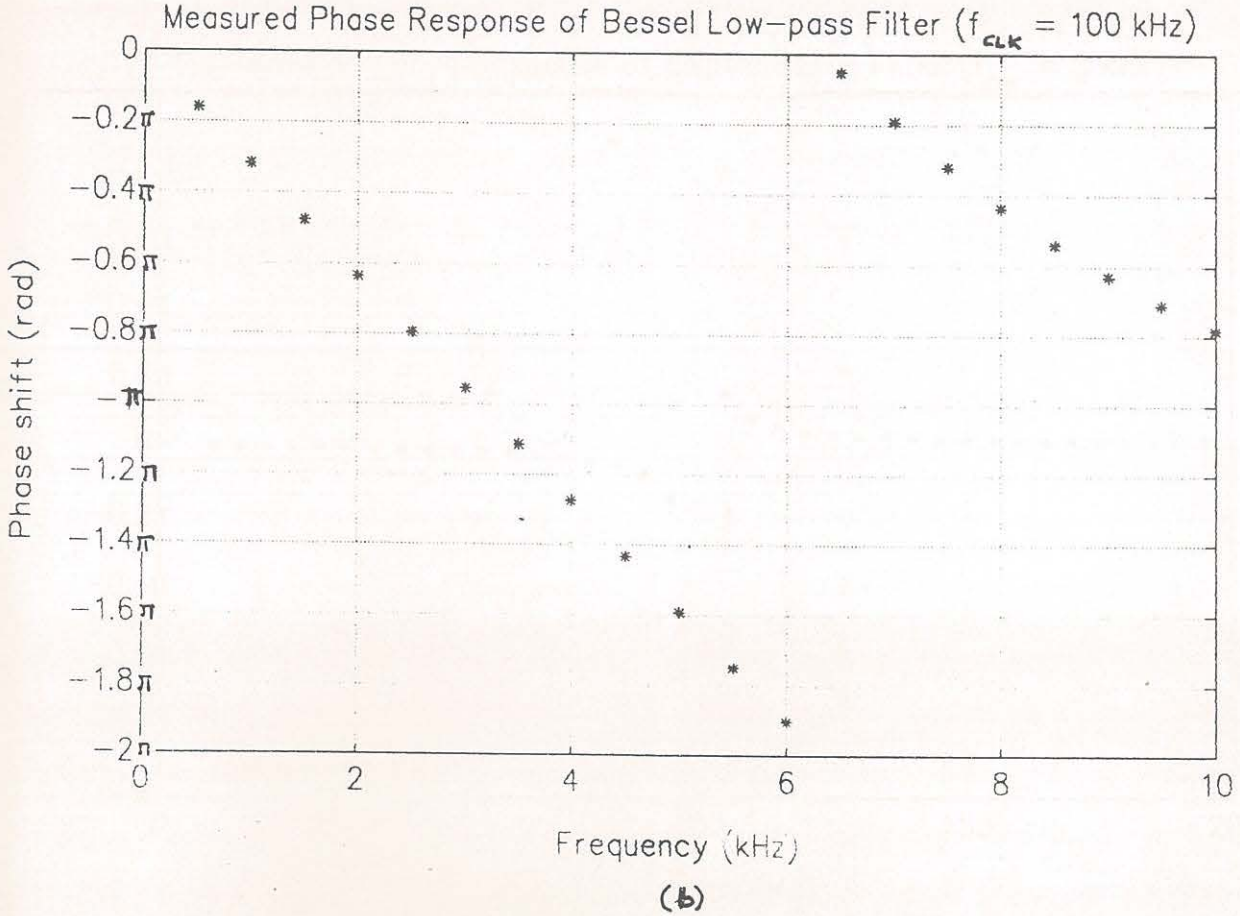




Fig. 3.10. Measured frequency response of eighth order elliptic low-pass filter : (a) magnitude response, (b) phase response.

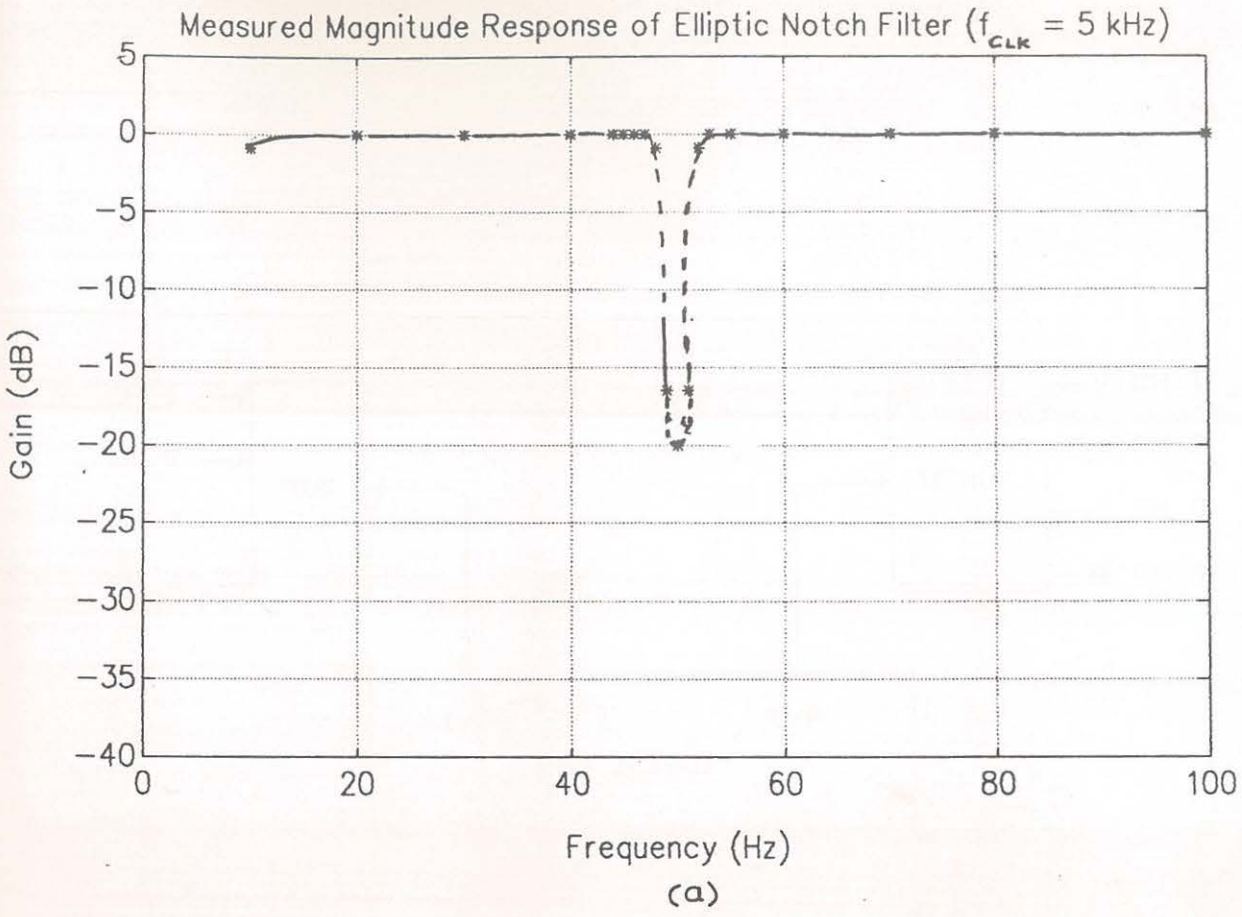



(a)




(b)

Fig. 3.11. Measured frequency response of eighth order Bessel low-pass filter : (a) magnitude response, (b) phase response.



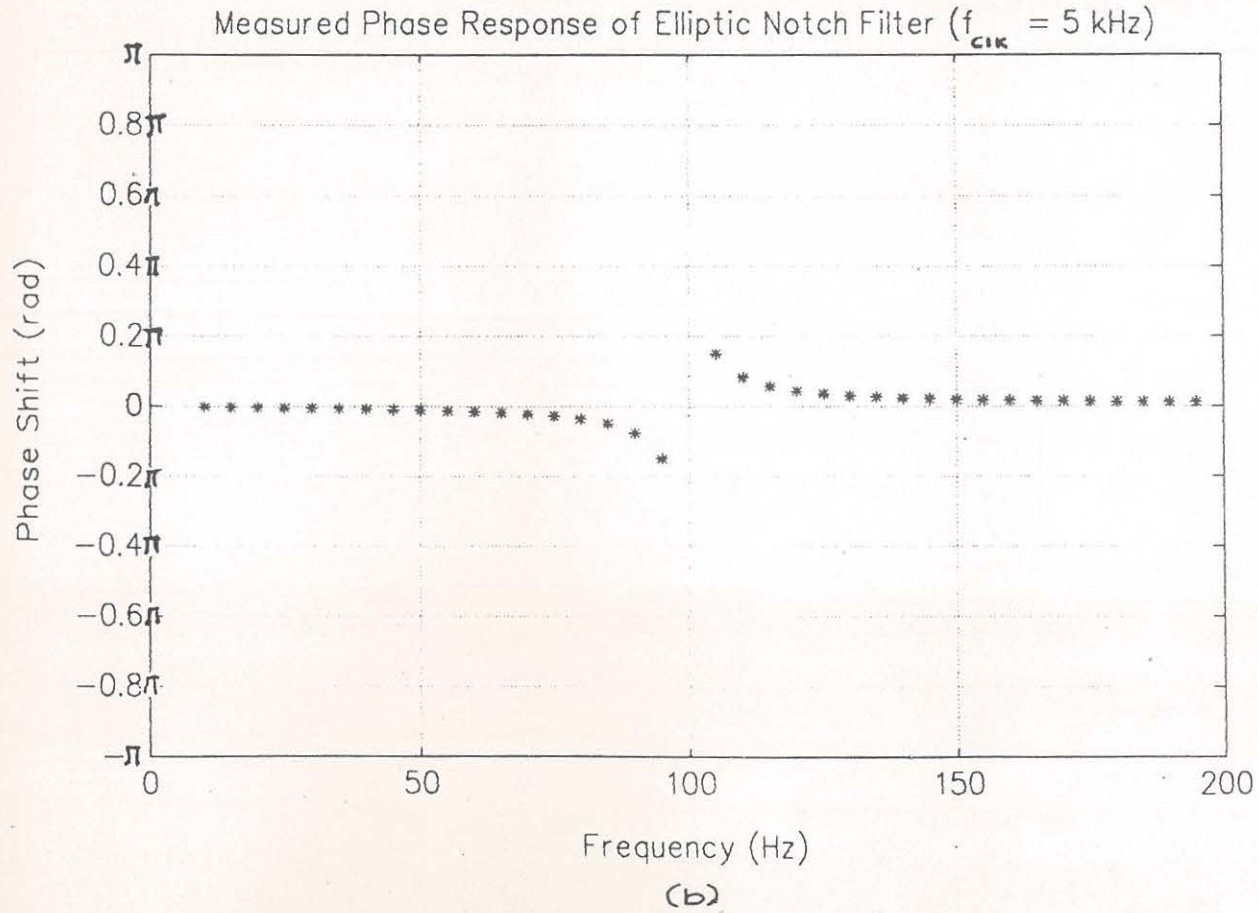




Fig. 3.12. Measured frequency response of second order elliptic notch filter. (a) magnitude response, (b) phase response.

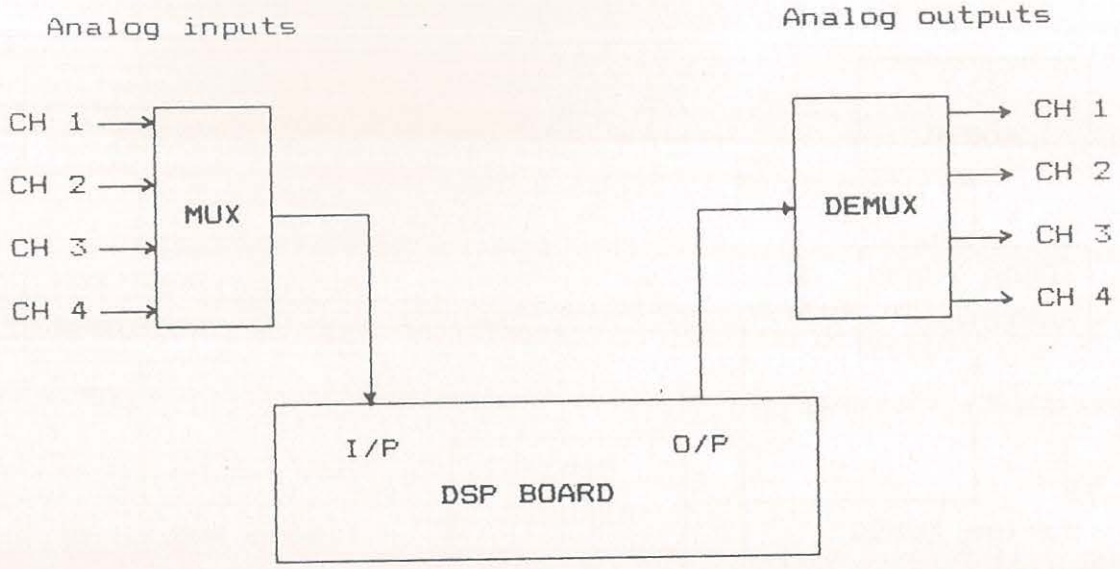



Fig. 4.1 Block diagram of I/O expansion with multiplexer and demultiplexer.

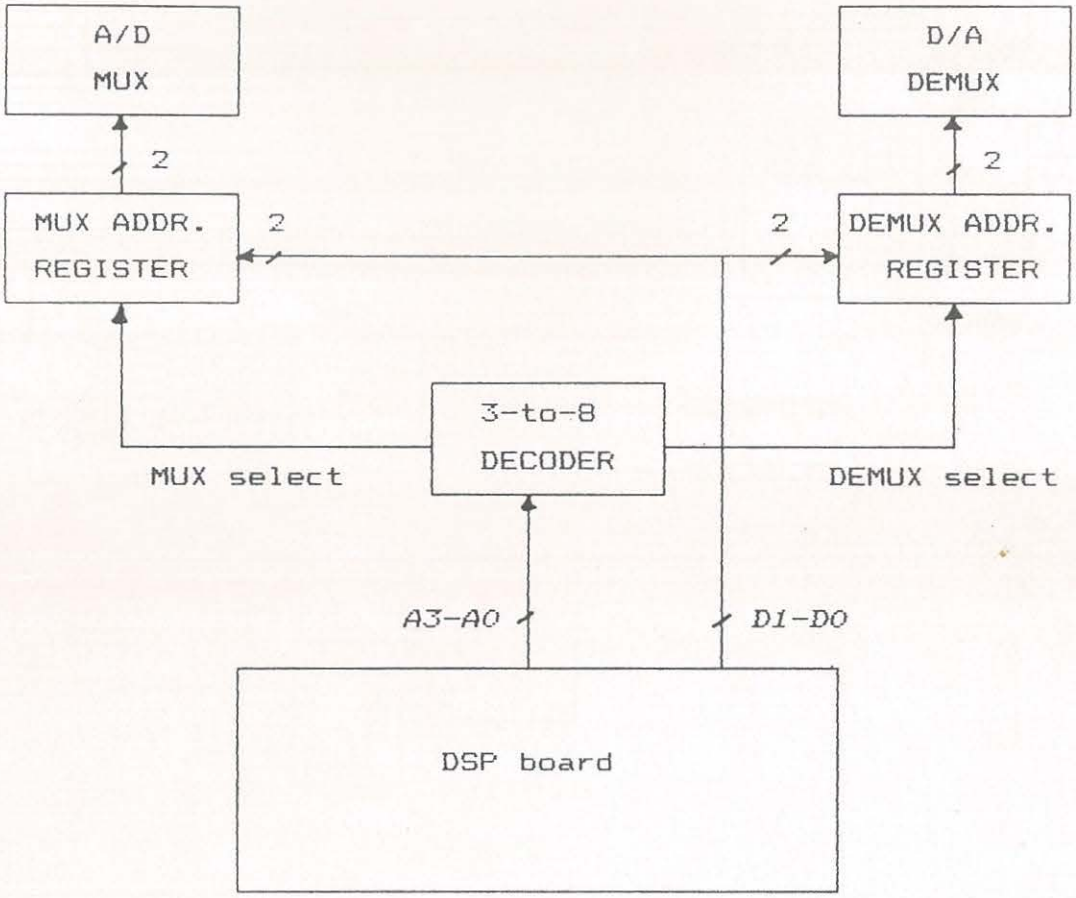



Fig. 4.2. Block diagram of the I/O expansion scheme.

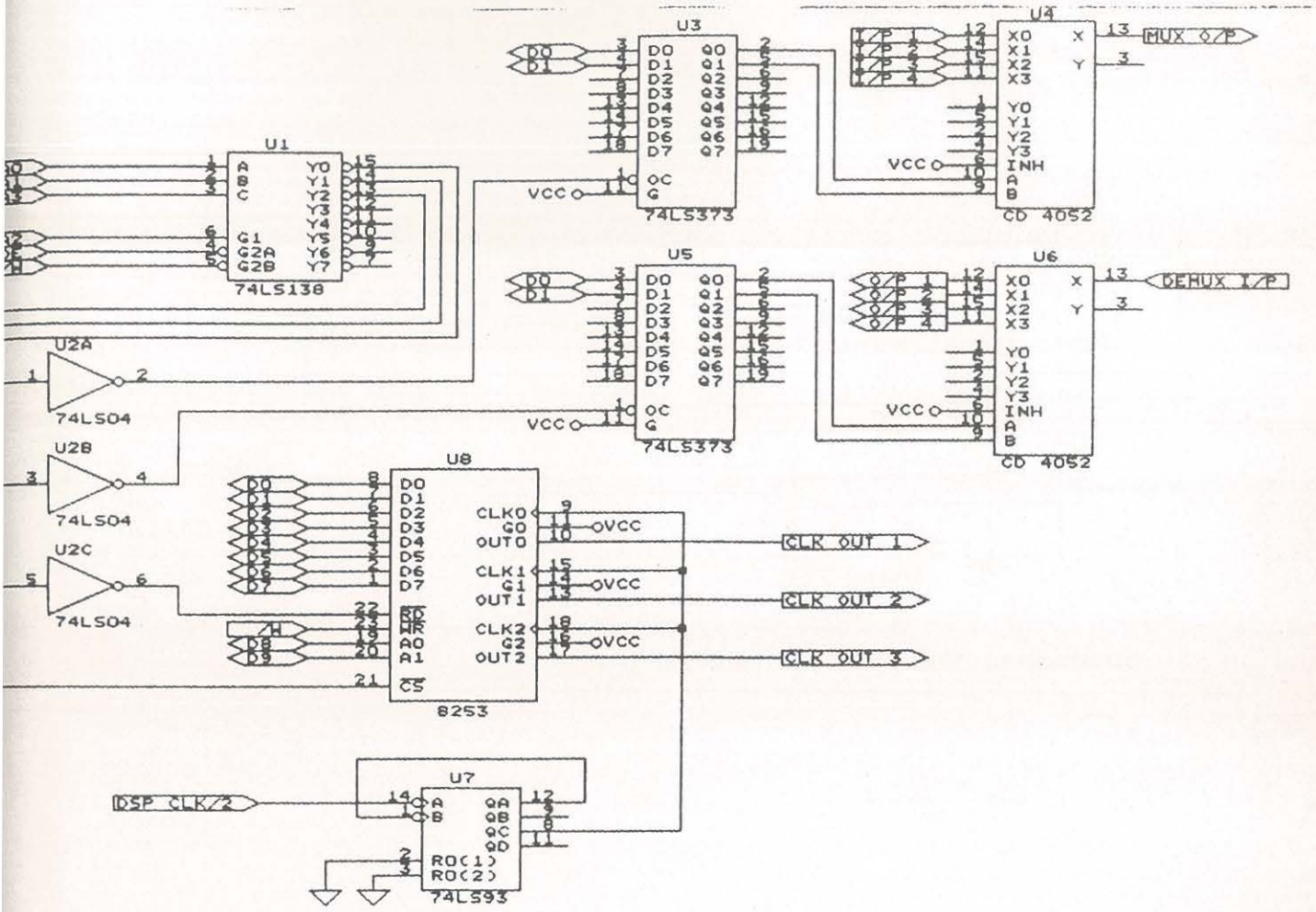



Fig. 4.3. Circuit schematic of the I/O expansion unit.

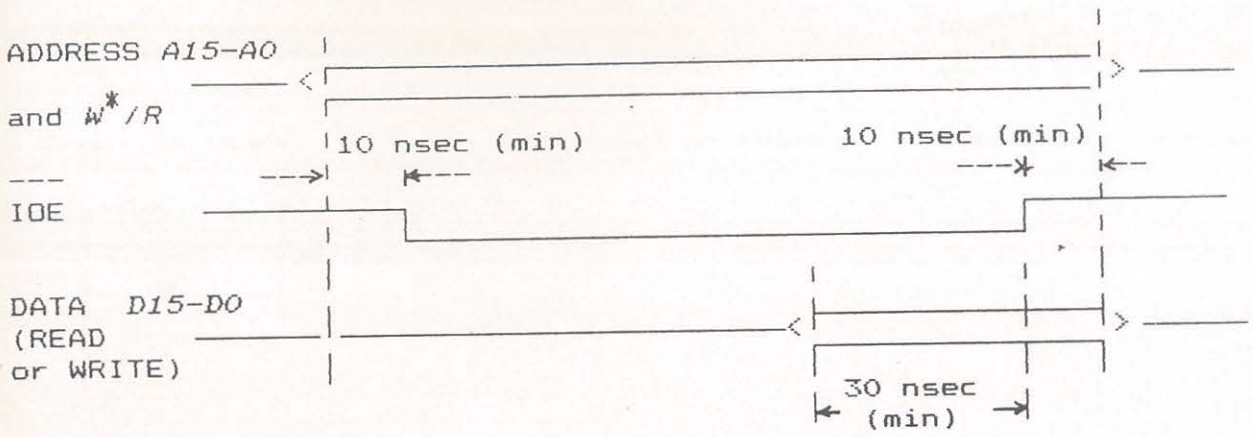
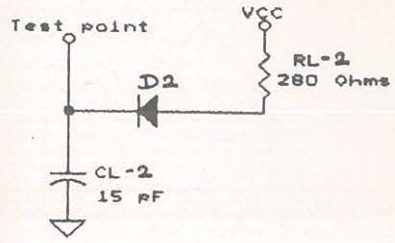
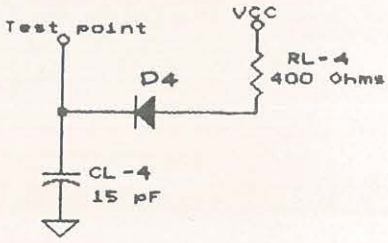


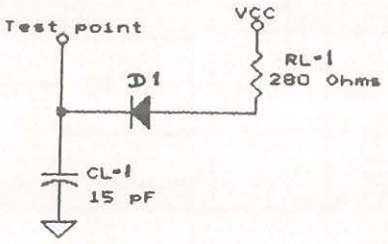

Fig 4.4. Timing diagram of OUT instruction for DSP processor TMS 320C25.



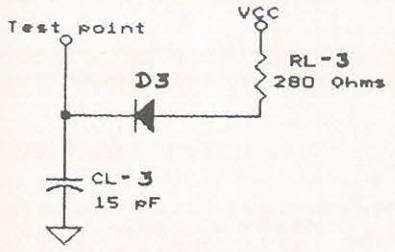

Load circuit for 74LS04




Load circuit for 74LS90




Load circuit for 74LS138




Load circuit for 74LS373

Fig. 4.5. Loading circuits for TTL ICs used on the I/O expansion unit.

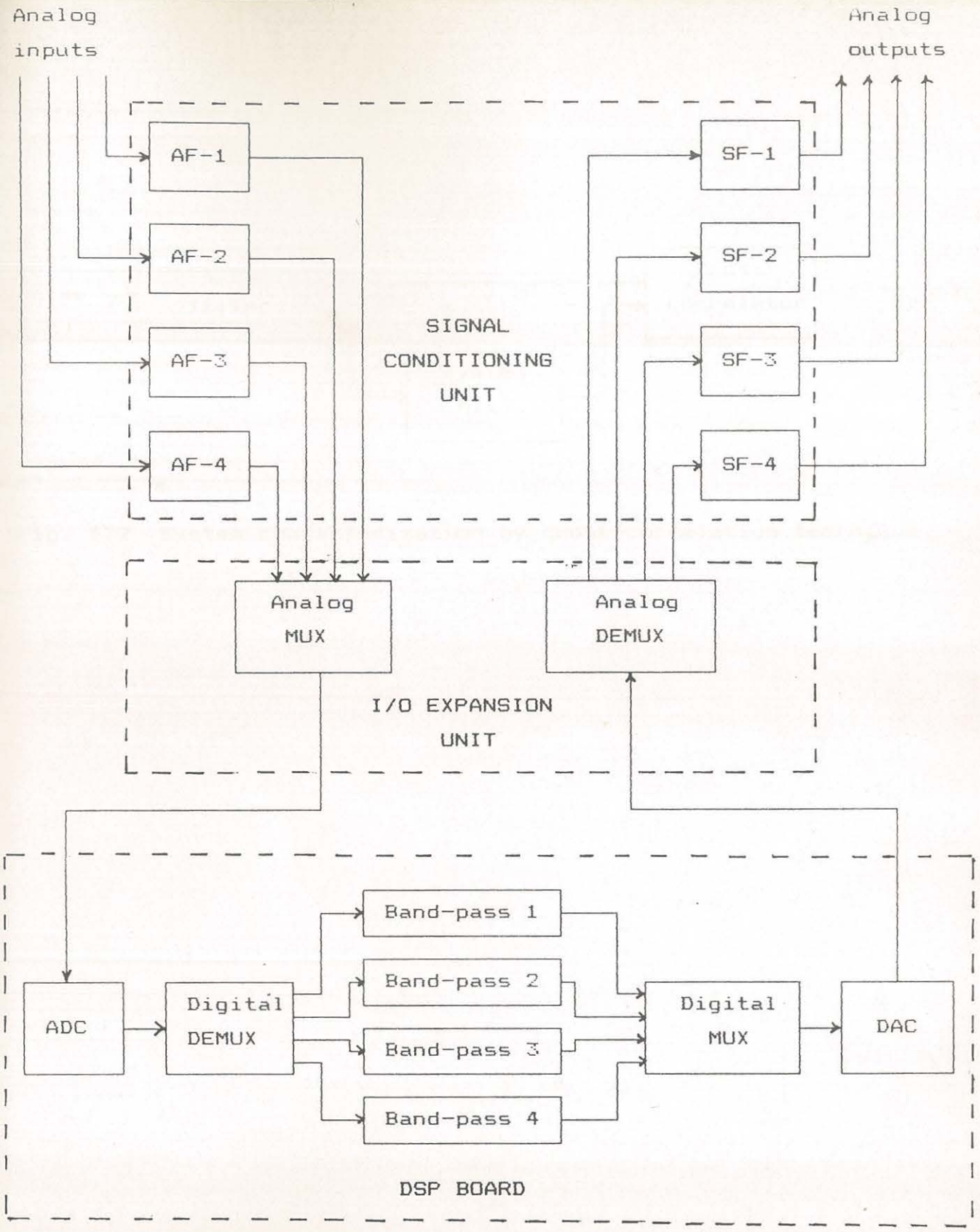



Fig. 5.1 Block diagram of band-pass filter for four channels.

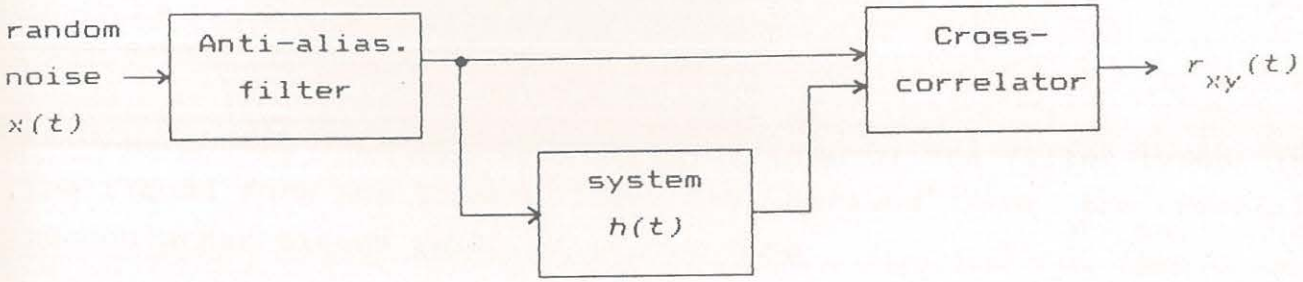



Fig. 5.2 System characterization by cross-correlation technique.

# APPENDIX A

## FILTER DESIGN

### A1. Filter Types

Here, the transfer functions for some of the filter types in the biquad form are listed. These are derived from the general second order biquad which is in the form

$$H(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + (\omega_0/Q)s + \omega_0^2} \qquad \text{(A1.1)}$$

1. Low-pass (LP) filter

$$H_{Lp}(s) = \frac{a_0}{s^2 + (\omega_0/Q)s + \omega_0^2} \qquad \text{(A1.2)}$$

This has two transmission zeros at $s = \infty$.

2. High-pass (HP) filter

$$H_{Hp}(s) = \frac{a_2 s^2}{s^2 + (\omega_0/Q)s + \omega_0^2} \qquad \text{(A1.3)}$$

This has two transmission zeros at $s = 0$.

3. Band pass (BP) filter

$$H_{Bp}(s) = \frac{a_1 s}{s^2 + (\omega_0/Q)s + \omega_0^2} \qquad \text{(A1.4)}$$

This has one transmission zeros at $s = \infty$ and one at $s = 0$.

4. Notch (NP) filter

$$H_{Np}(s) = a_2 \frac{s^2 + \omega_n^2}{s^2 + (\omega_0/Q)s + \omega_0^2} \qquad \text{(A1.5)}$$

This has two transmission zeros at $s = \pm j\omega_n$.

5. All pass filter

$$H_{Ap}(s) = a_2 \frac{s^2 - (\omega_0/Q)s + \omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2} \qquad \text{(A1.6)}$$

This has two transmission zeros, in the right half of the s-plane at mirror image location of poles.

## A2. Specifications of anti-aliasing filter

1. Maximum allowable pass-band ripple $A_p$

The maximum allowable pass-band gain variation $A_p$ of the anti-aliasing filter depends upon the resolution of the quantizer (A/D converter) preceding the anti-aliasing filter. The minimum signal detection level of the quantizer is specified as quantization step $\Delta$ given by

$$\Delta = 2\ V_m/(2^n - 1) \qquad \text{(A1.7)}$$

where input signal range is $\pm\ V_m$ and number of quantization bits is '$n$'.

Due to the variation in the pass-band gain, the signal level changes with frequency. In order that the error introduced during filtering is less than the resolution of the quantizer, the maximum variation in the signal level should be less than $\Delta/2$.

Let $\delta$ denote the maximum variation from unity gain. Then for input signal having a peak voltage of $V_m$, the maximum peak output voltage is then $V_m$ $(1 \pm \delta)$. The maximum error introduced in the signal level is then $V_m \delta$.

We want

$$V_m \delta < 1/2 \Delta \qquad \text{(A1.8)}$$

or $$\delta < \frac{1}{2^n - 1}$$

The maximum ripple in the pass-band $A_p$ is defined as

$$A_p \leq 20 \log [(1 + \delta)/(1 - \delta)] \qquad \text{(A1.9)}$$

Since $\delta << 1$, we get

$$A_p \leq 20 \log (1 + 2\delta) \qquad \text{(A1.10)}$$

For number of quantization bits $n = 10$ and signal range $\pm 5$ V we get

$$\Delta = 9.775 \times 10^{-3}$$

$$\delta < 9.77517 \times 10^{-4}$$

and

$$A_p \leq 0.01 \text{ dB} \qquad \text{(A1.11)}$$

However, such a low value of maximum variation is physically unrealizable and hence $A_p$ was chosen as

$$A_p \leq 0.1 \text{ dB}$$

By back calculations, it has been found that, for $n = 7$, the maximum allowable ripple in the pass-band would be 0.1 dB.

2. Minimum stop-band attenuation $A_{min}$

Minimum stop-band attenuation required depends upon the quantization noise as well as the signal-to-noise ratio at the input of the anti-aliasing filter. For uniform quantization, the root mean square quantization error $e_r$ is given as [12]

$$e_r = \sqrt{\bar{e}^2} = \Delta / \sqrt{12} \qquad \text{(A1.12)}$$

Assuming that the rms value of the signal $V_s = \alpha V_{..}$, the signal-to-quantization noise ratio is

$$\text{SQNR (dB)} = 20 \log (V_s/e_r) = 20 \log [\alpha (2^n - 1) \sqrt{12} /2 ] \qquad \text{(A1.13)}$$

For most common signals, $\alpha < 0.25$. For $\alpha = 0.25$, and for large value of $n$, we get,

$$\text{SQNR (dB)} \cong 6\, n - 7.26 \qquad \text{(A1.14)}$$

For signal-to-noise-ratio of $\rho$(dB), the minimum required attenuation in the stop-band $A_{min}$ is given as,

$$A_{min} \geq 6\, n - 7.26 - \rho \qquad \text{(A1.15)}$$

For number of quantization bits $n = 10$, and SNR = $\rho$ (dB) = 20 dB, we get

$$A_{min} = 32.74 \text{ dB} \qquad \text{(A1.16)}$$

We have chosen *Amin* = 40 dB, which is higher than required.

## A3. Order for different filter types for anti-aliasing filter

The order required for Butterworth, Chebychev, Bessel filters

that would satisfy the required specifications of the normalized filter is calculated for each type of the filter [2].
The normalized specifications are,

$$A_p = 0.1 \text{ dB};$$
$$\Omega_s = 1.1;$$
$$A_{min} = 40 \text{ dB},$$

We want $\omega_a / \omega_p = 1.1$.

Take, $\omega_a = \sqrt{1.1} = 0.9534$

$\omega_p = \sqrt{1/1.1} = 1.048$

For Butterworth filter the order is decided by,

$$A(\omega) = 10 \log (1 + \omega^{2n}).$$

Substituting the values, we get order of the filter satisfying the above specifications as 137.

For Chebyshev filter the order is decided by,

$$\varepsilon^2 = 10^{0.1Ap} - 1;$$
$$F(\omega) = \cos (n\cos^{-1}\omega) \quad ; \quad |\omega| \leq 1$$
$$= \cosh (n\cosh^{-1}\omega) \; ; \quad |\omega| > 1$$
$$L(\omega^2) = 1 + \varepsilon^2 F^2 (\omega);$$
$$A(\omega) = 10 \log L (\omega^2);$$

We want,

$$A(1) = 0.1 \text{ dB};$$

$A(1.1) = 40$ dB;

$A(1) = 0.1$ dB gives,

$$\varepsilon^2 = 0.023;$$

$A(1.1) = 40$ db gives,

$$L(1.21) = 10^4 ;$$
$$F(1.21) = 659.34;$$
$$\cosh (n\cosh^{-1}1.21) = 659.34;$$
$$n\cosh^{-1}1.21 = 7.184;$$
$$n \geq 12$$

For elliptic filter,

$$k = 1/\Omega_s;$$
$$k' = (1-k^2)^{1/2};$$
$$q_0 = \frac{1}{2} \frac{(1-k')^{1/2}}{(1+k')^{1/2}} ;$$

$$q \cong q_0 + 2q_0^5 + 15q_0^9 + 150q_0^{13};$$

$$D = \frac{10^{0.1A_a} + 1}{10^{0.1A_p} - 1};$$

$$n \geq \frac{\log(16D)}{\log(1/q)};$$

For the given specifications,

$$k = 0.8621;$$

$$k' = 0.506;$$

$q_O = 0.08414;$

$q = 0.08418;$

$D = 537829.67;$

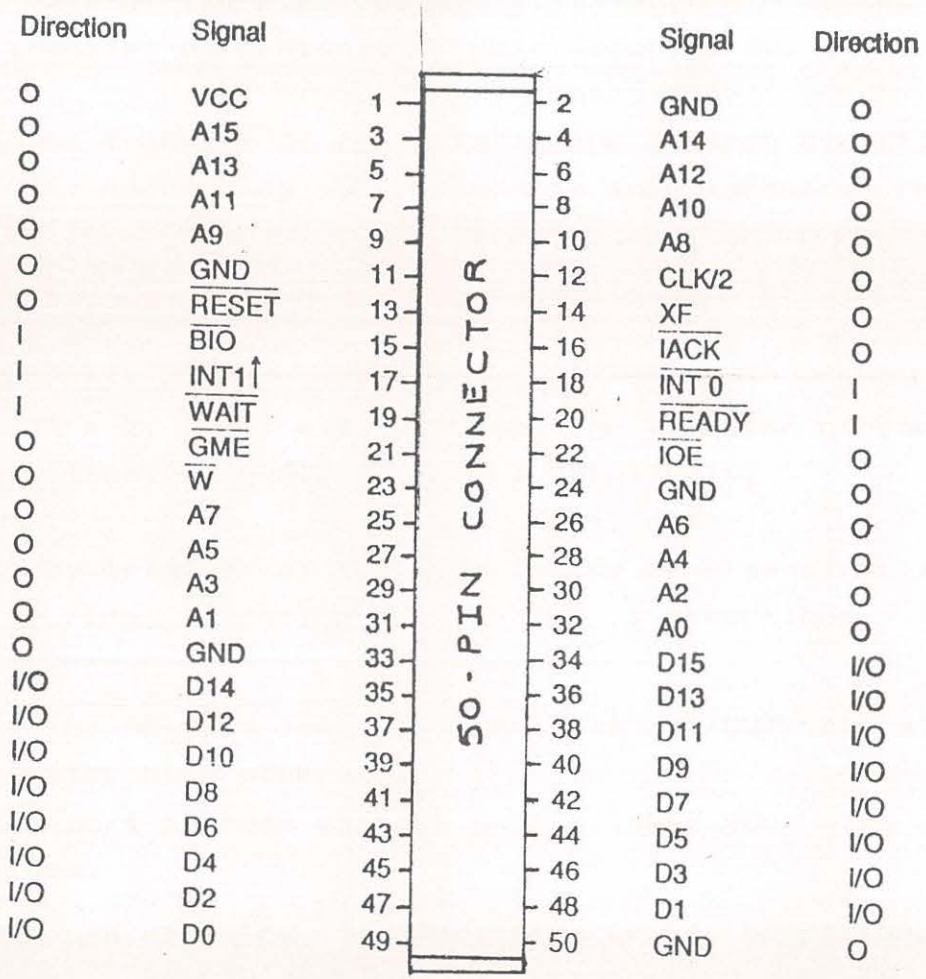
$n \geq 6.45;$

ie. $n \geq 7;$

# APPENDIX B

## I/O EXPANSION BUS AND I/O INSTRUCTIONS OF DSP BOARD

B1. The pin-out assignment on the I/O expansion bus of the DSP board PCL-DSP25, "DSPLINK", is as shown.



## B2. IN/OUT Instructions

This section provides a detailed review of the IN/OUT instructions. This DSP board support direct as well as indirect addressing.

Direct Addressing : Data memory is divided into number of pages. Page pointer register points to the base address, and offset (dma) from this page is specified in operand. For example,

OUT <dma>, <PA>

with base of the page pointed at 0x400; PA = 3; and dma = 01, does the transfer of contents of data memory 0x401 to port 3. Similarly

IN <dma>, <PA>

does the transfer of the data in the reverse direction.

Indirect Addressing : DSP supports some hardware registers which can be accessed by the software instruction to facilitate faster operation. The contents of the auxiliary register gives the data memory address. For example,

OUT <AR> , <PA>

with AR = 2; (AR2) = 0x400, does the transfer of contents of data memory location 0x400 to port 2. Similarly,

IN <AR>, <PA>

does the transfer of the data in the reverse direction.

During execution of IN/OUT instructions, the following occurs:

1. A pin $\overline{IOE}$ goes low, to indicate IN/OUT operation. The pin remains high otherwise.
2. The port address appears on the lower four bits of the address lines.
3. $\overline{W/R}$ pin goes low to indicate write operation for OUT and remains high otherwise.
4. Contents of the data memory appears on data lines.

# APPENDIX C

## Program Listing

P1. Sample program to illustrate I/O expansion.
('C' and DSP TMS 320C25 assembly language)

P2. Programmable clock generation.
('C' and DSP TMS 320C25 assembly language)

**P1.**
```
/* This program takes the input from the selected input channel
   and outputs it to the selected output channel.*/

# include <stdio.h>
# include <conio.h>
# include <dos.h>
# include <sti25dev.c>

main()
{
 int i,o;
 SelectBoard(1);                    /* Selects the DSP board (1) */
 WarmStart();                       /* Allows a user-progra  to
                                       interface with the TMS board,
                                       without interfering with any
                                       program already running on
                                       the DSP board.*/

 clrscr();
 printf("This is a sample program to illustrate the I/O expansion"
        " of the DSP board PCL-DSP25");
 printf("Enter the input channel address  (0 - 3) : ");
 scanf("%d",&i);
 printf("Enter the output channel address (0 - 3) : ");
 scanf("%d",&o);
 PutMem16('d',0x400,i);             /* Store input channel address
                                       in data memory location >400 of
                                       DSP board.*/
 PutMem16('d',0x401,o);             /* Store output channel address
                                       in data memory location >401  of
                                       DSP board.*/
 LoadObjectFile("test.mpo");        /* Load the assembly language
                                       program in the program memory of
                                       the DSP chip at the address
                                       specified in the program.*/

 Reset();                           /* Pulses the hardware reset signal
                                       to the DSP board, sets program
                                       counter to 0, and allows the
                                       processor to run.*/
}
```

P1. Sample program to illustrate I/O expansion (assembly language)

```
* * * * * * * * *
*     TEST        *
* * * * * * * * *

* PROGRAM TO PROVIDE AN INTERRUPT DRIVEN ECHO FROM ADC TO DAC
* WITH ADC CONNECTED TO THE SELECTED INPUT CHANNEL AND DAC
* CONNECTED TO SELECTED OUTPUT CHANNEL
* THE FOLLOWING LINKS MUST BE INSERTED BEFORE RUNNING THE CODE:
*       LK1a
*       LK12a
*       LK13a


* DEFINE ADDRESS CONSTANTS

PAGE0   EQU     0       Page 0 of data mem for mem-mapped regs
IMR     EQU     >4      Address of Mask Register in Page Zero
TEMP    EQU     >63     Word >63 of B2 will be temporary store
VAL     EQU     >64     Word >64 of B2 will hold output value
*
TIM     EQU     1       Port 1 is the timer address
*                       Use LK15b to generate processor interrupts.
ADC     EQU     3       Port 2 is the ADC address when using
*                       interval timer clocking (use LK17a)
DAC     EQU     3       Port 2 is the DAC address when using
*                       interval timer. Put link at LK16a.
ICHADD  EQU     >00     This has the input channel address selected
*                       by the user.
OCHADD  EQU     >01     This has the output channel address selected
*                       by the user.
MUX     EQU     >05     Port 5 is multiplexer port.
DEMUX   EQU     >04     Port 6 is demultiplexer port.

* DEFINE DATA CONSTANTS

TIMVAL  EQU     -100    Timer value for clocking at about 44KHz
IMASK   EQU     >FFC2   Interrupt mask to enable INT1 only

* SET ISR VECTOR
```

```
        AORG    >0
        B       MAIN

        AORG    >4              Address  of the INT1 vector
*
        B       ISR             Branch to service routine
*
* START OF MAIN PROGRAM
*
MAIN    AORG    >400            Start of available program area
*
        LDPK    PAGE0           Page pointer set to 0
*
        LRLK    >0,TIMVAL       Timer value in AR0
        SAR     >0,TEMP         Store in data memory temporarily
        OUT     TEMP,TIM        Output value to timer port
*
        LRLK    >1,IMASK        Load interrpt mask into AR1
        SAR     >1,IMR          Put it into Mask Register
*
        LDPK    8
        OUT     ICHADD,MUX      Select input channel
        OUT     OCHADD,DEMUX    Select output channel

        EINT                    Enable interrupts
*
LOOP    B       LOOP            Wait for interrupts to arrive
*
* THIS IS THE END OF THE MAIN PROGRAM
*
* THIS IS THE START OF THE INTERRUPT SERVICE ROUTINE
*
        AORG    >500            Address of ISR
*
ISR     IN      VAL,ADC         Store the ADC value in data mem
        OUT     VAL,DAC         Load data mem value to DAC
*
        EINT                    Re-enable the interrupts
        RET                     Return to main program
*
 END
```

P2. Programmable clock generation ('C' language).

```
/* THIS PROGRAM ASKS THE USR TO ENTER THREE CUT-OFF FREQUENCIES
   REQUIRED; DOES THE CALCULATIONS AND STORES THE APPROPRIATE VALUES
   AT THE MEMORY LOCATIONS REQUIRED BY THE ASSEMBLY LANGUAGE PROGRAM
   "CLOCK.ASM". CLOCK.ASM DOES THE INITIALISATION OF THE 8253 TIMER
   AND GENERATES THE CLOCK FREWQUENCIES.  */

# include <stdio.h>
# include <conio.h>
# include <dos.h>
# include <sti25dev.c>

main()
{
 int m_a1,m_a2,m_a3,l_a1,l_a2,l_a3;
 float a1,a2,a3,temp1,temp2,temp3,f_a1,f_a2,f_a3,c1,c2,c3,cl1,cl2,cl3;
 long i_a1,i_a2,i_a3;

 SelectBoard(1);                    /* SELECTS THE DSP BOARD (1) */
 WarmStart();

 /* PROGRRM ASKS FOR THREE CUT-OFF FREQUECIES REQUIRED IN KHz */
 clrscr();
 printf("This programme sets the clock frequency for the SC-filters.");
 printf("Three programmable frequencies are possible.");
 printf("Enter cutoff freq. of filter1 (KHz) = ");
 scanf("%f",&c1);  /* c1 = CUTOFF FREQ 1 (KHz) */
 printf("Enter cutoff freq. of filter2 (KHz) = ");
 scanf("%f",&c2);  /* c2 = CUTOFF FREQ 2 (KHz) */
 printf("Enter cutoff freq. of filter3 (KHz) = ");
 scanf("%f",&c3);  /* c3 = CUTOFF FREQ 3 (KHz) */

 /* The clock freq. is  2.5 MHz for the 8253 timer
    Clock freq. = cutoff * 100 */

cl1 = c1 * 100;  /* CLOCK 1 (KHz) */
cl2 = c2 * 100;  /* CLOCK 2 (KHz) */
cl3 = c3 * 100;  /* CLOCK 3 (KHz) */
```

```
a1 = 2500.0 / c11 ;
a2 = 2500.0 / c12 ;
a3 = 2500.0 / c13 ;

i_a1 = a1;
i_a2 = a2;
i_a3 = a3;

/* split into LSB and MSB */

temp1 = i_a1 / 256.0;
temp2 = i_a2 / 256.0;
temp3 = i_a3 / 256.0;

m_a1 = temp1;
m_a2 = temp2;
m_a3 = temp3;

l_a1 = (int) ((temp1 - m_a1) * 256);
l_a2 = (int) ((temp2 - m_a2) * 256);
l_a3 = (int) ((temp3 - m_a3) * 256);

l_a2 = 256 + l_a2;
      /* FOR COUNTER 1, D9 = 0, D8 = 1 ie. ([X] [xx01] [D] [D]) */
l_a3 = 512 + l_a3;
      /* FOR COUNTER 2, D9 = 1, D8 = 0 ie. ([X] [xx10] [D] [D]) */
m_a2 = 256 + m_a2;
      /* FOR COUNTER 1, D9 = 0, D8 = 1 ie. ([X] [xx01] [D] [D]) */
m_a3 = 512 + m_a3;
      /* FOR COUNTER 2, D9 = 1, D8 = 0, ie. ([X] [xx10] [D] [D]) */

/* Write control word for counter 0 to set in squre wave generation.*/
/* DATA PAGE POINTER IN "CLOCK.ASM" = 8 */

/* FOR CR, D9 = 1, D8 = 1 ie. ([X] [xx11] [D] [D]) */

 PutMem16('d',0x400,0x0336);
 /* COUNTER 0 IN WRITE LSB FIRST, MSB NEXT, BINARY COUNT AND SQUARE
    WAVE GEN. MODE */
```

```
PutMem16('d',0x401,l_a1);       /* LOAD LSB FOR COUNTER 0 */
PutMem16('d',0x402,m_a1);       /* LOAD MSB FOR COUNTER 0 */

PutMem16('d',0x403,0x0376);
/* COUNTER 1 IN WRITE LSB FIRST, MSB NEXT, BINAY COUNT AND SQUARE
   WAVE GEN. MODE */

PutMem16('d',0x404,l_a2);       /* LOAD LSB FOR COUNTER 1 */
PutMem16('d',0x405,m_a2);       /* LOAD MSB FOR COUNTER 1 */

PutMem16('d',0x406,0x03B6);
/* COUNTER 2 IN WRITE LSB FIRST, MSB NEXT, BINARY COUNT AND SQUARE
   WAVE GEN. MODE */

PutMem16('d',0x407,l_a3);       /* LOAD LSB FOR COUNTER 2 */
PutMem16('d',0x408,m_a3);       /* LOAD MSB FOR COUNTER 2 */

/* NOW LOAD THE ASSEMBLY LANG. PROGRAM  AND RUN IT TO LOAD THE
   COUNTERS. IN THIS ASM PROG. A BRANCH AT LOCATION 0 TO >400 CAUSES
   THE EXECUTION OF THE PROGRAM */

LoadObjectFile("clock.mpo");

/* RESET STARTS THE EXECUTION WITH PROGRAM COUNTER RESET TO 0 */
Reset();
}
```

P2. Programmable clock generation (assembly language).

```
* * * * * *
*  CLOCK  *
* * * * * *

C_PORT  EQU     >6      PORT 6 IS CUT-OFF TIMER PORT.
*
                AORG    >0
                B       START

* MAIN PROGRAM

START           AORG    >400

                LDPK    8               BASE ADDRESS OF DATA MEMORY
*                                       AT  >400

                OUT     >00,C_PORT      CONTROL WORD FOR COUNTER 0
                OUT     >01,C_PORT      LSB OF COUNT 0
                OUT     >02,C_PORT6     MSB OF COUNT 0

                OUT     >03,C_PORT      CONTROL WORD FOR COUNTER 1
                OUT     >04,C_PORT      LSB OF COUNT 1
                OUT     >05,C_PORT      MSB OF COUNT 1

                OUT     >06,C_PORT      CONTROL WORD FOR COUNTER 2
                OUT     >07,C_PORT      LSB OF COUNT 2
                OUT     >08,C_PORT      MSB OF COUNT 2

LOOP            NOP
                B       LOOP
```

# APPENDIX D

## DATA SHEETS

| | | |
|---|---|---|
| D1. | 74LS04 | : Hex Inverter |
| D2. | 74LS93 | : Binary Counter |
| D3. | 74LS138 | : 3-to-8 Decoder |
| D4. | 74LS373 | : Octal Latches |
| D5. | CD 4052 | : Dual 4 Channel MUX-DEMUX |
| D6. | MF 10 | : Switched Capacitor Filter |
| D7. | INTEL 8253 | : Programmable Timer/Counter |

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

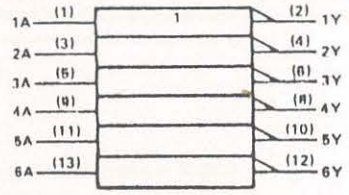
These devices contain six independent inverters.

The SN5404, SN54LS04, and SN54S04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7404, SN74LS04, and SN74S04 are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE (each inverter)**

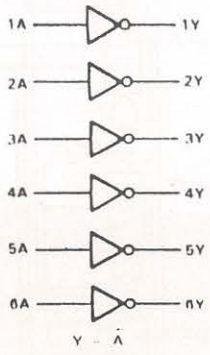
| INPUTS A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic symbol†



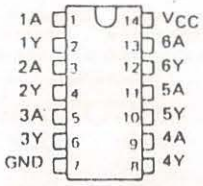

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

## logic diagram (positive logic)

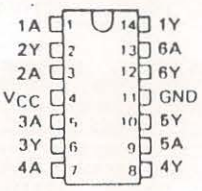



$Y = \overline{A}$

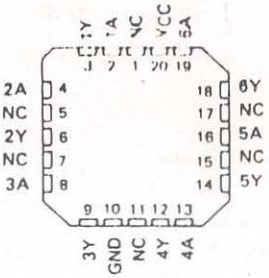
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404 . . . N PACKAGE
SN74LS04, SN74S04 . . . D OR N PACKAGE
(TOP VIEW)




SN5404 . . . W PACKAGE
(TOP VIEW)




SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)




NC – No internal connection

'90A, 'LS90 . . . Decade Counters

'92A, 'LS92 . . . Divide By-Twelve Counters

'93A, 'LS93 . . . 4-Bit Binary Counters

| TYPES | TYPICAL POWER DISSIPATION |
|---|---|
| '90A | 145 mW |
| '92A, '93A | 130 mW |
| 'LS90, 'LS92, 'LS93 | 45 mW |

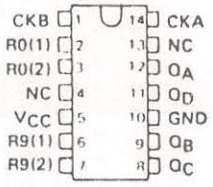
scription

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

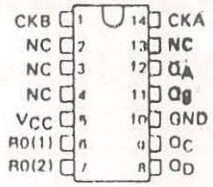
All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set to nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the $Q_A$ output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the $Q_D$ output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output $Q_A$.

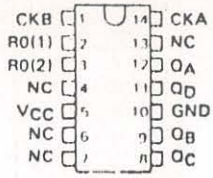
SN5490A, SN54LS90 . . . J OR W PACKAGE
SN7490A . . . N PACKAGE
SN74LS90 . . . D OR N PACKAGE
(TOP VIEW)




SN5492A, SN54LS92 . . . J OR W PACKAGE
SN7492A . . . N PACKAGE
SN74LS92 . . . D OR N PACKAGE
(TOP VIEW)



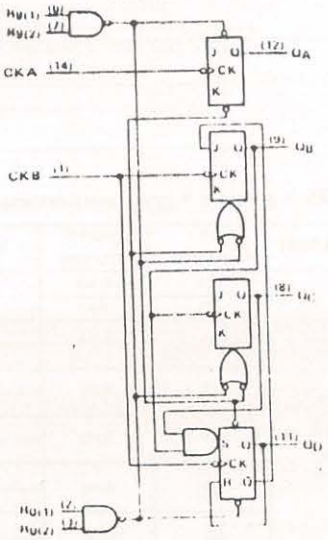

SN5493A, SN54LS93 . . . J OR W PACKAGE
SN7493 . . . N PACKAGE
SN74LS93 . . . D OR N PACKAGE
(TOP VIEW)



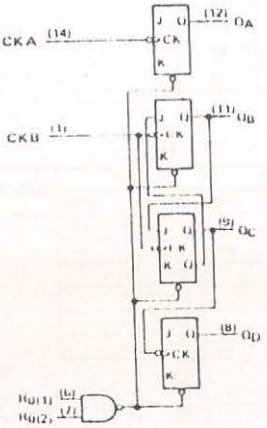

NC – No internal connection

## logic diagrams (positive logic)

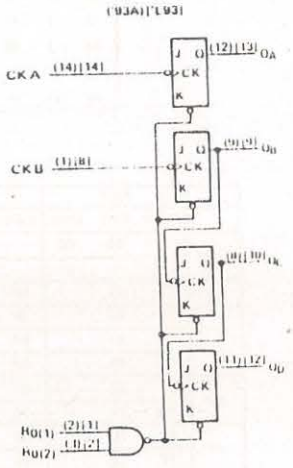
'90A, 'LS90




'92A, 'LS92




'93A, 'LS93




The J and K inputs shown without connection are for reference only and are functionally at a high level.
Pin numbers shown in ( ) are for the 'LS93 and '93A and pin numbers shown in [ ] are for the b4L93.

'90A, 'LS90
BCD COUNT SEQUENCE
(See Note A)

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

'90A, 'LS90
BI-QUINARY (5-2)
(See Note B)

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

'92A, 'LS92
COUNT SEQUENCE
(See Note C)

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | H | L | L | L |
| 7 | H | L | L | H |
| 8 | H | L | H | L |
| 9 | H | L | H | H |
| 10 | H | H | L | L |
| 11 | H | H | L | H |

'90A, 'LS90
RESET/COUNT FUNCTION TABLE

| RESET INPUTS | | | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $R_{9(1)}$ | $R_{9(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

'92A, 'LS92, '93A, 'LS93
RESET/COUNT FUNCTION TABLE

| RESET INPUTS | | OUTPUT | | | |
|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

'93A, 'LS93
COUNT SEQUENCE
(See Note C)

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

NOTES A. Output $Q_A$ is connected to input CKB for BCD count.
B. Output $Q_D$ is connected to input CKA for bi-quinary count.
C. Output $Q_A$ is connected to input CKB.
D. H = high level, L = low level, X = irrelevant

**Switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C**

| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | '90A | | | '92A | | | '93A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $f_{max}$ | CKA | $Q_A$ | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Figure 1 | 32 | 42 | | 32 | 42 | | 32 | 42 | | MHz |
| | CKB | $Q_B$ | | 16 | | | 16 | | | 16 | | | |
| $t_{PLH}$ | CKA | $Q_A$ | | | 10 | 16 | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 12 | 18 | | 12 | 18 | | 12 | 18 | |
| $t_{PLH}$ | CKA | $Q_D$ | | | 32 | 48 | | 32 | 48 | | 46 | 70 | ns |
| $t_{PHL}$ | | | | | 34 | 50 | | 34 | 50 | | 46 | 70 | |
| $t_{PLH}$ | CKB | $Q_B$ | | | 10 | 16 | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 14 | 21 | | 14 | 21 | | 14 | 21 | |
| $t_{PLH}$ | CKB | $Q_C$ | | | 21 | 32 | | 10 | 16 | | 21 | 32 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 14 | 21 | | 23 | 35 | |
| $t_{PLH}$ | CKB | $Q_D$ | | | 21 | 32 | | 21 | 32 | | 34 | 51 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 23 | 35 | | 34 | 51 | |
| $t_{PHL}$ | Set-to-0 | Any | | | 26 | 40 | | 26 | 40 | | 26 | 40 | ns |
| $t_{PLH}$ | Set-to-9 | $Q_A$, $Q_D$ | | | 20 | 30 | | | | | | | ns |
| $t_{PHL}$ | | $Q_B$, $Q_C$ | | | 26 | 40 | | | | | | | |

# SN54LS138, SN54S138, SN74LS138, SN74S138A
# 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

DECEMBER 1972 - REVISED MARCH 1988

- Designed Specifically for High-Speed:
  Memory Decoders
  Data Transmission Systems
- 3 Enable Inputs to Simplify Cascading and/or Data Reception
- Schottky-Clamped for High Performance

## description

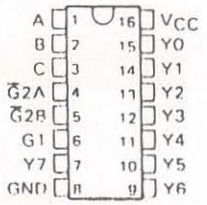
These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138, SN54S138, and SN74S138A decode one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

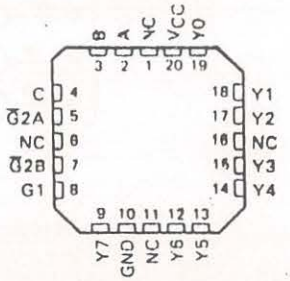
All of these decoder/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design.

The SN54LS138 and SN54S138 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS138 and SN74S138A are characterized for operation from 0°C to 70°C.

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138A . . . D OR N PACKAGE
(TOP VIEW)

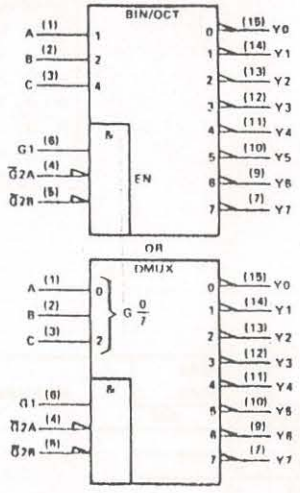



SN54LS138, SN54S138 . . . FK PACKAGE
(TOP VIEW)




NC – No internal connection

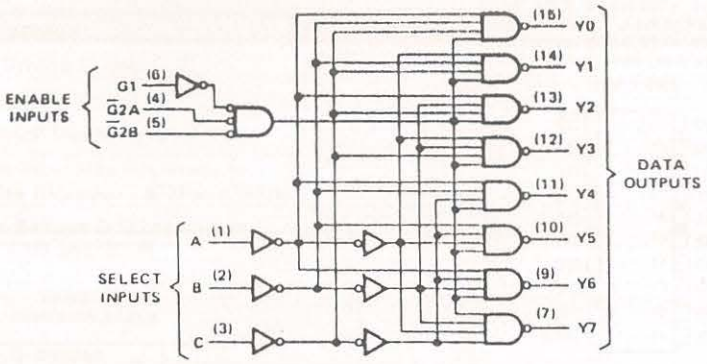
## logic symbols†




†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

## logic diagram and function table

'LS138, SN54S138, SN74S138A




Pin numbers shown are for D, J, N, and W packages.

'LS138, SN54138, SN74S138A
FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ENABLE | | SELECT | | | | | | | | | | |
| G1 | G2* | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

*$\overline{G2} = \overline{G2A} + \overline{G2B}$
H = high level, L = low level, X = irrelevant

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER[1] | FROM (INPUT) | TO (OUTPUT) | LEVELS OF DELAY | TEST CONDITIONS | SN54LS138 SN74LS138 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | Binary Select | Any | 2 | $R_L$ = 2 kΩ, $C_L$ = 15 pF, See Note 2 | | 11 | 20 | ns |
| $t_{PHL}$ | | | | | | 18 | 41 | ns |
| $t_{PLH}$ | | | 3 | | | 21 | 27 | ns |
| $t_{PHL}$ | | | | | | 20 | 39 | ns |
| $t_{PLH}$ | Enable | Any | 2 | | | 12 | 18 | ns |
| $t_{PHL}$ | | | | | | 20 | 32 | ns |
| $t_{PLH}$ | | | 3 | | | 14 | 26 | ns |
| $t_{PHL}$ | | | | | | 19 | 38 | ns |

# SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374
## OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

OCTOBER 1976 – REVISED MARCH 1988

- Choice of 8 Latches or 8 D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)

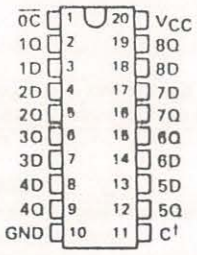
'LS373, 'S373
FUNCTION TABLE

| OUTPUT ENABLE | ENABLE LATCH | D | OUTPUT |
|---|---|---|---|
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

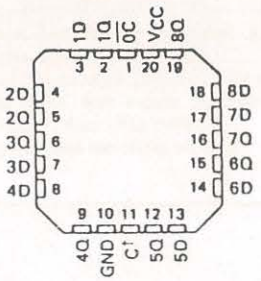
'LS374, 'S374
FUNCTION TABLE

| OUTPUT ENABLE | CLOCK | D | OUTPUT |
|---|---|---|---|
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . J OR W PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . DW OR N PACKAGE
(TOP VIEW)




SN54LS373, SN54LS374, SN54S373, SN54S374 . . . FK PACKAGE
(TOP VIEW)



National Semiconductor

# CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
# CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
# CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

## General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD} = 5V$, $V_{SS} = 0V$ and $V_{EE} = -5V$, analog signals from −5V to +5V can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

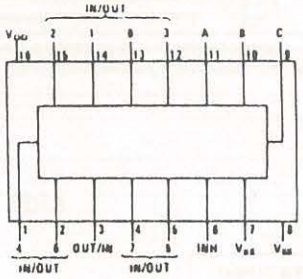
## Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to $15V_{p-p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD} - V_{EE} = 15V$
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at $V_{DD} - V_{EE} = 10V$
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD} - V_{SS} = 3–15V$) to switch analog signals to 15 $V_{p-p}$ ($V_{DD} - V_{EE} = 15V$)
- Matched switch characteristics: $\Delta R_{ON} = 5\Omega$ (typ.) for $V_{DD} - V_{EE} = 15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10V$
- Binary address decoding on chip

## Connection Diagrams

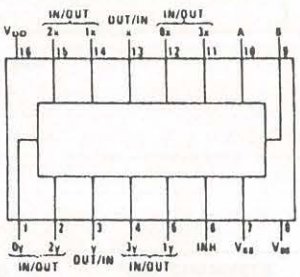
Dual-In-Line Packages

CD4051BM/CD4051BC



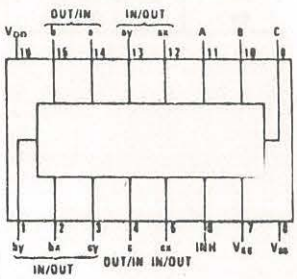

TOP VIEW

CD4052BM/CD4052BC




TOP VIEW

CD4053BM/CD4053BC




TOP VIEW TL/F/5682-1

Order Number CD4051B*, CD4052B*, or CD4053B*

*Please look into Section 8, Appendix D for availability of various package types.

## AC Electrical Characteristics* $T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

| Symbol | Parameter | Conditions | $V_{DD}$ | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PZH}$, $t_{PZL}$ | Propagation Delay Time from Inhibit to Signal Output (channel turning on) | $V_{EE} - V_{SS} = 0V$<br>$R_L = 1\ k\Omega$<br>$C_L = 50$ pF | 5V<br>10V<br>15V | | 600<br>225<br>160 | 1200<br>450<br>320 | ns<br>ns<br>ns |
| $t_{PHZ}$, $t_{PLZ}$ | Propagation Delay Time from Inhibit to Signal Output (channel turning off) | $V_{EE} = V_{SS} = 0V$<br>$R_L = 1\ k\Omega$<br>$C_L = 50$ pF | 5V<br>10V<br>15V | | 210<br>100<br>75 | 420<br>200<br>150 | ns<br>ns<br>ns |
| $C_{IN}$ | Input Capacitance<br>Control Input<br>Signal Input (IN/OUT) | | | | <br>5<br>10 | <br>7.5<br>15 | <br>pF<br>pF |
| $C_{OUT}$ | Output Capacitance (common OUT/IN) | | | | | | |
| | CD4051<br>CD4052<br>CD4053 | $V_{EE} - V_{SS} = 0V$ | 10V<br>10V<br>10V | | 30<br>15<br>8 | | pF<br>pF<br>pF |
| $C_{IOS}$ | Feedthrough Capacitance | | | | 0.2 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance | | | | | | |
| | CD4051<br>CD4052<br>CD4053 | | | | 110<br>140<br>70 | | pF<br>pF<br>pF |
| **Signal Inputs ($V_{IS}$) and Outputs ($V_{OS}$)** | | | | | | | |
| | Sine Wave Response (Distortion) | $R_L = 10\ k\Omega$<br>$f_{IS} = 1$ kHz<br>$V_{IS} = 5\ V_{p-p}$<br>$V_{EE} = V_{SI} = 0V$ | 10V | | 0.04 | | % |
| | Frequency Response, Channel "ON" (Sine Wave Input) | $R_L = 1\ k\Omega$, $V_{EE} = 0V$, $V_{IS} = 5V_{p-p}$,<br>$20 \log_{10} V_{OS}/V_{IS} = -3$ dB | 10V | | 40 | | MHz |
| | Feedthrough, Channel "OFF" | $R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$,<br>$20 \log_{10} V_{OS}/V_{IS} = -40$ dB | 10V | | 10 | | MHz |
| | Crosstalk Between Any Two Channels (frequency at 40 dB) | $R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$<br>$20 \log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3) | 10V | | 3 | | MHz |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay Signal Input to Signal Output | $V_{EE} = V_{SS} = 0V$<br>$C_L = 50$ pF | 5V<br>10V<br>15V | | 25<br>15<br>10 | 55<br>35<br>25 | ns<br>ns<br>ns |
| **Control Inputs, A, B, C and Inhibit** | | | | | | | |
| | Control Input to Signal Crosstalk | $V_{EE} = V_{SS} = 0V$, $R_L = 10\ k\Omega$ at both ends of channel.<br>Input Square Wave Amplitude = 10V | 10V | | 65 | | mV (peak) |
| $t_{PHL}$,<br>$t_{PLH}$ | Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF") | $V_{EE} = V_{SS} = 0V$<br>$C_L = 50$ pF | 5V<br>10V<br>15V | | 500<br>180<br>120 | 1000<br>360<br>240 | ns<br>ns<br>ns |

*AC Parameters are guaranteed by DC correlated testing.

Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF."

## Truth Table

| INPUT STATES | | | | "ON" CHANNELS | | |
|---|---|---|---|---|---|---|
| INHIBIT | C | B | A | CD4051B | CD4052B | CD4053B |
| 0 | 0 | 0 | 0 | 0 | 0X, 0Y | cx, bx, ax |
| 0 | 0 | 0 | 1 | 1 | 1X, 1Y | cx, bx, ay |
| 0 | 0 | 1 | 0 | 2 | 2X, 2Y | cx, by, ax |
| 0 | 0 | 1 | 1 | 3 | 3X, 3Y | cx, by, ay |
| 0 | 1 | 0 | 0 | 4 | | cy, bx, ax |
| 0 | 1 | 0 | 1 | 5 | | cy, bx, ay |
| 0 | 1 | 1 | 0 | 6 | | cy, by, ax |
| 0 | 1 | 1 | 1 | 7 | | cy, by, ay |
| 1 | * | * | * | NONE | NONE | NONE |

*Don't Care condition.

National Semiconductor Corporation

# MF10 Universal Monolithic Dual Switched Capacitor Filter

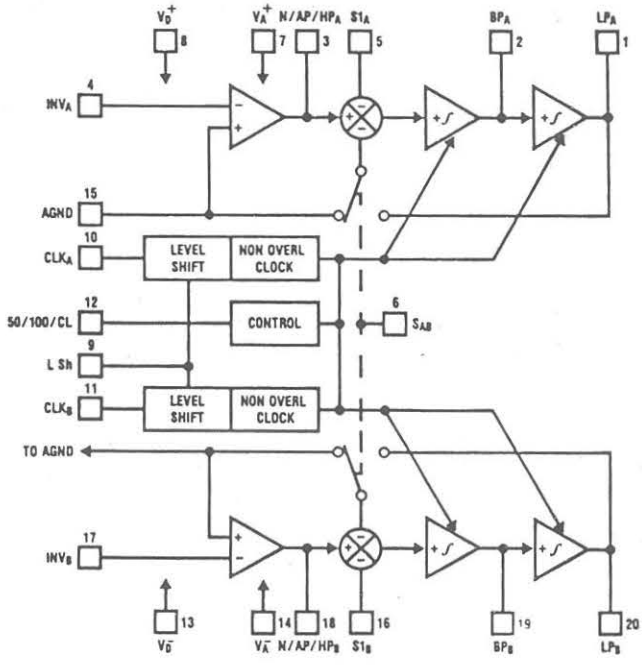
## General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

## Features

- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_o \times Q$ range up to 200 kHz
- Operation up to 30 kHz
- 20-pin 0.3" wide Dual-In-Line package
- 20-pin Surface Mount (SO) wide-body package

## System Block Diagram




Order Number MF10AJ or MF10CCJ
See NS Package Number J20A

Order Number MF10CCWM
See NS Package Number M20B

Order Number MF10ACN or MF10CCN
See NS Package Number N20A

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V^+ - V^-$) | 14V |
| Voltage at Any Pin | $V^+ + 0.3V$ |
| | $V^- - 0.3V$ |
| Input Current at any pin (Note 2) | 5 mA |
| Package Input Current (Note 2) | 20 mA |
| Power Dissipation (Note 3) | 500 mW |
| Storage Temperature | 150°C |
| ESD Susceptability (Note 11) | 2000V |

Soldering Information

| | |
|---|---|
| N Package: 10 sec. | 260°C |
| J Package: 10 sec. | 300°C |
| SO Package: Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (appendix D) for other methods of soldering surface mount devices.

## Operating Ratings (Note 1)

| Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ |
|---|---|
| MF10ACN, MF10CCN | $0°C \le T_A \le 70°C$ |
| MF10CCWM | $0°C \le T_A \le 70°C$ |
| MF10CCJ | $-40°C \le T_A \le 85°C$ |
| MF10AJ | $-55°C \le T_A \le 125°C$ |

## Electrical Characteristics $V^+ = +5.00V$ and $V^- = -5.00V$ unless otherwise specified.

**Boldface limits apply for $T_{MIN}$ to $T_{MAX}$; all other limits $T_A = T_J = 25°C$.**

| Symbol | Parameter | | Conditions | | MF10ACN, MF10CCN, MF10CCWM | | | MF10CCJ, MF10AJ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Typical (Note 8) | Tested Limit (Note 9) | Design Limit (Note 10) | Typical (Note 8) | Tested Limit (Note 9) | Design Limit (Note 10) | |
| $V^+ - V^-$ | Supply Voltage | MIN | | | | | **8** | | | **8** | V |
| | | MAX | | | | | **14** | | | **14** | V |
| $I_s$ | Maximum Supply Current | | Clock Applied to Pins 10 & 11 No Input Signal | | 8 | 12 | **12** | 8 | **12** | | mA |
| $f_o$ | Center Frequency Range | MIN | $f_o \times Q < 200$ kHz | | 0.1 | | **0.2** | 0.1 | | **0.2** | Hz |
| | | MAX | | | 30 | | **20** | 30 | | **20** | kHz |
| $f_{CLK}$ | Clock Frequency Range | MIN | | | 5.0 | | **10** | 5.0 | | **10** | Hz |
| | | MAX | | | 1.5 | | **1.0** | 1.5 | | **1.0** | MHz |
| $f_{CLK}/f_o$ | 50:1 Clock to Center Frequency Ratio Deviation | MF10A | Q = 10 Mode 1 | $V_{pin12} = 5V$ $f_{CLK} = 250$ kHz | ±0.2 | ±0.6 | **±0.6** | ±0.2 | **±1.0** | | % |
| | | MF10C | | | ±0.2 | ±1.5 | **±1.5** | ±0.2 | **±1.5** | | % |
| $f_{CLK}/f_o$ | 100:1 Clock to Center Frequency Ratio Deviation | MF10A | Q = 10 Mode 1 | $V_{pin12} = 0V$ $f_{CLK} = 500$ kHz | ±0.2 | ±0.6 | **±0.6** | ±0.2 | **±1.0** | | % |
| | | MF10C | | | ±0.2 | ±1.5 | **±1.5** | ±0.2 | **±1.5** | | % |
| | Clock Feedthrough | | Q = 10 Mode 1 | | 10 | | | 10 | | | mV |
| | Q Error (MAX) (Note 4) | | Q = 10 Mode 1 | $V_{pin12} = 5V$ $f_{CLK} = 250$ kHz | ±2 | ±6 | **±6** | ±2 | **±6** | | % |
| | | | | $V_{pin12} = 0V$ $f_{CLK} = 500$ kHz | ±2 | ±6 | **±6** | ±2 | **±6** | | % |
| $H_{OLP}$ | DC Lowpass Gain | | Mode 1 R1 = R2 = 10k | | 0 | ±0.2 | **±0.2** | 0 | **±0.2** | | dB |
| $V_{os1}$ | DC Offset Voltage (Note 5) | | | | ±5.0 | ±15 | **±15** | ±5.0 | **±15** | | mV |
| $V_{os2}$ | DC Offset Voltage (Note 5) | MIN | $V_{pin12} = +5V$ $(f_{CLK}/f_o = 50)$ | $S_{A/B} = V^+$ | −150 | −185 | **−185** | −150 | **−185** | | mV |
| | | MAX | | | | −85 | **−85** | | **−85** | | |
| | | MIN | $V_{pin12} = +5V$ $(f_{CLK}/f_o = 50)$ | $S_{A/B} = V^-$ | −70 | | | −70 | | | mV |
| | | MAX | | | | | | | | | |
| $V_{os3}$ | DC Offset Voltage (Note 5) | MIN | $V_{pin12} = +5V$ $(f_{CLK}/f_o = 50)$ | All Modes | −70 | −100 | **−100** | −70 | **−100** | | mV |
| | | MAX | | | | −20 | **−20** | | **−20** | | |
| $V_{os2}$ | DC Offset Voltage (Note 5) | | $V_{pin12} = 0V$ $(f_{CLK}/f_o = 100)$ | $S_{A/B} = V^+$ | −300 | | | −300 | | | mV |
| | | | $V_{pin12} = 0V$ $(f_{CLK}/f_o = 100)$ | $S_{A/B} = V^-$ | −140 | | | −140 | | | mV |
| $V_{os3}$ | DC Offset Voltage (Note 5) | | $V_{pin12} = 0V$ $(f_{CLK}/f_o = 100)$ | All Modes | −140 | | | −140 | | | mV |

## Electrical Characteristics (Continued) $V^+ = +5.00V$ and $V^- = -5.00V$ unless otherwise specified.

**Boldface limits apply for $T_{MIN}$ to $T_{MAX}$; all other limits $T_A = T_J = 25°C$.**

| Symbol | Parameter | | Conditions | MF10ACN, MF10CCN, MF10CCWM | | | MF10CCJ, MF10AJ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typical (Note 8) | Tested Limit (Note 9) | Design Limit (Note 10) | Typical (Note 8) | Tested Limit (Note 9) | Design Limit (Note 10) | |
| $V_{out}$ | Minimum Output Voltage Swing | BP, LP PINS | RL = 5k | ±4.25 | ±3.8 | **±3.8** | ±4.25 | **±3.8** | | V |
| | | N/AP/HP PIN | RL = 3.5k | ±4.25 | ±3.8 | **±3.8** | ±4.25 | **±3.6** | | V |
| GBW | Op Amp Gain BW Product | | | 2.5 | | | 2.5 | | | MHz |
| SR | Op Amp Slew Rate | | | 7 | | | 7 | | | V/μs |
| | Dynamic Range (Note 6) | | $V_{pin12} = +5V$ $(f_{CLK}/f_o = 50)$ | 83 | | | 83 | | | dB |
| | | | $V_{pin12} = 0V$ $(f_{CLK}/f_o = 100)$ | 80 | | | 80 | | | dB |
| $I_{sc}$ | Maximum Output Short Circuit Current (Note 7) | Source | | 20 | | | 20 | | | mA |
| | | Sink | | 3.0 | | | 3.0 | | | mA |

## Logic Input Characteristics Boldface limits apply for $T_{MIN}$ to $T_{MAX}$; all other limits $T_A = T_J = 25°C$.

| Parameter | | Conditions | MF10ACN, MF10CCN, MF10CCWM | | | MF10CCJ, MF10AJ | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Typical (Note 8) | Tested Limit (Note 9) | Design Limit (Note 10) | Typical (Note 8) | Tested Limit (Note 9) | Design Limit (Note 10) | |
| CMOS Clock Input Voltage | MIN Logical "1" | $V^+ = +5V, V^- = -5V,$ $V_{LSh} = 0V$ | | +3.0 | **+3.0** | | **+3.0** | | V |
| | MAX Logical "0" | | | −3.0 | **−3.0** | | **−3.0** | | V |
| | MIN Logical "1" | $V^+ = +10V, V^- = 0V,$ $V_{LSh} = +5V$ | | +8.0 | **+8.0** | | **+8.0** | | V |
| | MAX Logical "0" | | | +2.0 | **+2.0** | | **+2.0** | | V |
| TTL Clock Input Voltage | MIN Logical "1" | $V^+ = +5V, V^- = -5V,$ $V_{LSh} = 0V$ | | +2.0 | **+2.0** | | **+2.0** | | V |
| | MAX Logical "0" | | | +0.8 | **+0.8** | | **+0.8** | | V |
| | MIN Logical "1" | $V^+ = +10V, V^- = 0V,$ $V_{LSh} = 0V$ | | +2.0 | **+2.0** | | **+2.0** | | V |
| | MAX Logical "0" | | | +0.8 | **+0.8** | | **+0.8** | | V |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** When the input voltage ($V_{IN}$) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF10ACN/CCN when board mounted is 55°C/W. For the MF10AJ/CCJ, this number increases to 95°C/W and for the MF10CCWM this number is 66°C/W.

**Note 4:** The accuracy of the Q value is a function of the center frequency ($f_0$). This is illustrated in the curves under the heading "Typical Peformance Characteristics".

**Note 5:** $V_{os1}$, $V_{os2}$, and $V_{os3}$ refer to the internal offsets as discussed in the Applications Information section 3.4.

**Note 6:** For ±5V supplies the dynamic range is referenced to 2.82V rms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μV rms for the MF10 with a 50:1 CLK ratio and 280 μV rms for the MF10 with a 100:1 CLK ratio.

**Note 7:** The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

**Note 8:** Typicals are at 25°C and represent most likely parametric norm.

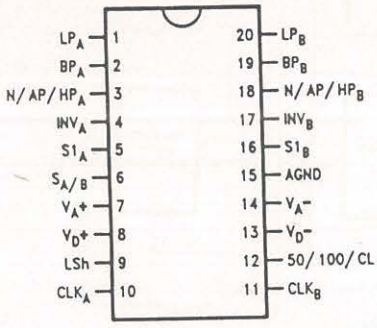
**Note 9:** Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 10:** Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

**Note 11:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.

## Connection Diagram

**Surface Mount and Dual-In-Line Package**




TL/H/5645–18

**Top View**

## Pin Descriptions

LP(1,20), BP(2,19), N/AP/HP(3,18) — The second order lowpass, bandpass and notch/allpass/highpass outputs. These outputs can typically sink 1.5 mA and source 3 mA. Each output typically swings to within 1 V of each supply.

INV(4,17) — The inverting input of the summing op-amp of each filter. These are high impedance inputs, but the non-inverting input is internally tied to AGND, making $INV_A$ and $INV_B$ behave like summing junctions (low impedance, current inputs).

S1(5,16) — S1 is a signal input pin used in the allpass filter configurations (see modes 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).

$S_{A/B}$(6) — This pin activates a switch that connects one of the inputs of each filter's second summer to either AGND ($S_{A/B}$ tied to $V^-$) or to the lowpass (LP) output ($S_{A/B}$ tied to $V+$). This offers the flexibility needed for configuring the filter in its various modes of operation.

intel

# 8253/8253-5
# PROGRAMMABLE INTERVAL TIMER

- MCS-85™ Compatible 8253-5
- 3 Independent 16-Bit Counters
- DC to 2.6 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- Available in EXPRESS
  - —Standard Temperature Range
  - —Extended Temperature Range

The Intel® 8253 is a programmable counter/timer device designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2.6 MHz. All modes of operation are software programmable.

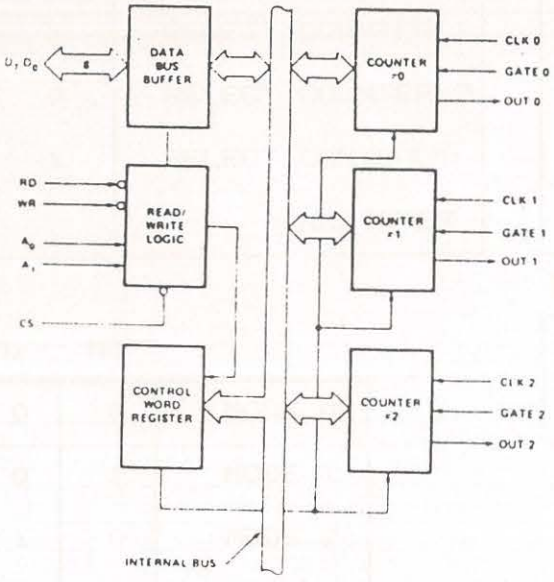



Figure 1. Block Diagram

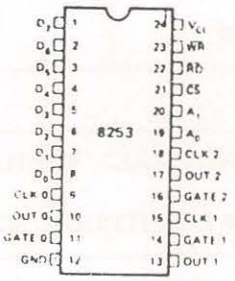



Figure 2. Pin Configuration

The modes of operation for 8253 timer are as shown,

Mode 0 - Interrupt on terminal count,
Mode 1 - Hardware one-shot,
Mode 2 - Pulse generator,
Mode 3 - square wave generator,
Mode 4 - Software triggered strobe,
Mode 5 - Hardware triggered strobe.

The control word format is as shown in the Table D1.

CONTROL WORD

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| SC1 | SC0 | RW1 | RW0 | M2 | M1 | M0 | BCD |

SC - SELECT COUNTER

| SC1 | SC0 | |
|---|---|---|
| 0 | 0 | SELECT COUNTER 0 |
| 0 | 1 | SELECT COUNTER 1 |
| 1 | 0 | SELECT COUNTER 2 |
| 1 | 1 | SELECT CONTROL REGISTER |

RW - READ / WRITE

| RW1 | RW0 | |
|---|---|---|
| 0 | 0 | ILLEGAL |
| 0 | 1 | R/W LSB ONLY |
| 1 | 0 | R/W MSB ONLY |
| 1 | 1 | R/W LSB FIRST MSB NEXT |

M - MODE

| M2 | M1 | M0 | |
|---|---|---|---|
| 0 | 0 | 0 | MODE 0 |
| 0 | 0 | 1 | MODE 1 |
| X | 1 | 0 | MODE 2 |
| X | 1 | 1 | MODE 3 |
| 1 | 0 | 0 | MODE 4 |
| 1 | 0 | 1 | MODE 5 |

BCD

| | |
|---|---|
| 0 | BINARY COUNTER 16 BITS |
| 1 | BCD COUNTER (4 DECADES) |

# APPENDIX E

## PCB LAYOUTS

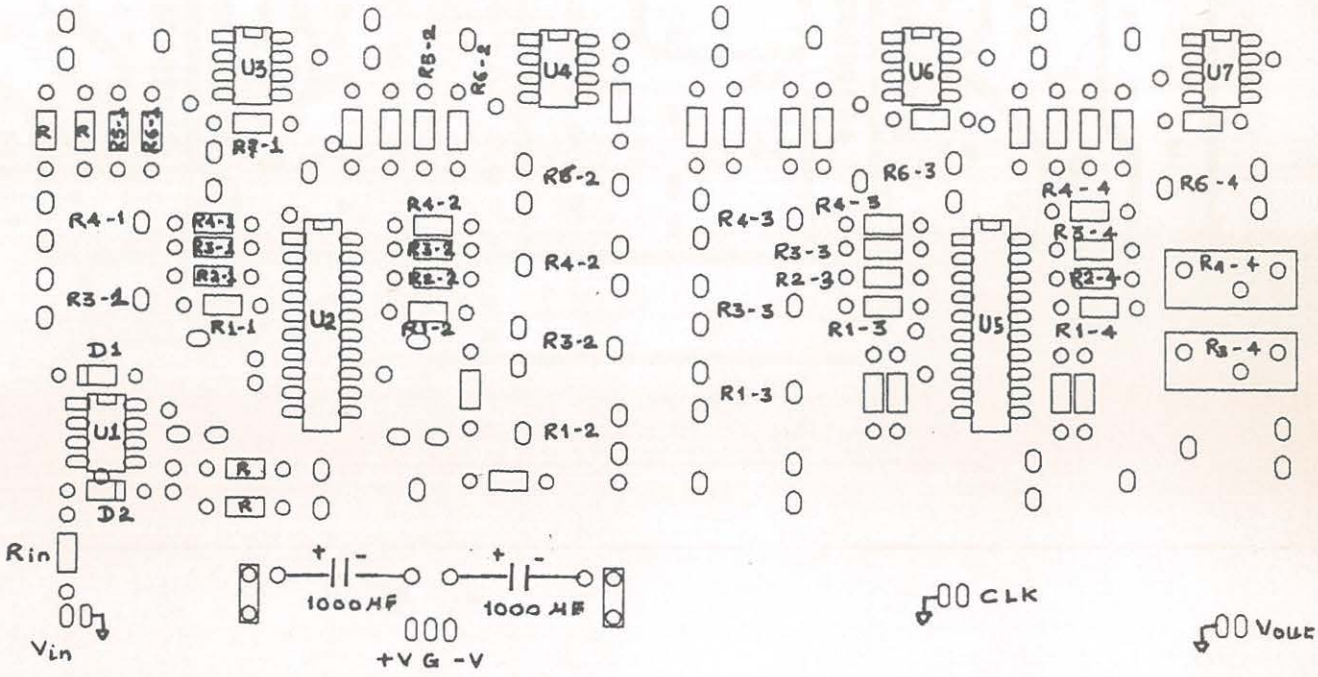
E1. PCB layout of elliptic, Bessel and notch filter.

E2. PCB layout of I/O expansion unit.

## E1. PCB layout of elliptic, Bessel, notch filter.

Same layout gives the required filter depending upon the component values.

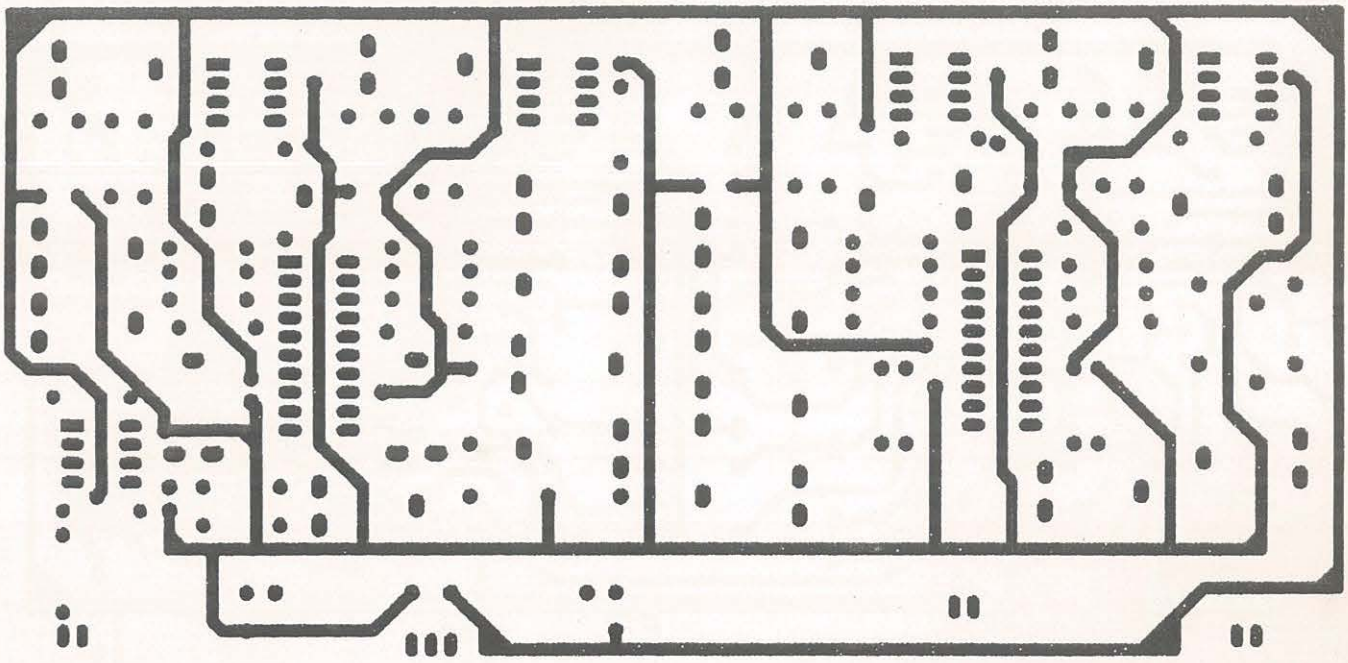
1. Component placement
2. Component side layout
3. Solder side layout



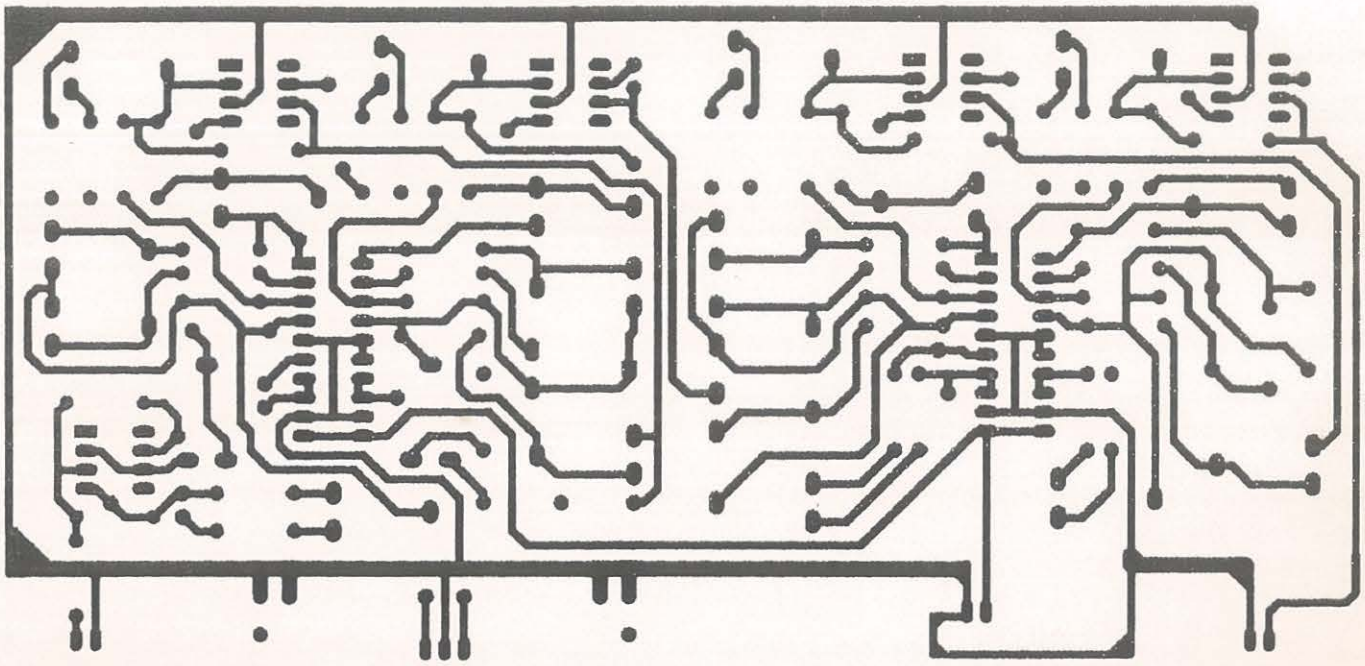

1. Component placement on the filter PCB.

* For Bessel filter the ICs U3, U4, U6, U7, may not be used, or they may be used as unity-gain inverter.

* For notch filter, only the first section consisting of U1, U2, U3, and the corresponding components has been used.



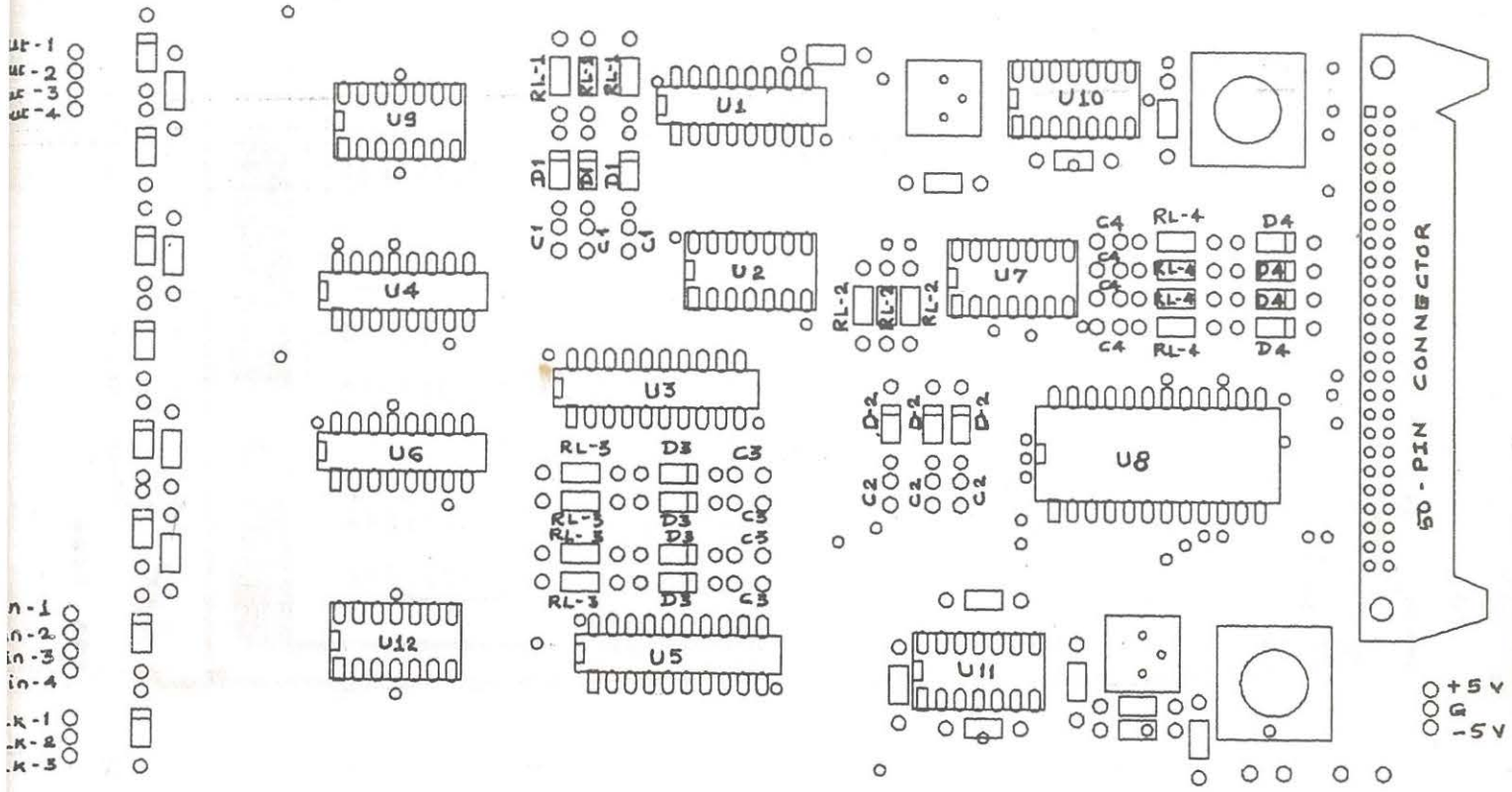
2. Component side layout of filter PCB.



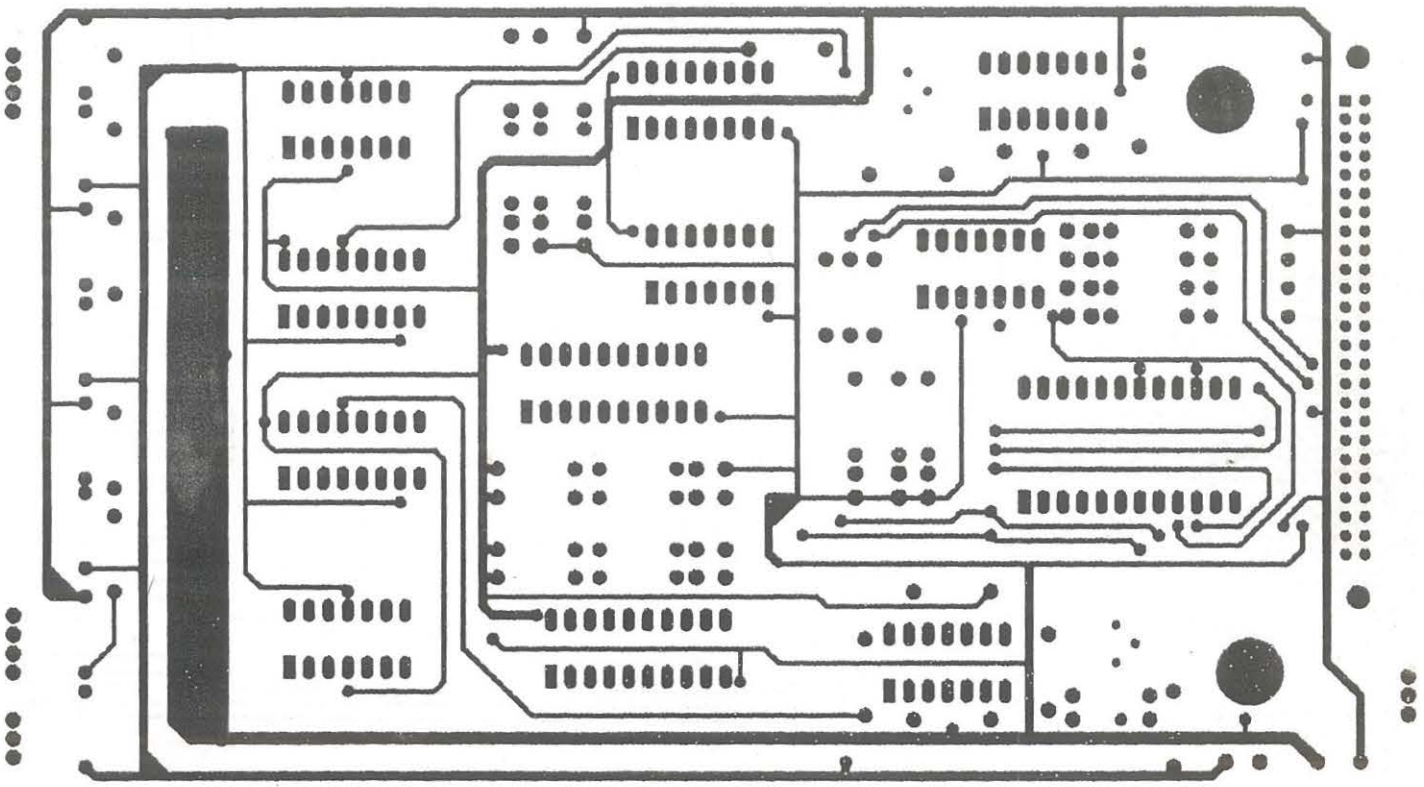
3. Solder side layout of filter PCB.

E2. PCB layout of the I/O expansion unit.

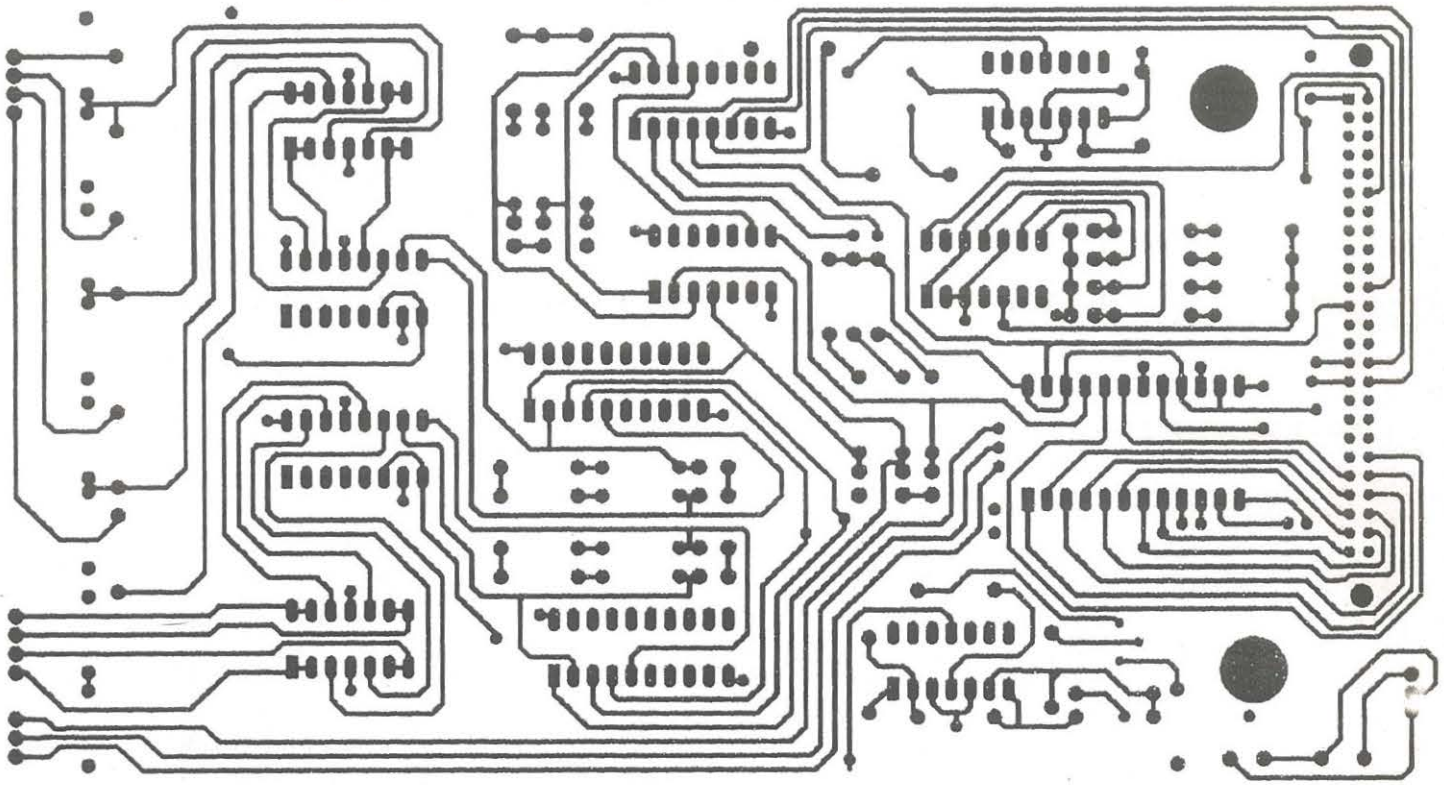
1. Component placement
2. Component side layout
3. Solder side layout




1. Component placement on PCB of I/O expansion unit.



2. Component side layout of PCB of I/O expansion unit.



Solder side layout of PCB of I/O expansion unit.

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