DESIGN AND IMPLEMENTATION OF A SURGICAL DIATHERMY UNIT FOR CLOSED CHEST CATHETER ABLATION

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by

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Abstract

Closed chest catheter ablation is one of the surgical interventions for removing disorders in conduction pathways in the endocardium. The aim of this project is to develop a system for (a) delivering regulated power to the surgical site, (b) monitoring endocardium surface electrograms before and after the ablation, and (c) monitoring electrode-tissue interface temperature for controlling the lesion size created by ablation.

The core of the system is a power modulator with output power of 50 W. A carrier frequency of 500 kHz is amplitude modulated to provide waveforms for three different surgical activities namely: cut, coagulation and blending. The modulating waveforms are generated through a D/A port of a PC add-on data acquisition card. The output of this power modulator is monitored and three different tones are generated for facilitating in identification of the different activities. For finding out the exact site of ablation, the endocardium electrogram amplified by an ECG amplifier is sampled through A/D port of the data acquisition card and monitored on the PC screen. Electrode-tissue interface temperature is monitored through a temperature sensor AD 590 and A/D port of the data acquisition card. This temperature can be used to control the power delivered to the ablation site and thereby to control the size of lesion created. A switched mode power supply has also been developed as required for the power modulator. The power modulator output is isolated from the system ground through a ferrite core transformer.

CONTENTS

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LIST OF FIGURES

CHAPTER 1
INTRODUCTION

The heart provides nutrition, and oxygen through continuous pumping of the blood into the lungs and into the peripheries. It is also, responsible for removing wastes like carbon dioxide from the different body parts. This spontaneous and self-sustaining pumping action of the heart is because, it has a special system:

1. for generating rhythmical electrical impulses, spontaneously, leading to rhythmical contraction of the heart muscle, and
2. for conducting these impulses rapidly throughout the heart resulting in co-ordinated contraction of the myocardium.

This rhythmical, conduction system of the heart is susceptible to damage by heart disease, especially by ischemia of the heart tissues resulting from poor coronary blood flow. The consequence is often an abnormal heart rhythm, along with an adverse effect on the pumping efficiency of the heart.

The adult human heart normally contracts at a rate of about 60-90 beats per minute. Fig.1.1. illustrates the excitatory and conductive system of the heart that controls these cardiac contractions. The figure shows:

A. the S-A node in which the normal rhythmic self-excitatory impulse is generated,
B. the inter-nodal pathways that conduct the impulse from S-A node to A-V node,
C. the bundle of HIS, which conducts the impulse from atria into the ventricles, and
D. the left and right bundles of Purkinje fibers, which conduct the cardiac impulse to all parts of the ventricles [1].

Normally, following excitation of cardiac muscle, there is a relaxation phase, until a new signal begins in the S-A node. However, under certain situations like infarction in the myocardium, this normal sequence of events does not occur. Instead, the cardiac impulse sometimes circulates in the cardiac muscle without stopping. This is the phenomenon called re-entry or the circuit movement [1,2]. This re-entry can cause abnormal patterns of cardiac contraction or abnormal cardiac rhythms that completely ignore the pace-setting effects of the S-A node. This is a totally abnormal situation, and can cause very serious cardiac arrhythmias, including ventricular arrhythmias, in which the heart beats at higher rate than the normal beating rate, with or without co-ordinated contractions of the cardiac muscles.

In the majority of cases, anti-arrhythmic drug treatment is effective in suppressing such arrhythmia [3]. However, approximately 25 percent of patients can not be cured through drug therapy, or develop unacceptable side effects [3]. Therefore, some kind of surgical intervention is required. Surgical interventions such as encircling ventriculotomy have been used in attempts to control medically untreatable arrhythmias [3]. In which, all possible sites of arrhythmogenicity are electrically isolated, from surrounding healthy tissue. For that after opening the ventricle, a perpendicular incision is made in the endocardium along the entire outer limit of the endocardial fibrosis, thus separating infarcted tissue from healthy tissue. However this technique is invasive, risky and may generate more side effects, if incision made is not of proper size. The closed chest cardiac catheter ablation is an useful alternative for encircling ventriculotomy. In which radio frequency current is used for the destruction of the arrhythmogenic biological tissue. This technique can be used for ablation of accessory pathways, created

by infarction in endocardium, in close proximity to critical structures like the AV node or HIS bundles.

1.1 CLOSE CHEST CATHETER ABLATION

In the closed chest catheter ablation, catheter-electrodes are introduced into a vein (e.g. jugular vein) and advanced to the atrio-ventricular cavities, under fluroscopic guidance [4]. The catheter is a hollow tube of variable length and bore, made of one of many substances such as soft or hard rubber, gum, elastic, glass, silver, or even optical fibres. The electrodes at the tip of the catheter can be used for sensing or stimulating. Radio frequency energy is applied through these electrodes for performing the ablation process. Ablation can be performed with DC shocks applied through the catheter. However, this technique has several problems, including variability of the size of the ablation lesion at a given energy setting, production of a pressure wave, and incapability of the catheter to withstand high voltages and currents [5]. By the use of radio frequency alternating current, most of these limitations can be avoided. The radio frequency energy can be supplied through a standard electrosurgical unit. The ablation causes myocardial injury by direct electrical tissue heating as well as by passive heating of contiguous tissue.

Before performing this ablation process, one has to find out the correct site to be ablated. By ensuring that the ablation is localized to the precise area where arrhythmia arises, we can destroy the area completely. Unipolar electrograms derived from the tip electrode at the ablation site can be useful for this purpose. Close contact between the ablation electrode and ablation site may be obtained by fluroscopic inspection, and by observing a high rate of rise of the unipolar electrogram voltage, and

appearance of ST segment elevation in this electrograms [3]. Fig. 1.2 shows the difference between the electrograms derived from normal tissue and arrhythmogenic tissue.

The ablation done by radio frequency energy should be controllable. Otherwise, lesions created by this ablation process, may cover the non-defective site. The control of lesion size can be done by controlling the electrode-tissue interface temperature, This in turn depends on the radio frequency power and time for which it has been supplied. Also, it has been observed during radio frequency ablation, that if temperature of the electrode-tissue interface increases to more than 100°C then it will result in boiling of blood plasma and adherence of denatured plasma proteins to the electrodes. This can be seen by the formation of coagulant and thrombus on the electrode surface as well as occasional adherent on tissue on catheter removal. Coincident with these, a sudden rise in electrical impedance and resultant rapid decline in radio frequency current also is observed [5] which is shown in Fig.1.3. The temperature of the electrode-tissue interface has to be controlled for avoiding any side effects.

1.2 OBJECTIVE

A typical experimental set-up for the cardiac ablation process is illustrated in Fig. 1.4. The overall operation of the system proposed is as follows:

A. Cardiac catheterization - the catheter having tip electrodes is introduced in the vein and advanced to the endo-cardial region, under fluroscopic guidance.
B. Identification of the site for ablation through measurement of endo-cardial electrograms.
C. Having identified the region of ablation, the radio frequency

energy is supplied through the power modulator (electrosurgical unit) which ablates the region by creating lesions.

D. Monitoring of the electrode tissue interface temperature during stimulation for controlling lesion size by regulating the radio frequency power supplied to the ablation site through a temperature feedback system.

The aim of this project is

(a) To develop a system (Electrosurgical Unit) capable of applying radio frequency energy for closed chest catheter ablation.

(b) To provide the ability to determine the exact site for ablation using electrograms and post-ablation monitoring of these electrograms as a measure of the efficiency of the ablation.

(c) To Monitor and control electrode-tissue temperature for limiting lesion size.

The implementation of the system for the closed chest catheter ablation has been divided into following modules:

1. Computer controlled power modulator (Electrosurgical Unit).
2. Power modulator output monitoring.
3. Interface circuitry for data acquisition from catheter electrodes for monitoring electrograms.
4. Electrode tissue interface temperature monitoring and feedback control of radio frequency power supplied from the electro surgical unit.
5. Software development (data acquisition, generation of modulating signals, controlling of radio frequency power, on-line electrogram display on monitor, timer setting and indicating arrangement, feedback program for control of

temperature).

6. Modulator power supply.

1.3 OUTLINE OF THE REPORT

Chapter 2 discusses the functioning of the electro surgical unit (computer controlled power modulator) along with the carrier signal generator and gate drive circuits. Test results are also discussed.

Chapter 3 presents output monitoring circuits, which include the electro surgical output monitoring, electrograms and temperature monitoring at the ablation site.

Software for generating modulating signals and monitoring electrograms and temperature is discussed in the Chapter 4.

Chapter 5 discusses the high voltage d.c. power supply required for the power modulator.

The last chapter presents the summary of this project and also proposes the suggestions for future work.

CHAPTER 2

COMPUTER CONTROLLED POWER MODULATOR

2.1 INTRODUCTION

The computer controlled power modulator is the main part of the surgical diathermy unit and serves the functions of an electrosurgical unit. It provides radio frequency current to generate heat in tissues either by direct application of power to the electrodes in the body or by striking an electric arc. By using appropriate techniques, the rf current can be used to cut tissue and coagulate blood vessels, and thus replaces the conventional scalpel in many surgical applications. This chapter will introduce the power modulator (electrosurgical unit). The design aspects of basic functional circuits of a particular solid state power modulator are also presented here. The output monitoring for different surgical activities of the power modulator is discussed in the next chapter.

2.2 POWER MODULATOR

Electrosurgery uses radio frequency (power) in the range of 100 kHz - 10 MHz [2]. This frequency range is selected to avoid intense muscle activity and the electrocution hazard which occurs if lower frequencies are employed. The action of surgical diathermy machine depends on the heating effect generated by radio-frequency power which is delivered to the patient's body. The high frequency current flows through the sharp edge of a wire loop, or bent loop, or through the point of a needle into tissue, which is ultimately responsible for a very high current density at the delivery point [2]. This point is kept in contact with the

tissue which is to be destroyed. The tissue is heated to such an extent that the cells immediately under the electrode are torn apart due to boiling of the cell fluid. The return path of this high frequency current is through a reference electrode, which establishes a large contact area with the patient so that the return radio frequency current develops very little heat at this electrode. Fig. 2.1 shows the set up for electro-surgery. A typical electrosurgical unit can generate different types of waveforms namely cut, coagulate and blend, depending upon the application.

The overall operation of the electrosurgical unit depends mainly on two factors: the amount of power delivered at the surgical site and the waveform used. Different surgical activities like cutting, coagulating, and blending use different types of waveform for delivering power to the surgical site [6]. The waveforms for the above mentioned activities are shown in the Fig. 2.2. The waveform for cut activity is purely a sinusoidal waveform, and can be obtained by modulating the sinusoidal carrier by a constant level modulating signal. The waveform for coagulation is repeated sinusoidal pulses. It can be obtained by modulating the carrier with a sinusoidal burst of repeated frequency fm. The waveform for blending is the combination of cut and coagulation. The modulating signal for it is the sinusoidal burst with the additional dc superimposed on it. Hence, effectively, the electrosurgical unit generates different amplitude modulated waveforms with power amplification.

From surveying the data sheets and relevant literature we have decided the specifications of the power modulator, to be developed in this project. These are as follow:

1.Output power 50 W.

2.Output voltage 500 V p_p.

3.Frequency of output signal should be 500 kHz.

4.Capable of three different surgical activities, namely:
(a) cut, (b) coagulate, and (c) blend.

5.Output should be isolated from earth.

2.2.1 Circuit of the power modulator

In this unit, the various output waveforms are generated by modulating a 500 kHz sinusoidal carrier with appropriate modulating waveforms. The necessary output power could have been obtained either by using a modulator followed by power amplifier or by using power modulator. In the first case the power amplifier required will have to be biased for amplifying all the frequency components of the modulated signal. So, we can not use class C or upper class power amplifier, which have higher power efficiency. Hence, we have decided to use a power modulator.

The circuit diagram for the power modulator is shown in Fig. 2.3 [6]. Here a BJT is cascoded with a MOSFET. The carrier signal is applied at the gate of the MOSFET. This carrier signal is in a pulsatile waveform. The modulating signal is applied to the base of the BJT. And the resonant circuit is tuned to the the carrier frequency (i.e. pulse repetition rate of the gate drive). The Q-factor of this resonance circuit is adjusted in such a way that it can pass signal of frequency range $f_c \pm f_m$, where f_c is carrier frequency and f_m is modulating signal frequency. Here the output power can be controlled through controlling the base voltage of BJT. Thus by this circuit, both the power amplification and amplitude modulation can be achieved, simultaneously.

We have used the same principle to achieve power modulation, except that the BJT is replaced by a MOSFET. Here, the BJT is replaced by the MOSFET because of (a) relative simplicity

of MOSFET gate drive circuit, and (b) availability of the MOSFET at the required ratings. The circuit diagram for the power modulator is shown in Fig.2.4. Here an n-channel enhancement type power MOSFET is cascoded with another n-channel enhancement type MOSFET. The lower transistor Q_1 is used as a switch, which controls the total conduction time of upper transistor Q_2. This is used as the power controlling device, since the output power can be controlled through its gate voltage. The gate voltage of Q_1 is a pulsatile waveform whose pulse repetition rate is the carrier frequency of the final modulated signal. By varying the duty cycle of this waveform the total conduction period of both the transistors can be varied.

A tank circuit is used at the drain of Q_2. It is tuned at the fundamental frequency of the carrier. The high frequency transformer of the tank circuit acts as a power transfer device to the load connected at its secondary. It also provides isolation between the load and the high voltage power amplification circuit and blocks d.c. current flowing through the load. The diode used between the tank circuit and drain of Q_2 prevents negative voltage on the drain of Q_2. The gate signal for Q_2 is derived from a digital-to-analog port of a data acquisition card with the help of a computer.

As stated earlier, our aim is to design the power modulator which can give the output power of 50 W at 500 kHz frequency, with peak to peak voltage as 500 V. This power is applied to the patient's body through active electrode. The impedance observed between active electrode and reference electrode is approximately 200 Ω, if the temperature of electrode-tissue interface is less then 100 ^{o}C [4]. Therefore the maximum current flowing through the load (here patient's body), and hence through secondary of isolation transformer T1 is 0.5 A.

The primary-to-secondary ratio of the isolation transformer used is 1:1. Therefore, same amount of current will flow through the primary of T_1. This current also will flow through both the switching devices Q_1 and Q_2, and diode D_1. Maximum dc voltage applied to the power modulator is 250 V. Therefore, the maximum blocking voltage across both the switching devices Q_1 and Q_2, and diode D is 250 V. Also the frequency of operation is 500 kHz, both Q_1, Q_2 selected are high speed, higher current capacity, and high voltage capacity n-channel power MOSFETs. Q_1 is of type IRF830, and Q_2 is of type K1357. The data sheets of both Q_1 and Q_2 are shown in the Appendix D. Here, it should be noted that as Q_1 is acting as a switch it should be of switching type MOSFET and Q_2 is acting as power amplifier, it should have sufficient power handling capacity. Also, the output power is directly controlled through the gate voltage of Q_2. So, for lowering the voltage level of this gate voltage Q_2 must have low limit of threshold voltage. The diode D_1 is of type BY26C and have ratings sufficiently higher then required. The data sheet of which is also presented in Appendix D.

The tank circuit is tuned at 500 kHz. Here the inductance of the primary winding of the isolation transformer is approximately 300 μH. So, the capacitance C_1 calculated from formula $f = 1/(2\pi L C_1)^{1/2}$ is 337 pF. The capacitance C_1 selected should have working voltage more then 500 V. We have used C_1 = 330 pF with 680 V working voltage.

The design of high frequency transformer required for tank circuit is given in the Appendix A.

2.2.2 Analysis of the power modulator circuit

The I_d vs V_{ds} characteristics for a n-channel enhancement type MOSFET are shown in Fig. 2.5 and Fig. 2.6 [7]. From these we can see that there are two regions of operation: the triode region and the pinch-off region. The boundary between these two regions is determined by $V_{gd} = V_t$ or equivalently $V_{ds} = V_{gs} - V_t$. Where V_t = gate threshold voltage. In the triode region, the I_d vs V_{gs} characteristic, is shown by

$$I_d = \mathbb{B} [(V_{gs} - V_t)V_{ds} - 1/2V_{ds}^2] \qquad (2.1)$$

where $V_{gs} \geq V_t$ and $V_{ds} \leq (V_{gs} - V_t)$.

In the pinch off region the current I_d is constant for a given value of V_{gs}. This is also called as saturation region, and in this region the current I_d is given by

$$I_d = 1/2\ \mathbb{B}\ (V_{gs} - V_t)^2. \qquad (2.2)$$

where $V_{gs} \geq V_t$ and $V_{ds} \geq (V_{gs} - V_t)$. This relation is shown in Fig. 2.6.

From equations (2.1) and (2.2) it can be seen that drain current is directly dependent on gate to source voltage. Therefore by controlling the gate voltage of the Q_2 the total drain current in the cascoded circuit can be controlled, and the power delivered to the load can be controlled.

The tank circuit is driven by Q_2. The resonance frequency of the tank circuit is given by the equation

$f=1/(2\pi L C)^{1/2}$. The overall efficiency of the power modulator depends on R_p, the effective parallel resistance of the tank circuit, which in turn depends on R_g, the effective dynamic resistance of the driver Q_2. The dynamic resistance of the driver depends on the class of operation. This class of operation directly depends on the total conduction period of the driver MOSFET which can be controlled through the t_{on} period of the gate waveform of the lower MOSFET Q_1. For achieving higher efficiency t_{on} period of this gate waveform should be minimum. But as we go on decreasing the t_{on} period the more and more harmonics will be presented at the output. For filtering out these harmonics the Q-factor of tank circuit should be high enough. Which in turn causes problem in tuning the resonance circuit. So we have to trade off between efficiency and the tuning difficulty of resonance circuit, and accordingly t_{on} of the gate waveform of lower MOSFET Q_1 has to be selected.

2.3.1 Circuit of the carrier signal generator

For generating the pulsatile waveform for the gate voltage of Q_1 the circuit shown in Fig.2.7 is used [8]. Here the principle of positive feedback is used. The LM339 is a high speed quad comparator IC. The capacitor of value 120 pF is connected between the inverting terminal of LM339 and ground. The separate charging and discharging path is provided through diodes and variable resistors. One path, through R_4 and D_1 will charge the capacitor and the other path, R_5 and D_2 will discharge the capacitor. The charging time constant will decide the t_{on} time where as discharging time constant will decide the t_{off} time of the pulsed waveform. The 15kΩ resistance at the output is a pull-up resistor. The total hysteresis of the loop will be set through selection of R_1, R_2 and R_3. The value of all these three resistances is chosen

to be 560 KΩ. Two Schmitt inverters are used at the output for proper wave shaping.

2.3.2 Analysis of the carrier signal generator circuit

To analyze this circuit assume that the output is initially high. For this to be true, the voltage at the negative input must be less than the voltage at the positive input. Therefore, capacitor C_1 is discharged. The voltage at the positive input is given by

$$V_x = \frac{V_{cc} R_2}{R_2 + (R_1 || R_3)} \qquad (2.3)$$

If $R_1 = R_2 = R_3$, then

$$V_x = 2 V_{cc}/3. \qquad (2.4)$$

Capacitor C_1 will charge up through R_4 so that when it has charged up to a value equal to V_x, the comparator output will switch. With the output V_o = GND, the value of V_x is reduced by the hysteresis network to a value given by:

$$V_x = \frac{V_{cc} (R_2 || R_3)}{R_1 + (R_2 || R_3)} \qquad (2.5)$$

$$V_x = V_{cc} / 3. \qquad (2.6)$$

Therefore the charging time and discharging time equations for V_y are given as,

$$V_y = Vmax (1 - e^{-t_{on}/R_4 C_1}) \quad \text{During charging.} \qquad (2.7)$$

$$V_y = Vmax\ e^{-t_{off}/R_5C_2} \qquad \text{During discharge.} \qquad (2.8)$$

Assuming comparator can switch between gnd and $+V_{cc}$ and considering the diode drop:

$$Vmax = 2/3\ (V_{cc} - V_{be}) \qquad (2.9)$$

$$\text{therefore} \qquad 1/[2(1 - V_{be})] = e^{-ton/R_4C_1} \text{ and} \qquad (2.10)$$

$$i/[2(1-V_{be})] = e^{-toff/R_5C_1}. \qquad (2.11)$$

$$\text{therefore} \qquad ton = R_4C_1 \ln [\ 2(1-V_{be})] \qquad (2.12)$$

and

$$toff = R_5C_2 \ln [\ 2(1-V_{be})]. \qquad (2.13)$$

2.4 GATE DRIVE CIRCUIT FOR THE POWER MODULATOR

The MOSFET is essentially a voltage - controlled device. A voltage of specified limits must be applied between gate and source in order to produce a current flow in the drain.The threshold voltage of the upper MOSFET Q_2 is 6.0 V. So, for controlling the drain current of Q_2 and so the controlling of output power it required to have a gate signal of level more then 6 V. We have decided to derive this gate signal from the the digital-to-analog port of data acquisition add_on card. The maximum signal level available from this port is 5 V. Hence, for getting require voltage level, the amplification of this voltage signal is essential. Here, the voltage signal coming out from digital-to-analog port of data acquisition card is first buffered through an opamp and then applied to the gain control circuit.

Also, since the gate terminal of the MOSFET is electrically isolated from the source by a silicon oxide layer, only a small leakage current flows from the applied voltage source into the gate. However, for effective switching of the MOSFET it is necessary to deliver sufficient current to charge the input capacitor in the desired time. This is accomplished simply by having an emitter follower before applying the signal to the gate of Q_2.

2.5 POWER SUPPLY REQUIREMENT

As the output power requirement for the power modulator developed is 50 W maximum, it is necessary to have a power supply of higher wattage rating. Also the voltage level of output is 500 V peak-to-peak and the transformer primary to secondary turn ratio selected is 1:1. The voltage at the transformer secondary switch between +250 V to -250 V. And transformer only couples the ac voltage the voltage level at primary should also be switched in such a way that the ac voltage level at the primary remains 500 V. So, if the dc supply to the tank circuit and so to the power modulator is kept at least at 250 V, then the voltage at the primary can switch between 250 V above and 250 V below from the average level of 250 V, which is a supply voltage. Here, we have neglected the ac losses across the switching devices, during their on time. Hence it is necessary to have a 250 V dc power supply for power modulator. Also the maximum load current is 0.5 A, we have decided to have a dc power supply of 250 V and 0.5 A, output. The maximum power output is hence 125 W. The design and description of this power supply is presented in the chapter 5.

Both the gate drive circuit and carrier signal generator circuit require a +12 V low voltage supply. The gate drive circuit requires the +16 V supply.

2.6 TEST RESULTS AND DISCUSSION

The actual waveforms at the secondary of the transformers are shown in the Fig. 2.10 to Fig. 2.15. Fig. 2.10 and Fig. 2.11 are waveforms required for cutting in no load and load conditions respectively. Similarly Fig. 2.12 and Fig. 2.13 are waveforms for coagulation and Fig. 2.14 and Fig. 2.15 are waveforms required for blending in no load and load conditions respectively. Load used here is a potato. The actual testing on animal is also carried out.

From the waveforms it is clear that when the load is connected at the secondary, the output voltage waveform is not remaining sinusoidal, and also peak to peak voltage level gets reduced. This is because when load is connected the equivalent impedance of tank circuit will be changed, which in turn changes the Q factor of the tank circuit, which in turn changes the wave-shape of the output waveform. Also when the load is connected the current will flow in the secondary. For counter balancing this (current) additional current will also flow in the primary, which will effectively change R_g , the dynamic resistance of the driver. This also changes the Q factor of the tank circuit. Also the load voltage is lower than the no load voltage as some voltage is dropped across R_g.

On the animal testing of this power modulator is carried out and the cutting action is observed on it. The animal selected was guinea-pig. The effect of cutting on guinea-pig was better then that on potato. Coagulation and blending activities are also observed on the potato. In the case of coagulation the effect was not prominent. The probable reason for that is voltage level may

not be sufficient in the case of coagulation, when test is performed on the potato. In the case of blending the effect is observed on the potato. But it is very difficult to separate out the effect of blending activity with that of cutting, visually.

The V_{g2} vs V_{nl} and V_{g2} vs V_{fl} plots are shown in the Fig. 2.16 and Fig.2.17 respectively. Both the plots show that output voltage is directly proportional to gate voltage of upper MOSFET, and so the output power.

CHAPTER 3

OUTPUT MONITORING

3.1 INTRODUCTION

The output of the power modulator is essentially an amplitude modulated waveform. Different modulated signals can be generated from the output of the power modulator, depending upon the type of surgery to be performed. In our case three different activities namely, cut, coagulation and blending are chosen and accordingly three different waveforms are generated from the output of the power modulator.

For facilitating identification of each activity during surgery, an audio tone is generated. It is different for different activities. It is generated by using modulating signals themselves. The modulating signal can available before the output power amplification stage. But it will be better if the modulating signal is derived from the modulated output of the power modulator, since it can also reflect the nonlinearity or improper functioning of the output stage. The modulator output monitoring circuit is built for monitoring the output of power modulator.

For determining the ablation site, the electrograms are monitored. It can also be useful in finding out the effectiveness of ablation process, by post-ablation monitoring. The ECG monitoring circuit is used for that purpose.

The electrode-tissue interface temperature has to be

monitored for controlling the power delivered to the ablation site. For that temperature monitoring circuit is used.

In this chapter the design and description of each of the three monitoring circuits are presented along with power supply required for them. This will be followed by test results for the same.

3.2 POWER MODULATOR OUTPUT MONITORING

A block diagram of the circuit for monitoring the modulator output is shown in Fig. 3.1. An additional secondary winding on the transformer in the modulator tank circuit (T_1 in Fig. 2.1) is used for monitoring the modulator output. By using the additional secondary, the main output, to be used for electro surgery, remains isolated from the monitoring circuit. The monitoring secondary winding is 1 turn only and gives an output of 25 V p_p when the modulator's main output is at 500 V p_p. This is attenuated to input signal level required for monitoring circuitry. In the monitoring circuitry, first the modulating signal is retrieved from the modulated envelope and is given to the modulating signal detection circuit which detects one of the three demodulated signals or no-signal condition and generates one of the four different possible outputs. The outputs Z_1, Z_2, and Z_3 corresponding to the three modulating envelopes of cut, blending or coagulation are used to select one of the three different RC time constants of audio tone generator circuit, which in turn generates one of the three audible tones of 1000 Hz, 500 Hz and 250 Hz respectively [2]. The output of the audio tone generator is given to the speaker through power amplification stage. Control signal Z_4 is used for resetting the output of tone generator

circuit in no-signal condition and thus to ensure no output tone for no input signal to monitoring circuit.

3.2.1 Demodulator

The circuit diagram of the demodulator is shown in Fig. 3.2. It is an envelop detector [9]. A diode D_1 is placed in series with the parallel combination of load resistance R_1 and capacitor C_1. Followed by a first order low pass filter. Here the capacitor will charge to the peak of each carrier cycle and discharge through the resistance R_1. The RC time constant should be adjusted such that load voltage can change fast enough to follow the modulation envelope. A low pass filter made of R_2 and C_2 has been included for further eliminating the effect of carrier from the demodulated output.

3.2.2 Audio indicator

Audio indicator detects the three different waveforms namely cut, coagulation and blending coming out from the power modulator. These waveforms are shown in Fig. 2.1. The waveform for cut is constant level dc signal whereas the waveform for coagulation is a sinusoidal burst of repetition rate of 10 kHz.The waveform for blending is same as waveform for coagulation with dc signal superimposed on it. For coagulation, the modulating envelope change between 0 V to Vp. Thus, the minimum level for coagulation waveform is at zero voltage level, whereas the minimum level for cut and blending waveform is not at zero voltage level. This fact can be used here to detect either waveform is of coagulation or it is of cut or blending. Also, the cut waveform is a constant level dc signal which differs from other two by no ac

quantity in the waveform. This second fact can be used to detect whether the waveform is cut or either coagulation or blending. With consideration of both the differences we can detect whether waveform is of cut, coagulation or blending. All these three waveforms have non-zero average values. These fact can be used for detecting the no-signal condition. The circuit of audio indicator is divided into two different parts: (a) Envelope detecting circuit, and (b) Tone generator circuit. In this sub section both the circuits are discussed.

(a) Envelop classifier circuit

The circuit for detecting the modulating envelop is shown in Fig. 3.3. The output of the demodulator circuit is applied to the input of the comparator U_1, through resistance R_1. Diodes D_1 and D_2 are the protection diodes connected across inverting and noninverting terminals of the comparator U_1, where as Diode D_3 is connected between the inverting terminal and ground. The pull up resistance R_2 is connected between supply voltage and open collector output of the comparator U_1. The output of the comparator U_1 is applied to the passive high pass filter which is followed by an a.c. detector circuit. The passive high pass filter is made up of the capacitor C_1 and the resistance R_3. The two transistors Q_1 and Q_2 are used in the a.c. detector circuit. Here both the transistors are working as the switches. The value of the resistance R_4 and the capacitor C_2 are selected such that the charging time of the capacitor C_2 is very much greater than the time period of input a.c. signal is presented at the base of the transistor Q_1. So, when a.c. signal is presented at the base of the transistor Q_1 during the ON time of the transistor Q_1, the capacitor C_2 will be discharged through the

transistor Q_1 and during OFF time of the transistor Q_1, the capacitor C_2 will not be able to charge up to a level such that the transistor Q_2 can turn on. Therefore, when an a.c. signal whose time period is less then time constant R_4C_2, is presented at the base of Q_1 the transistor Q_2 will not turn on and the output X will be at a high level. If the a.c. signal is not presented at the base of the transistor Q_1, the capacitor C_2 will get time to charge sufficiently to turn on the transistor Q_2 and output X will be at low level.

The output of the demodulator circuit is also applied to the passive high pass filter, made up of the series capacitor C_3 and the parallel resistance R_6. This high pass filter is applied to an a.c. detect circuit, whose output is labeled as Y in the Fig. 3.3.

Both the output X and Y are applied to the logic circuitry, which generate the three different outputs as per the logic level of input X and Y. The logic circuit is made up of two CMOS inverter and three CMOS AND gates. The three different outputs generated from this logic circuit is labeled as Z_1, Z_2, and Z_3. The output Z_4 shown in figure is the output from averaging filter, which is used here to detect no-signal condition.

In the case of cutting and blending signals the output of the comparator U_1 will remain high at the level of the supply voltage. Hence, there is no a.c. signal present at the input of the a.c. detector circuit. Therefore output X will remain at a low level, almost at the ground level. In the case of the coagulating signal, the output of the comparator will switch between supply voltage and ground therefore the output of a.c. detector will

remain high, at the level of supply voltage.

Similarly the output Y of the second a.c. detector circuit will remain at the low level for cutting and at the high level for coagulating and blending. Depending upon the level of X and Y one of the three outputs of the logic circuit will go high. The levels of outputs Z_1, Z_2 and Z_3 with different levels of X and Y are shown in table below:

Input waveforms	X	Y	Z_1	Z_2	Z_3
Cut	Low	Low	High	Low	Low
Blend	Low	High	Low	High	Low
Coag	High	High	Low	Low	High

(b) Tone generating circuit

The circuit for generating tone is shown in Fig 3.4. Each of these three outputs Z_1, Z_2, and Z_3 from envelope detecting circuit is applied to the control pins of the three different analog switches. The inputs of these three analog switches are connected to the supply voltage and outputs are connected to pin 7 of U_5 through three different resistances. The U_5 is a LM 555 and is used as an astable multivibrator. The frequency of the output waveform of it can be controlled through selection of the resistors R_{10}, R_{11}, R_{12}, R_{13} and the capacitors C_6. The resistors R_{10}, R_{11}, and R_{12} will decide the three different tones to be generated. The frequency of tone generated is given by equation

$$T = 0.693\ (R + 2R_{13})\ C_{6} \qquad (3.1)$$

where, $R = R_{10}$ or R_{11} or R_{12}.

The selection of resistors R_{10} or R_{11} or R_{12} in the astable multivibrator circuitry will be decided by the three outputs Z_1, Z_2, and Z_3 of the envelope detecting circuit respectively. Finally the output of the tone generator circuit is applied to a speaker through power amplifier Q_5. The volume can be controlled by potentiometer P_1.

Outputs Z_1, Z_2 and Z_3 from envelope detecting circuit are applied to the tone generating circuit. One of the three analog switches will be turned on and one of the three resistors R_{10}, R_{11} and R_{12} will be selected. And therefore one of the three RC time constants of audio tone generator circuit will be selected and three different audible tones will be generated for three different activities, cutting, coagulating and blending. The table below shows the output tone against the logic levels of output Z_1, Z_2, Z_3 and Z_4.

Z_1	Z_2	Z_3	Z_4	Output Tone
High	Low	Low	High	Tone for Cut
Low	High	Low	High	Tone for Blend
Low	Low	High	High	Tone for Coag
-	-	-	Low	No tone

3.2.3 Test results

Separate testing of audio indicator was performed by applying modulating signals from function generator. For each of the activity namely: cut, coag and blend, an appropriate modulating signal is applied. In each case distinct tone is heard. For each of the three cases the modulating signal should be appropriate for proper audio output. The analysis for each waveform for input range against possible output tone is presented in table below:

TYPES OF WAVEFORM	SIGNAL LEVEL		POSSIBLE OUTPUT TONE
	Min.	Max.	
Cut	> 0.7 V	-	Tone for Cut
	< 0.7 V	< 0.7 V	No tone
Coag	< 0.7 V	> 0.7 V	Tone for coag
	> 0.7 V	> 0.7 V	tone for Blend
	< 0.7 V	< 0.7 V	No tone
Blend	> 0.7 V	> 1.4 V	tone for Blend
	< 0.7 V	> 0.7 V + min. level	tone for coag
	> 0.7 V	< 1.4 V	tone for cut
	< 0.7 V	< 0.7 V + min. level	No tone

3.3 ECG MONITORING

When a depolarization wave transmits through the heart, the electrical current flowing into the heart tissues, spreads all the way to the surface of the body [1]. If electrodes are placed on the body surface, electrical potential generated by the heart can be recorded. The recording is known as the electrocardiogram. By analyzing this ECG, functioning of heart can be predicted. Ischemic heart tissue will not be able to transmit the electrical current generated due to depolarization of the heart. Therefore, if the electrodes are kept in contact with these ischemic zones then electrical potentials will not be developed at the electrode-tissue interface. This fact can be utilized in determining ischemic regions and also the ablation site. It can also be useful for determining the efficiency of ablation process, by monitoring post ablation electrograms.

3.3.1 Circuit of ECG monitoring

The ECG monitoring circuit are basically an ECG amplifier, the circuit for which is given in the Fig.3.5 The catheter electrodes pick up electrical potentials from the endocardial region and apply them to the ECG amplifier. The design of this amplifier is based on considerations of good common-mode rejection. The circuit used here was given by M.Fostik [10]. It is primarily a two stage instrumentation amplifier made with five operational amplifiers. The input amplifiers U_4 and U_5 constitute a differential amplifier with a variable differential gain and unity gain for common-mode signals. Maximum differential

gain is 40 for this stage. The differential gain for this stage is given by

$$1 + \frac{2R_4}{R_6} \qquad (3.2)$$

The first stage gain is limited to 40 to prevent saturation caused by electrode d.c. offset. R_4-C_1 and R_5-C_2 are used to provide desired high frequency cut off of 100 Hz. The second stage is formed by U_6 and U_7 as the same configuration as the first, but it is a.c. coupled at the input using C_3-R_7 and C_4-R_8, which have a value chosen to give a low frequency cutoff at 100 Hz. The differential gain of this stage is set to 25 by adjusting R_{11}. So overall maximum differential gain of amplifier is 1000. U_1 and U_2 are two buffers which connect the electrodes to the two stage differential amplifier. Also the mismatch of the electrode source resistances causes common-mode signal to a differential mode signal due to finite input impedance. It is desirable to reduce this common mode voltage. This can be accomplished by attaching a third electrode to the patient. This electrode provides a low-impedance path between the patient and the amplifier common so that common mode voltage is small. For this a driven right leg circuit is used [11]. Here a third electrode is not connected to the ground directly, because, if the circuit is not isolated, dangerous currents could flow through the third electrode. The output of this ECG amplifier is sampled through data acquisition card and displayed on the computer screen.

3.3.2 Test results

ECG amplifier developed here is tested with applying

sinusoidal signal from the function generator. The results obtained are listed below:

Differential gain Ad = 909
CMRR = Ad/Ac = 93.15 dB
Input impedance = 1.88 MΩ
Output impedance = 389 Ω

The frequency response is shown in Fig. 3.6, and typical ECG waveform derived using surface electrodes is shown in Fig. 3.7.

3.4 TEMPERATURE MONITORING

The sudden rise in the electrical impedance during radio frequency ablation is due to the elevation of electrode-tissue interface temperature above the boiling point [4]. This results in lowering the radio frequency power delivered to the ablation sight. If the electrode-tissue interface temperature is maintained less than 100^{o}C for the duration of energy delivered then boiling of plasma along with its associated impedance rise should not occur. Therefore the continuous monitoring of electrode-tissue temperature is required.

3.4.1 Circuit of temperature monitoring

Here monitoring of electrode-tissue interface is done through a temperature sensor AD 590 which produces an output current proportional to absolute temperature. The data sheet for AD 590 is presented in Appendix C. IT is used as a high impedance current regulator passing 1 μA for every rise of 1 ^{o}C of temperature. The circuit for converting this current to voltage is shown in Fig. 3.8. Here the zener diode is acting as a constant

voltage source. R_2 and R_3 are adjusted for calibration. Here, the temperature sensor will supply the current I_t depending to the temperature. Total current passing through the feedback resistance R_5 and R_6 is I_O and

$$I_O = I_C + I_t \qquad (3.3)$$

where I_C is the current which will be determine by resistance R_2, R_3 and zener voltage Vz. Output voltage is proportional to the current I_O and the feedback resistances R5 and R6.

$$I_c = V_z \; / \; (R_2+R_3) \qquad (3.4)$$

Here the output voltage is set to zero corresponding to an input temperature of 75 ^{O}C. At this temperature the current supplied by the temperature sensor is I_t= 273+75 = 348 μA as per the data sheets. For output voltage to be zero for this particular temperature the current I_C should be same as I_t, so that the output current I_O will be zero at this temperature. If zener voltage is V_z then

$$R_2 + R_3 = \frac{V_z}{I_C} \qquad (3.5)$$

Now for every degree centigrade change in temperature the current I_t changes by 1 μA. For output to be changed 100 mV for every degree centigrade change the resistances R5 and R6 should be selected by

$$R_5 + R_6 = \frac{V_O}{I_O} \qquad (3.6)$$

The values selected are listed in the circuit diagram. Thus the change in output voltage is directly in accordance with the change in input temperature. This voltage is sampled by the data acquisition card during the ablation and the information derived from it is used to control the output power supplied by power modulator.

3.4.2 Test results

The input temperature vs output voltage characteristic for is shown in Fig. 3.9. From the figure it is clear that the characteristic is linear through out the temperature range of interest.

3.5 POWER SUPPLY FOR MONITORING CIRCUITS

The power supply required for various monitoring circuits are as follow:

1. Audio Indicator +12 V.
2. ECG monitoring circuit +12 V and -12 V.
3. Temperature monitoring circuit +12 V and -12 V.

Total current requirements of all three monitoring circuits is 600mA maximum from +12 V supply and 40 mA maximum from -12 V supply.

For meeting this requirement the separate low voltage regulated power supply is designed, which is capable of giving output of +12 V with maximum current output of 1 A and -12 V with maximum current of 100 mA. This power supply is separate from the

low voltage power supply required for the power modulator peripheral circuits.

3.6 ASSEMBLY

All three monitoring circuits are bread boarded and tested separately. Three different PCBs are developed for them. The pcb layouts for all these three monitoring circuits are shown in the Appendix C. Along with components placement. For housing these three pcbs a metal box of size: depth = 9 inches, width = 9 inches, and height = 6 inches has been fabricated.

CHAPTER 4

SOFTWARE

4.1 INTRODUCTION

In the closed chest catheter ablation there are main two activities namely: 1. finding out the ablation site and 2. applying the regulated power to the ablation site found. The ablation site can be found out by monitoring the endocardial electrograms. And the power applied to the surgical site can be controlled by controlling the level of the gate voltage of Q_2 of the power modulator. Also, during the application of regulated power the electrode-tissue interface temperature has to be monitored. For all these activities mentioned above we have decided to use a computer.

The output voltage of the power modulator is the amplitude modulated waveform. This amplitude modulation can be achieved through applying the gate voltage of upper MOSFET Q2 in Fig. 2.3. As from the equations (2.1) and (2.2), it can be seen that the drain current I_d of Q2, and so the output load current is in direct proportion of the input gate voltage of Q2. So, by varying the level of input voltage to gate of Q2, the current level in the output and so the level of voltage developed across the load can be varied.Thus, the gate signal of Q2 does not only act as modulating signal but also it acts as a output power controlling signal. This control cum modulating signal can be generated through hardware also. But it has been decided to generate this modulating signal through D/A port of data acquisition card. For that Dynalog's pc add-on data acquisition card PCL 218 is used.

For finding out the ablation site the electrograms derived from the catheter electrodes has to be monitored. For that the analog output of the ECG amplifier circuitry is sampled through analog-to-digital port of the data acquisition card and the digital data is used to produce the incoming ECG signal on the computer screen.

The electrode tissue interface temperature should not be exceed more than 100 ^{o}C for preventing any abnormal impedance rise [4]. For that electrode-tissue interface temperature has to monitored. For that purpose the output of the temperature monitoring circuitry is sampled through analog-to-digital port of the data acquisition card . The temperature monitored is displayed on the screen and same is used to control the output power of the power modulator through controlling the amplitude of the modulating signal generated.

In this chapter the algorithms for all three computer base activities mentioned, are discussed.

4.2 GENERATION OF THE MODULATING SIGNAL FROM DAC

Three types of modulating signals are to be generated for three different surgical activities. So, the software development for generating the modulating signals is divided into three parts: generation of modulating signal for (a) cut, (b) coagulation, and (c) blending. Here, the modulating frequency is decided empirically and it equal to 10 kHz.

The modulating waveform for cut is a constant level dc signal and waveform for coagulation is the sinusoidal burst of repetition rate of 10 kHz. The waveform for blending is the

addition of cut and coagulation waveforms, which also has repetition rate of 10 kHz.

For generating the any of the three modulating signals describe above, a common procedure adopted is as below:

1. Initialize the data acquisition card. (The details of this data acquisition card is given in the Appendix *)
2. Set the data sending rate on the D/A port, through the pacer setting of data acquisition card.
3. Generate corresponding data set required for generating a particular type of modulating signal.
4. Send generated data set to the D/A port with predetermine sending rate, unless interrupted.

Here, for generating the data sets for all three waveforms a universal equation is used.

$$dt = D\_lvl + \text{ac component} \qquad (4.1)$$

where ac component $= A \sin (2 \pi f_m n T_s)$ if value > 0

$= 0$ if value ≤ 0.

where dt = data that to be sent on A/D port

D_lvl = DC level

A = Amplitude

f_m = Modulating frequency

T_s = sampling interval

n = no of samples

For cut A = 0 so the ac component = 0,

which gives equ. dt = D_lvl.

For coagulation D_lvl = 0 which gives the equ.

$$dt = \text{ac component} \qquad (4.2)$$

Here, f_m = 10 kHz. Total 20 samples are taken during one cycle of period 100 μs. i.e. at every 5 μs interval the data is sampled So, for this case n = 20 and T_s = 5 μS. this data set of 20 data represents the one cycle of sin ($2 \pi f_m n T_s$). But, as from the waveform require for the coagulation,

$dt = A \sin (2 \pi f_m n T_s)$ when $\sin (2 \pi f_m n T_s)$ is positive.

$dt = 0$ otherwise. (4.3)

The value of A controls the amplitude of output modulating signal.

For blending the signal is summation of both cut and coagulation. So, the equation for blending modulating signal is

$$dt = D\_lvl + \text{ac component.}$$

The ac component is calculated as in the case of coagulation.

Ones the data set is generated, each and every data of that data set is sent to the D/A port of the data acquisition card with the predetermine data sending rate. Here, the data sending rate is set to 10 kHz. The amplitude of the output modulating signal can be control through value of D_lvl if the signal is of cut, through value of A if the signal is of coagulation , and through value of D_lvl or (and) A if the signal is of blending.

4.3 MONITORING OF THE ELECTROGRAMS

ECG signals are very low frequency signals having frequency less than 100 Hz. For monitoring this ECG signal, it is sampled through A/D port of data acquisition card. The sampling rate is set to 200 Hz. The signal from ECG amplifier is applied to the one channel of ADC of data acquisition card. The sampling rate is set through the pacer trigger of the data acquisition card. Graphics routine is written to display the sampled value of ECG signal. But for displaying this sample value the proper scaling as to be done as per the graph-mode pixel setting of the monitor. Facility has been provided for changing the sample rate of the incoming signal. Though the graphics routine is slower in execution, the on line displaying of ECG signal is made possible because of low sampling rate. The time interval between two successive sample is 5 ms.

Also, the storage facility is made for storing last one minute data of ECG signal. These data are stored in the file. But for avoiding the data transfer time in the file if the file is in the hard-disk, the virtual disk is created in the working ram. And ECG data are written in the file on that virtual disk. The monitoring of ECG can be terminated through key interruption from key board.

4.4 TEMPERATURE MONITORING

The electrode-tissue interface temperature is monitored continuously, during the generation of modulating signal in stimulation phase. Now for generating the modulating signal from DAC it is essential to send data to DAC at the predetermine sending rate. So, the monitoring of the temperature is done simultaneously with the generation of modulating signal, then it

is a time critical activity. Therefore, for minimizing the time for monitoring, interrupt service of computer is used. Interrupt routine is developed for measuring the temperature from the temperature monitoring circuit. The rate of generation of interrupt for monitoring temperature is set to 20 Hz. Which is 500 times lower then the rate of modulating signal generated. The temperature read from ADC is in the form of voltage. This voltage is converted into temperature using the formula developed in chapter 3, for temperature monitoring circuit.

CHAPTER 5

MODULATOR POWER SUPPLY

5.1 INTRODUCTION

As stated in chapter 2, power modulator requires a high voltage dc supply with following requirements.

1) output voltage of 250 V and a current rating 0.5 amp.,
2) isolation from ac power mains,
3. regulation of output dc voltage against variations in input mains voltage and variation in load current.

These requirements can possibly be met by either a series pass linear regulated supply or by a switching regulated supply.

In a series pass linear regulated supply [12,13], an isolation transformer, steps up or steps down the ac mains voltage to the appropriate value. The secondary voltage is rectified and filtered and then applied to the series pass regulator. Output dc voltage is sampled and applied to the feedback control circuit which provides negative feedback to the series pass regulator for regulating output dc voltage. In this power supply, the isolation transformer operates at the line frequency, and hence size of transformer is relatively large and overall power supply is bulky. Also, efficiency of the series pass linear power supply is low due to the large dissipation of the power in the series pass elements.

Most of these problems are overcome in switching mode power supply (SMPS) [12,13]. Out of several SMPS designs available, one particular type, namely the half bridge converter type was selected for this project. In this chapter, the circuit description of the power supply, selection of components, assembly of the power supply, and test results will be presented.

5.2 CIRCUIT OF THE SWITCHING REGULATED POWER SUPPLY

Fig.5.1 shows a simplified block diagram of a switching regulator power supply, also known as switching mode power supply (SMPS). In this scheme the ac mains voltage is directly rectified and filtered to produce an unregulated dc voltage, which in turn is applied to a switching element. The switch is operated at a high frequency, in the range of 20 kHz to 1MHz, chopping the dc voltage into pulses with a high repetition rate. This pulsatile waveform is fed into the isolation transformer, stepped up or down to an appropriate value and then rectified and filtered to produce the required dc output voltage V_o . This output voltage can be controlled by varying the duty cycle of the chopped waveform generated by making switching element on or off. A portion of this output voltage V_o is monitored and compared against a fixed reference voltage, and the error signal is used to control the on-off times of the switch, and thereby the duty cycle of the chopped waveform. Thus regulation of the output voltage V_o is achieved. Since the switch is either on or off, it dissipates very little power, resulting in a high overall power supply efficiency. Another advantage is that the size of the transformer can be quite small due to high operating frequency.

There are various SMPS circuits, basically differing in the configuration of the switching elements : (1) single switch, (2) half bridge push-pull, requiring two switching devices, and (3) full bridge push-pull requiring four switching devices [13]. The first one is simplest but it suffers from the problem of saturation of the transformer core. We have decided to use half-bridge converter configuration, because of the relative complexity of driving circuits for the full-bridge converter. The switching elements can be BJTs, power MOSFETs, or gate turn-off

thyristers. We have selected MOSFETs as switching elements, because the drive circuits are relatively simple and these devices were available for the required ratings. In the following subsection, we will be discussing the circuit schematic of this power supply in three parts

(a) Input rectifier and filter circuit,

(b) Converter circuit, and

(c) Feedback and control circuit.

5.2.1 Input rectifier, filter, and surge current suppressor circuit

The circuit for input rectifier and filter stage is shown in the Fig. 5.2. Here, the four discrete diodes are used to form a bridge type of full-wave rectifier [13]. When selecting these rectifier diodes, the following specification should be considered:

1) maximum forward rectifier current,

2) peak inverse voltage (PIV) rating,

3) surge current capability.

Rectifier stage is followed by filter. Here two equal valued capacitors are used in series. This connection is employed here for two reasons: This filter stage is followed by converter stage, which is a half bridge type of converter. In which one end of primary of the power transformer has to be connected to a point at a potential half way between input points. The capacitors C_1 and C_2, and resistors R_1 and R_2 provide y_2 at a potential of $V_{in}/2$ with respect to y_3, where V_{in} is the unregulated dc voltage output between y_1 and y_3. This voltage V_{in} is connected to converter circuit. Further, by using two capacitors in series, the voltage rating for each capacitor gets halved. Here, it should be noted

that capacitor value for filtering action is half of the two individual capacitors.

Initially when the ac mains is switched on, the capacitors C_1 and C_2 in the filter circuit will be in the discharged state, and therefore the initial charging current will be limited by dynamic resistances of diodes of bridge rectifier only. This initial charging current called surge current is of a large value. For limiting this surge current, an input surge current suppressor has been devised. Resistance R_5 has been introduced in the charging path of the capacitors. Once the capacitors get charged, this resistance R_5 is shorted by relay Rl_1. The relay Rl_1 is normally remains in off state, when it is not energized. The two ends of resistance R_5 is connected between central terminal and on terminal of the relay Rl_1. So, when the relay Rl_1 is energized, the resistance R_5 will be bypassed. The voltage divider made of R_3 and R_4 samples the unregulated dc voltage V_{in} and the sampled voltage is applied to the switching transistor Q_3 through zener diode Z_1. The transistor Q_3 is used to drive the relay Rl_1. The ratio R_3 and R_4 are adjusted such that when the capacitors C_1 and C_2 are charged fully, the voltage across R_4 will be sufficient to turn on the transistor Q_3. The resistance R_6 limits the current passing through zener diode Z_1 and through base of Q_3. The zener diode Z_1 will ensure that the Q_3 will not turn on before capacitor C_1 and C_2 are charged fully. The diode D_{11} is the flywheel diode and provides path for current when relay Rl_1 de-energizes.

5.2.2 Half bridge converter circuit

The half bridge converter circuit, is shown in Fig. 5.3. It uses two MOSFET switches in push-pull configuration, and is adopted from the circuit using BJTs given in [13]. The unregulated

dc input V_{in} is applied between y_1 and y_3 . y_3 is the reference point for this circuit. The source of Q_1 and drain of Q_2 are connected together at y_4 and this point is connected, through capacitor C_3, to one end of primary of transformer T_1 (which provide isolation as well as transformation). The other end of the primary winding is returned to y_2. During operation, either both devices will be off, or one of them will be on. When Q_1 turns on, point y_4 goes to the line y_1, generating a voltage pulse of $V_{in}/2$. When Q_1 turns off and Q_2 turns on, the polarity of the transformer primary reverses, since it is now connected to line y_3, generating a negative pulse of $V_{in}/2$. The turn-on-turn-off action of Q1 and Q2 therefore will generate a V_{in} peak-to-peak pulsatile waveform, which in turn is stepped up, rectified and filtered to produce the output dc voltage. The voltage stress imposed on each switching device i.e. the maximum voltage across it in off-state is V_{in}. Here Q_1 and Q_2 are n-channel MOSFETs, used as switching devices. The capacitor C_3 will prevent any dc current flowing in transformer, thus preventing core saturation. This dc current could have resulted due to asymmetric operation of switching devices, or due to unbalance in potential differences across y_1y_2 and y_2y_3.

The switching frequency of the MOSFETs is generally kept constant. The rectified and filtered dc output voltage depends on V_{in} and duty cycle of the pulses, and therefore can be controlled by controlling the relative pulse width of the gate voltages. The figure also shows typical gate control waveform and the voltage at y_4 under ideal safe operation of devices.

Diode D_5 and D_6 are the two flywheel diodes and are connected from drain to source of Q_1 and Q_2 respectively. They are used to provide current path for any current in primary of the power transformer, during when the switching devices are off. This

current lags behind the voltage at the primary due to inductive effect of the transformer primary.

The transformer T_1 used here is pulse type of transformer. Which is capable of handling the required power at the frequency of interest. The output voltage from the secondary of power transformer is pulse type of waveform. Since the pulse frequency is generally kept in the range of 20 kHz to 1MHz, the rectifiers used in the converter stage should be capable of operating at this frequency. Here, four diodes are used to constitute a bridge rectifier for rectifying the output pulsatile waveform of secondary of transformer. The rectifier stage is followed by filter stage, which is a LC filter and used here to reduce ripple in the output dc voltage..

5.2.3 Feedback and control circuit

An amount of output voltage is sampled and applied to the feed back and control circuit for regulating the output voltage. This circuit should retain isolation between the primary and secondary side of the transformer T_1. Also it should provide appropriate gate drives for switching devices Q_1 and Q_2. The block diagram of feedback circuit is shown in the Fig. 5.4.

The feedback voltage is converted to the frequency using voltage-to-frequency converter. This is followed by an opto-isolator, and a frequency-to-voltage converter. This arrangement provides dc-to-dc isolation. This feedback signal is applied to the inverting input of an error amplifier. The non-inverting input of the error amplifier is being connected to the reference voltage. The output of the error amplifier is used to modulate the pulse width of the output of pulse width modulator. The outputs of pulse width modulator are used to

control the on and off time of switching devices of the converter circuit, through driver circuitry.

Here as the output voltage increases the voltage to the inverting input of error amplifier of pulse width modulator increases so the amplifier output decreases, which in turn decreases the pulse width. This results in reduction of duty cycle and consequently, a reduction in the relative on-time of both the switching devices. Therefore the average value of output voltage will decrease. Thus we have a negative feedback, which stabilize the output.

5.3 CIRCUIT COMPONENTS IN THE POWER SUPPLY

The design specifications of power supply are set to 250 V and 0.5 A output voltage and current respectively, as mentioned in chapter 2. The regulation of output voltage for this power supply is empirically selected as 1% with variation of input ac mains from 200 V to 250 V and with variation of output load current from 0 to 0.5 A. Also the output ripple factor is aimed to less than 1% with the voltage range and current range are specified for output voltage regulation. As, This power supply is directly operated from ac mains, the unregulated dc voltage input V_{in} to the converter circuit is

$$V_{in} = 2 E_m / \pi \qquad (5.1)$$

where E_m is the peak value of input ac voltage

$$V_{in} = 2 (\sqrt{2} * 230) / \pi \qquad (5.2)$$

therefore $V_{in} = 320$ V

Therefore the chopped signal at the primary of the power transformer T_1 is between $\pm$160 V.
The transformer primary current can be calculated by the following formula [13]

$$I_c = \frac{P_{out}}{\eta \, \delta_{max} \, V_{in}} \qquad (5.3)$$

where P_{out} is the output power
η is the converter efficiency
δ_{max} is the maximum duty cycle

Typical values for η is 0.7 and δ_{max} is 0.9.

The primary current for above values is 0.62 A. This primary current will flow through the switching devices. Also the maximum blocking voltage across each device is V_{in}, therefore the switching devices selected, must have current rating more then 0.62 A and voltage rating more then 320 V.

The selection of circuits components for this power supply will be discussed in three parts as in previous section.

5.3.1 Circuit components in input rectifier, filter and surge current suppressor circuit

With output power P_{out} = 125 W, and assumed efficiency η = 0.7 after input rectifier stage

$$P_{in} = P_{out} / \eta = 178 \text{ W, and} \qquad (5.4)$$

the input current for the bridge rectifier,

$$I_{in} = P_{in} / V_{in} = 178 / 320 = 0.55 \text{ A.} \qquad (5.5)$$

Current flowing through each diode of input rectifier is thus 0.55 A and maximum blocking voltage is maximum input voltage from ac mains. Four diodes selected for input rectifier are of type 1N 5404. They have maximum forward rectification current capability of 3 A, peak inverse voltage blocking capability of 600 V and surge current capability of 30 A.

Assuming that the design can tolerate a ripple of 25 V peak-to-peak and that the capacitor has to maintain the voltage level for every half cycle (10 ms), the capacitance for input filter can be calculated from the formula [9]

$$C = I\ t / \Delta V = 0.55\ (10 * 10^{-3}) / 25 = 220 * 10^{-6} \text{ F} \qquad (5.6)$$

Since C is made of C_1 and C_2 in series, the required value are $C_1 = C_2 = 2C = 440\ \mu F$. As both the capacitors are in series the voltage stress across each capacitor will be $V_{in}/2 = 160$ V. Here, C_1 and C_2 are 470 μF each, with working voltage of 400 V.

R_1 and R_2 are bleeder resistances of 10 K value each, which provides the discharge path to the capacitors C_1 and C_2 when input mains is switched off. Total discharge time for each capacitor is 10 K * 470 μF = 4.7 s. The wattage capacity of each resistance should be $(160\ V)^2 / 10\ K = 2.56$ W. The selected resistances have wattage capacity of 10 W.

In the surge current suppressor circuit, the relay Rl_1 is 12 V, 150 Ω relay. The minimum current required to energize

this relay is 12/150 = 0.08 A. The transistor Q_3 is BEL 100N transistor with maximum collector current = 1 A. The power supplied to the collector of Q_3 is +12 V. For limiting the maximum collector current to 0.1 A, the resistance R_7 is selected to be 12/0.1 = 120 Ω. The zener diode is of 5.6 V value. R_3 is 33 K and R_4 is 5 K. For unregulated voltage V_{in} = 320 V, the voltage across R_4 is (320 * 5)/38 ≃ 42 V. For selecting R_6 the equation $VR_4 = VR_6 + V_z + V_{be} + VR_7$ is used. Here, V_z = 5.6 V, V_{be} = 0.7 V, VR_7 = (0.08 * 120 Ω) = 9.6 V. So, VR_6 ≃ 26 V. The base current of Q_3 is 0.1 mA. So, the value R_6 = 26/0.1 = 260 K. We have used R_6 = 270 K. The flywheel diode D_{11} is BY 126 diode.

5.3.2 Circuit components in half bridge converter circuit

The transformer primary current will pass through both the switching devices Q_1 and Q_2. Also the maximum blocking voltage on each device is V_{in}. The frequency of switching for these switching devices is 50 kHz in this power supply. Here Q_1 and Q_2 are selected MOSFETs of type K1357, which has maximum current capacity of 3 A and maximum drain to source voltage capacity is 800 V. It can be operated up to 3 MHz of switching frequency.

Series capacitor C_3 will prevent the dc bias to the transformer, thus preventing the core saturation. The series capacitor C_3 should handle the full primary current. This capacitor forms a resonant circuit with the output filter inductor. The resonance frequency of which is given by

$$f_R = 1 / 2 \pi (L_R * C_3)^{1/2} \qquad (5.7)$$

where f_R is the resonance frequency

L_R is Reflected filter inductance.

The reflected filter inductance to the transformer primary is

$$L_R = (N_p/N_s)^2 L \qquad (5.8)$$

where L is the output filter inductance. Therefore

$$C_3 = \frac{1}{4\pi^2 f_R^2 (N_p/N_s)^2 L} \qquad (5.9)$$

In order for charging of the coupling capacitor C_3 to be linear, the resonance frequency must be chosen to be well below the converter switching frequency [13]. For practical purpose

$$f_R = 0.25\, f_s \qquad (5.10)$$

where f_s is converter switching frequency.
Here,

$f_s = 50$ kHz
$f_R = 12.5$ kHz
$N_p/N_s = 1/1.75$
$L = 14\ \mu H$

therefore $C_3 = 0.35\ \mu F$.
Here, C_3 has a selected value = 0.2 μF (two 0.1 μF capacitor in parallel).

Both the diodes D_5 and D_6 are switching diodes and capable of switching at the frequency of operation which is 50 kHz in our case. Both D_5 and D_6 are of type BA159.

As the output dc voltage required is 250 V dc, the maximum voltage swing required before rectification is $\pm$250 V at secondary of the power transformer if the input to primary of

power transformer is of square wave type. Considering the maximum duty cycle of chopped pulsatile waveform at primary is 0.9 the required secondary voltage at the secondary of power transformer is $\pm 250 / 0.9 \simeq \pm 280$ V. Therefore, primary to secondary turn ration required is 320/560 = 1/1.75.

The frequency of operation has been selected to be 50 kHz, hence ferrite core, in which losses at high frequency are low, is used in the transformer core. The transformer has been designed for 125 W power. The details on transformer core is presented in Appendix A.

The maximum load current is 0.5 A. This current will flow through the diodes of output rectifier. Also maximum peak to peak secondary voltage of power transformer is 560 V. Therefore maximum blocking voltage across each diode is 560 V as the bridge type full wave rectifier is used. Here diodes selected have forward current capacity of 3 A, with peak inverse voltage blocking capacity of 800 V and capable of operating at 50 kHz frequency. The BA159 type diodes are selected.

LC type filtering circuit is used at the output for removing the ripple from the output dc voltage. For ripple less then 1 % value of inductor selected is 14 μH and the value of capacitor C_4 can be calculated from the formula [9]

$$\gamma = 0.47 / (4 \omega^2 L C_4 - 1) \qquad (5.11)$$

where γ is the ripple factor for LC type filter [9]

ω is the frequency of operation

For $\gamma = 0.01$ and $\omega = 50$ kHz, $C_4 \simeq 10$ μF. Here C_4 is of value 40 μF with working voltage of 500 V.

5.3.3 Circuit components in feedback and control circuit

The block diagram for feedback and control circuit is shown in Fig. 5.4 and discussed early in subsection 5.2.3. The function of this circuit is to control the duty cycle of the gate drive of the converter MOSFETs, so that the output dc voltage is maintain constant, for varying input ac mains voltage and varying load current. This is to be achieved by comparing a sample of output voltage with a fixed reference voltage. Here we have selected a reference voltage of 2.5 V. Here R3 is selected as 50 K resistance. Where as R_4 is variable resistance of 10 K value. The value of R4 can be adjusted such that the output from sampler is 2.5 V.

For voltage-to-frequency conversion, we have used VCO part of the PLL chip, CD 4046 IC (National Semiconductor). Its output is a square wave, whose output frequency depends on the input voltage, capacitor C_5 and resistance R_5. The voltage-to-frequency characteristic is as shown in the Fig. 5.6, for C_5= 0.01 μF and R_5= 10 K.

The square wave output of the voltage-to-frequency converter is applied to to the frequency-to-voltage converter through opto-isolator in order to achieve dc-to-dc isolation. Opto-isolator of type 6N 136 is used here for isolating the output from input. Buffer IC CD4041 is used before applying the output of opto-isolator to the frequency-to-voltage converter.

The frequency-to-voltage converter used here is LM 2917 (National Semiconductor). Whose output voltage is proportional to the input frequency. Here, as the voltage input to voltage-to-frequency converter varies, the frequency input to the frequency-to-voltage gets varied. Now, for achieving the same

variation in the output voltage of frequency-to-voltage converter it is necessary to linear relationship between voltage input to the voltage-to-frequency converter and voltage output from frequency-to-voltage converter. This relationship is graphically represented in Fig.5.7.

For pulse width modulation, we have used LM 3524 (National semiconductor). It generates two different outputs pulsatile waveforms, duty cycle of which can be controlled through input voltage. The internal block diagram of this pulse width modulator is shown in Fig. 5.8. This chip has an error amplifier whose inverting input is connected to the output of dc-to-dc isolation circuitry and non-inverting input is connected to the fixed reference voltage. The chip also as an internal oscillator, whose frequency can be selected by the external R and C components, in Fig. 5.5 is R_{14} and C_8 respectively. The output frequency of this oscillator is given by formula $f = 1/R_{14} C_8$. We have selected value of R_{14} as variable resistor, so that this frequency can be altered. The current value is set to 50 kHz. Depending upon the difference between two inputs of error amplifier, the output duty cycle will vary. Here, maximum duty cycle for output pulsatile waveform is 45 % and both the outputs are never be at high level at a time.

Though MOSFET is voltage driven device, due to gate-to-source capacitance, the gate current require should also be appropriate, for proper operation of MOSFET. Also, in half bridge type of converter Q1 requires floating point gate drive. For meeting both these requirements the MOSFET driver IR2110 (International Rectifier) is used. It is a monolithic high voltage and high speed dual driver with independent floating high side and fixed low side reference output channels. Its inputs are compatible with CMOS outputs or with LSTTL outputs using pull up

resistors. The dual outputs is applied to the gate of both the switching devices. The data-sheet for this MOSFET driver is given in the Appendix D.

5.4 POWER SUPPLY FOR FEEDBACK AND CONTROL CIRCUIT

The feedback and control circuit also provides dc-to-dc isolation for maintaining the isolation achieved by isolation transformer in the converter circuit. For maintaining this isolation it is necessary to have isolated power supplies for both side circuitry of opto-isolator. The reference point for vtof and input side of opto-isolator is the circuit ground z_2. Where as reference point for output of opto-isolator and rest of the feedback and control circuitry is reference point y_3. So, the power supplied to frequency-to-voltage converter and to input side of opto-isolator is with respect to circuit ground z_3 and that for remaining circuitry of feedback and control circuit is with respect to reference y_3.

The circuit diagram of both the power supply is shown in Fig 5.9. The input power is derived from the ac mains with isolation cum step down transformer. For avoiding two different input transformers a signal transformer is used with two separate secondaries. As, the output voltage level of both the power supplies are same, the VA ratings of both the secondaries are also same. Both the secondaries outputs are applied to two separate bridge type of full wave rectifiers, which in turn followed by capacitor type of filters. For getting regulated output voltage, the outputs from filters are applied to the 3 pin IC regulators.

This feedback and control circuit typically requires +12 V power supply on either side of opto-isolator with respect to corresponding references. This is the output from 3-pin regulator.

Here, we have used LM7812 as 3-pin regulator, which requires minimum 2.5 V voltage difference between its input and its output, for proper regulation action of output voltage [14]. So, the unregulated output ur1 is at least 12 + 2.5 = 14.5 V. This is the voltage output from capacitor filter. Which is given by $2V_m/\pi$, where V_m is the maximum output voltage of secondary voltage. for $2V_m/\pi$ = 14.5 V, V_m comes out to be 22 V. And so the voltage rating of both secondaries is from o to $V_m/\sqrt{2} \simeq 15$ V. The current rating for both the secondaries selected is 1 A. As the bridge type full-wave rectifier is used the maximum blocking voltage across each diode is equal to V_m = 22 V. Here 1N4001 type of diodes are used for constituting bridge rectifier. The diode selected have maximum blocking voltage is 100 V and maximum forward current limit is 1A. For capacitor filter 1000 μF capacitor with working voltage of 50 V is used.

5.5 ASSEMBLY AND TESTING

All three circuits of power supply are first assembled and tested separately, and mounted on different PCBs. Each of the input rectifier and filter circuit, and the feedback and control circuit are mounted on a single PCB, where as the half bridge converter circuit is mounted on two different PCBs. A metal box of size: depth = 355 mm, width = 305 mm and height = 152 mm (14 * 12 * 6) is fabricated for housing all these PCBs. The low voltage power supply for feedback and control circuit is also assembled, tested. It also housed in the same metal box.

The output voltage obtained from the power supply is observed for half an hour. It was remained constant at 250 V without any significant heating of the components used.

The ripple shown at the output was 4 V peak to peak.

Therefore the ripple factor is 4/250 = 0.016.

Variation in output voltage is observed for change in input ac mains voltage. It has been observed that the output voltage remains constant for the input voltage variation in the range of 190 V to 255 V. Thus the regulation of output voltage is achieved for this range of input variation.

With load the output voltage regulation is achieved for the range 0 to the 0.3 amp. of load current.

The insulation testing between terminals x_1 and z_2, x_1 and z_2, x_2 and z_1, and x_2 and z_2 is carried out with the meager. In all cases it is more then 500 MΩ.

CHAPTER 6

SUMMARY

6.1 INTRODUCTION

The closed chest catheter ablation is one of the surgical interventions for removing conduction pathaways, which are responsible for life threatening tachycardias. This can be achieved by applying radio frequency (RF) energy to electrode, introduced into the endocardium through cardiac catheterization. The RF can be supplied through an electrosurgical unit. But for avoiding complications, it is necessary to control the size of the lesion created during ablation process. This lesion size is dependent on the electrode-tissue interface temperature and temperature is dependent on RF power delivered. The aim of this project is to develop a system which can be used for controlled supply of RF energy to ablation site through monitoring of electrode-tissue interface temperature. Also it can be useful for monitoring the endocardial surface electrograms before and after the ablation, which can be useful for finding out the correct site for ablation, and for evaluating the efficiency of the ablation.

6.2 SYSTEM DEVELOPED

System for closed chest catheter ablation is proposed in the block diagram form. The system development had been divided in number of small modules:

1. Computer controlled power modulator (Electrosurgical Unit).
2. Modulator output monitoring.
3. Interface circuitry for data acquisition from ECG and temperature monitoring circuits.

4. Software development for generating modulating signal, control of output power, monitoring and display of ECG and temperature.
5. Modulator power supply.

In the computer controlled power modulator, three different modulated signals namely: cut, coagulation, and blending are generated. The design objective was to get output of power modulator to 500 V p-p at 500 kHz with the maximum power output power 50 W. The actual output achieved from the power modulator is 500 V p_p at 415 kHz. The frequency of output signal is different from specified frequency because of tolerances in the transformer primary inductance value and capacitor value of the tank circuit.

The modulating signals for these power modulator are generated by software with the help of data acquisition add_on card. These modulating signals are interfaced to the power modulator with the help of gate drive circuitry, discussed in Chapter 2. The output of the power modulator is an amplitude modulated signal. By controlling the level of these modulating signal voltage level of output can be controlled. Hence the output power can be controlled through these modulating signals.

For facilitating the identification of different surgical activities the output of power modulator is monitored and three different tones are generated for these three different surgical activities. For that a small voltage level signal is obtained by incorporating another secondary winding of lesser turns along with the main secondary winding of the output power transformer of the power modulator. Modulating signals are derived from the modulated output signal of the power modulator, and applied to audio indicator circuitry, which in turn, can produce three different tones, by decoding these modulating signals.

For controlling the lesion's size, created by application of this radio frequency power, it is necessary to control the electrode-tissue interface temperature. For that temperature monitoring circuit is built, which monitors the temperature at the electrode-tissue interface and provides the temperature information to the computer through data acquisition card. The information of this temperature is used to control the output power for controlling the electrode-tissue interface temperature.

For identifying the actual surgical site in the closed chest catheter ablation, the electrograms are monitored, for that the ECG monitoring circuit is developed. The monitoring of these electrograms will also be useful in knowing effectiveness of the ablation process.

As the output power of power modulator varies with variation in the types of surgery, and therefore current drawn varies. therefore it is necessary to have a regulated power supply. The switched mode regulated power supply of 125 W is designed for this purpose. The power required for other peripherals of power modulator and for monitoring circuits are met through separate low voltage power supplies.

6.3 APPLICATION TESTING

The testing for each module was carried out. The test results for each module have been presented in respective chapters. The testing of whole system was also carried out by integrating each and every module. Due to practical limitation of testing and non-availability of catheter with temperature sensor

mounted on it, the actual closed chest catheterization could not be done.

The radio frequency power generated by the power modulator can be applied to the surgical site through catheter electrodes configuration or by simple electro surgical electrodes, depending upon requirements. The testing of this power modulator was done on vegetables namely: potato and tomato and also the testing is carried out on the animal (Guinea-pig). The subject under testing had been put on the reference electrode and the rf power from the power modulator had been applied through the needle type active electrode, under the control of computer. Different surgical activities, duration of power and maximum electrode-tissue interface temperature had been supplied to the computer. In both the vegetable and the animal testing the cutting and blending effect is observed, but it was difficult to isolate them visually. It was also noted here that the effect of tissue destruction observed was better on the animal than on the vegetable. The coagulation effect was observed but it was not prominent. The animal testing was done on the tissues of intestine, on the muscle tissues and on the skin tissues.

The testing of ECG monitoring circuitry is done by taking surface electrograms. The ECG monitoring circuitry is designed for monitoring the ECG signals from the endocardium. The signal amplitude of ECG picked up from endocardium has higher amplitude than the ECG picked up from surface of the body. Gain of ECG amplifier is set corresponding to the endocarium ECG signal.

The temperature of electrode-tissue interface is also monitored, but not during the application of RF power, as excessively high voltage generated at the electrode-site, during application of RF power, can cause failure of low voltage circuit

components in the temperature monitoring circuit.

The generation of modulating signal from data acquisition card of computer is also observed, with corresponding output from power modulator. The results are as per expectation. Also, the control of output power of the power modulator can be carried out by controlling the level of modulating signal is observed. The results are satisfactory, and after certain threshold level the power output is totally controllable through level control of modulating signal.

The power required for power modulator is supplied through the switching mode power supply designed. The power supply is tested during no-load and load conditions. The results are well within the tolerance range.

6.4 SUGGESTIONS FOR FUTURE WORK

The specifications for the power modulator are chosen to meet the requirements of radio frequency power in the closed chest catheter ablation. But if the same power modulator is to be used as normal electrosurgical unit, available commercially, it is necessary to increase the power level of output signal of power modulator. Also for improving the performances of the different surgical activities: cut, coagulation, and blending, the voltage levels of output waveforms must be increased [2]. For that the secondary turns of the output power transformer of power modulator have to be increased. But that increase will increase the current ratings on the primary side. Which in turn increases the current ratings of switching devices at the primary side. Here, we have used the switching devices at the primary of power transformer of 6 time more capacity than output current specified in our case. So, when increasing the secondary turns, the current limitation of

components used in power modulator has to be considered along with the consideration of output power requirement from the power supply.

The temperature sensor used here is not an electrically, isolated. Due to that when the high voltage radio frequency signal is applied to the surgical site, the temperature can not be measured simultaneously, because it can damage the low voltage temperature monitoring circuitry. Actually, in practical implementation of closed chest catheter ablation, a catheter having thermister mounted on can be used. The thermister of which is electrically isolated but thermally conductive from the electrode. So, by having this type of catheter it is possible to monitor temperature during application of RF power, and thereby a closed loop control system for controlling radio frequency power can be ensured. Also, the temperature monitor circuit can be modified such that it can be protected from high voltage.

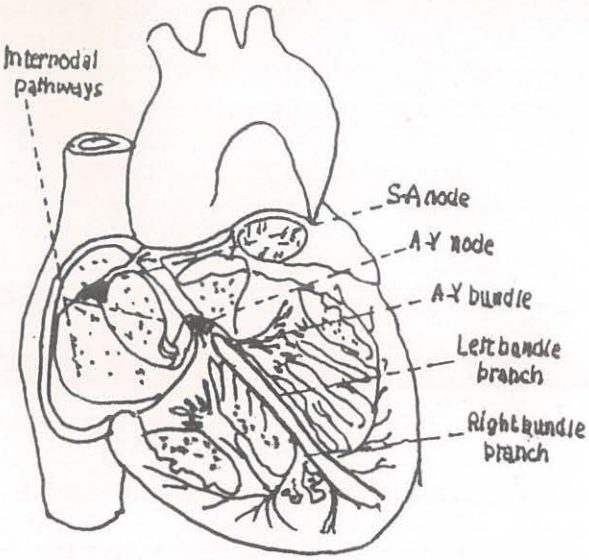


Fig. 1.1 Inter nodal pathways in the heart (adopted from [1])

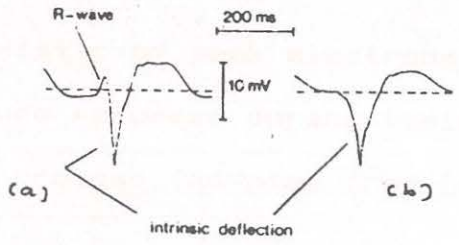


Fig. 1.2 Unipolar cardiograms recorded from endocardium
(adopted from [14])
(a) during ventricular tachycardia
(b) some distance away from position of
ventricular tachycardia

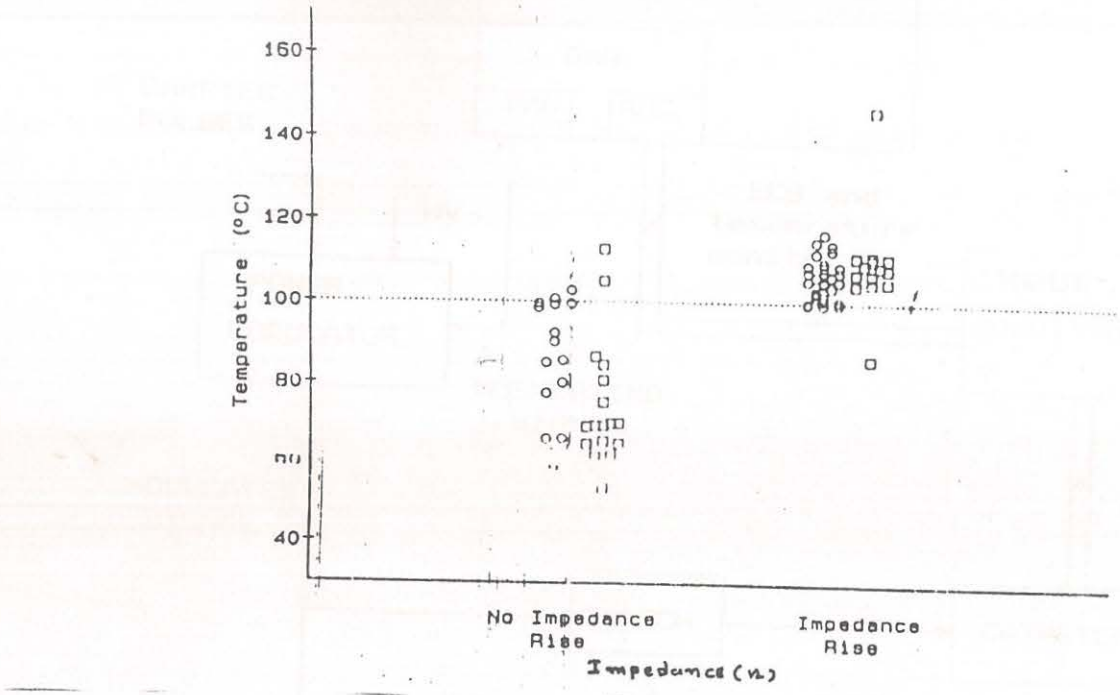


Fig. 1.3 Characteristic of peak electrode-tissue interface temperature recorded during lesion production in ablation process (adopted from [6])

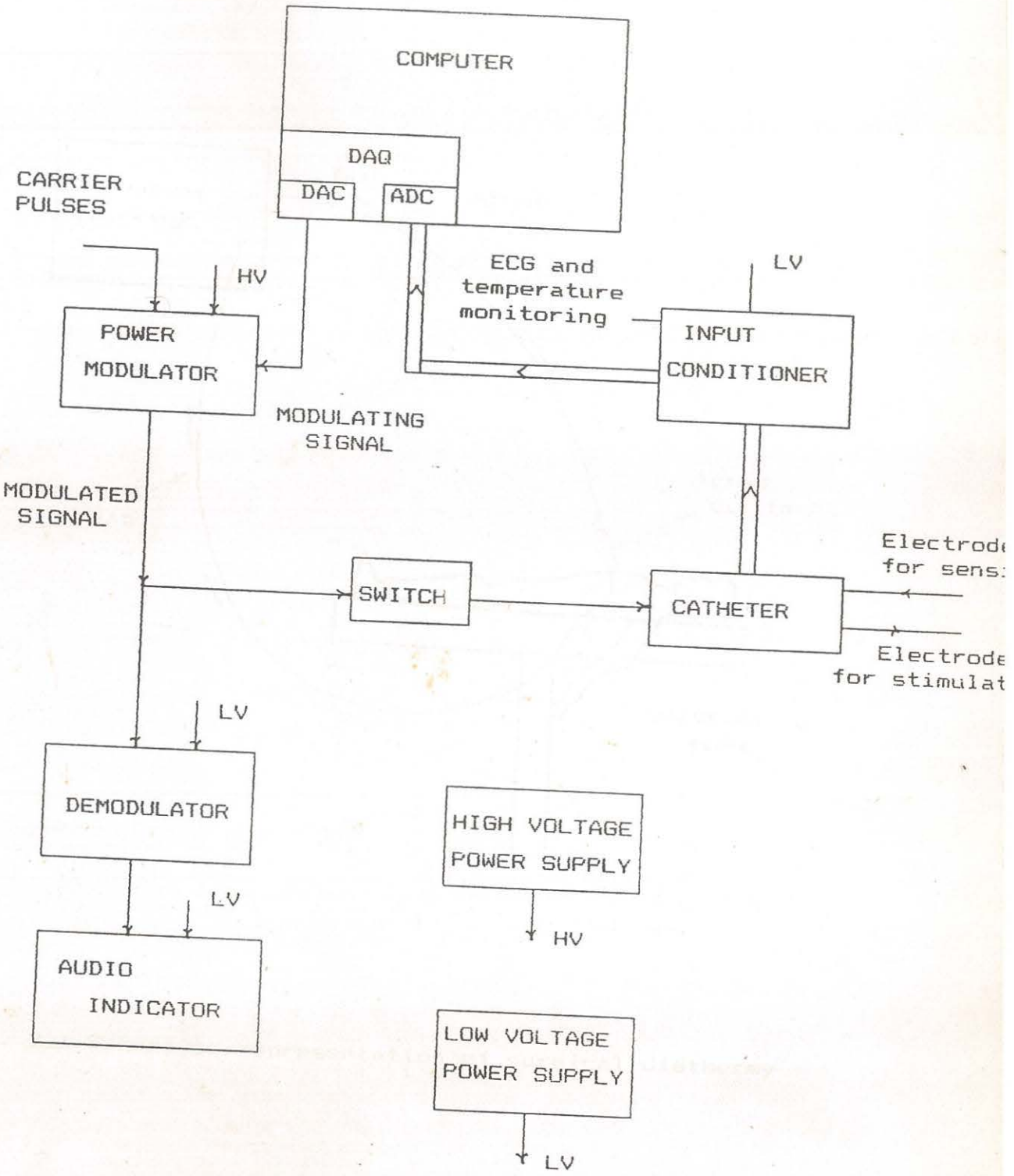


Fig. 1.4. Schematic diagram of proposed system

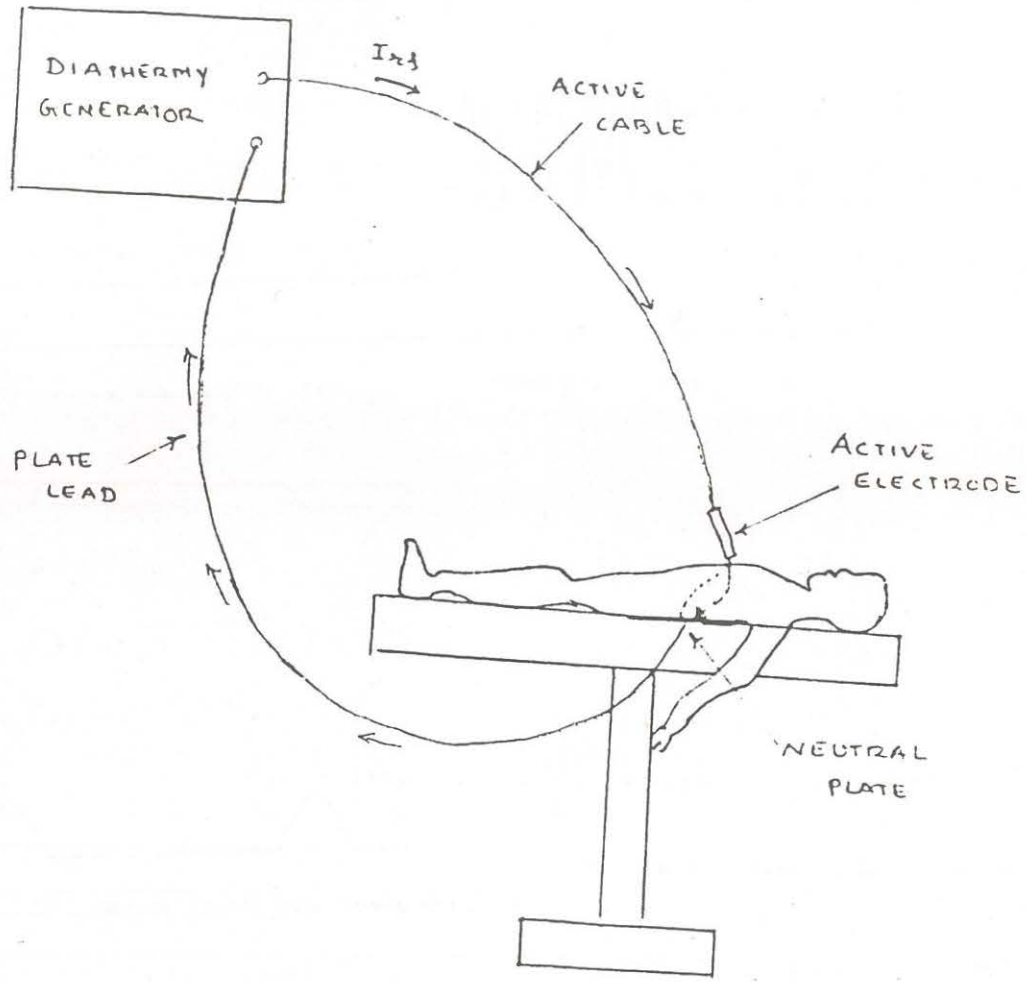


Fig. 2.1 Schematic representation of surgical diathermy

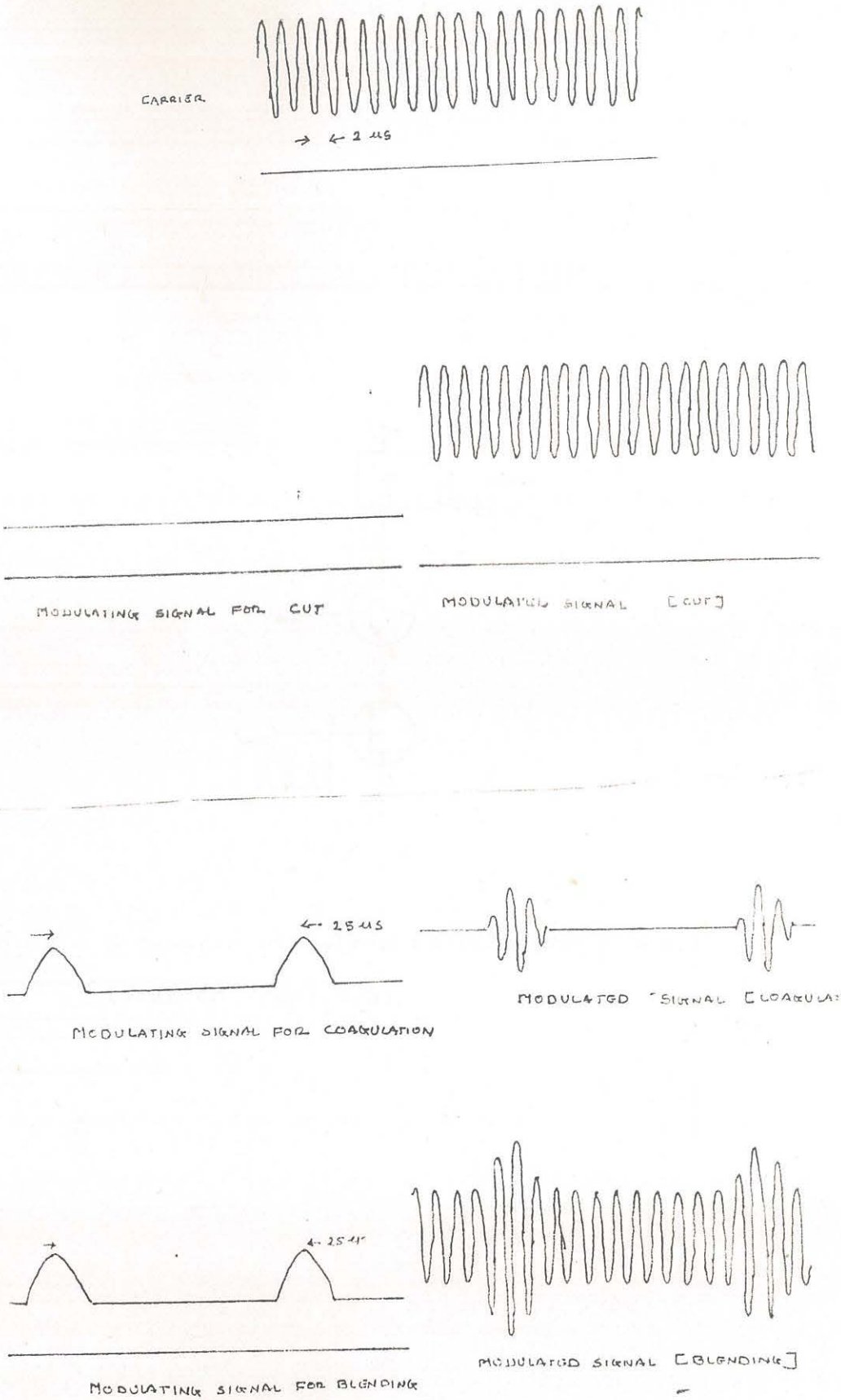


Fig. 2.2 Typical waveforms for cutting, coagulation and blending

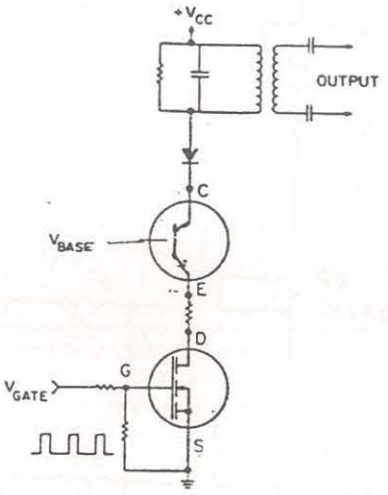


Fig. 2.3 Schematic of hybrid cascode power modulator

(adapted from [12])

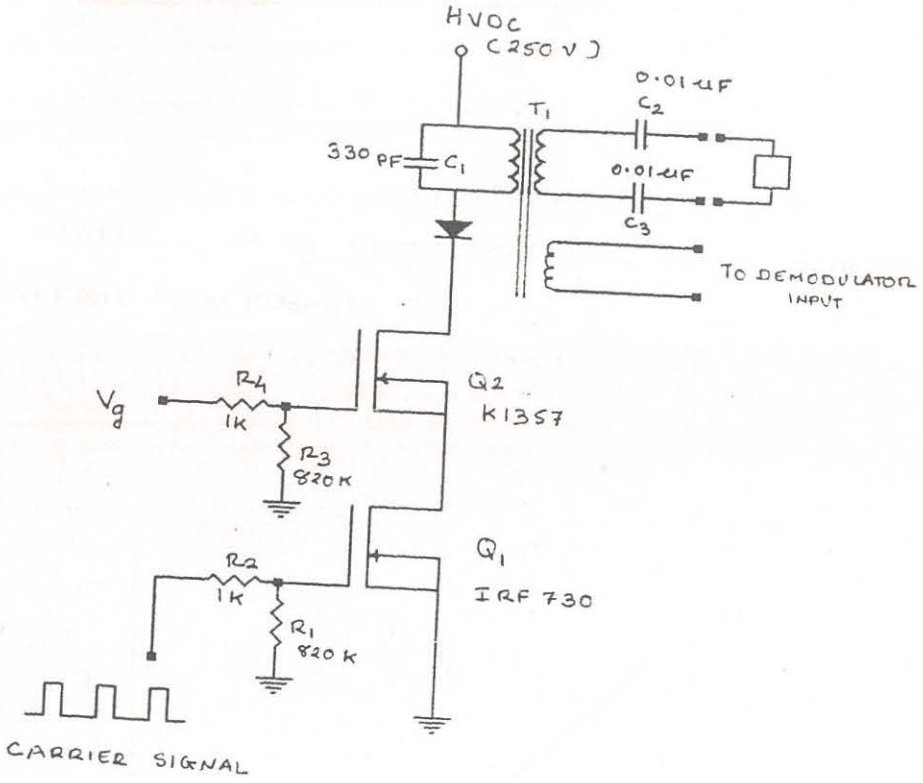


Fig. 2.4 Schematic of power modulator circuit

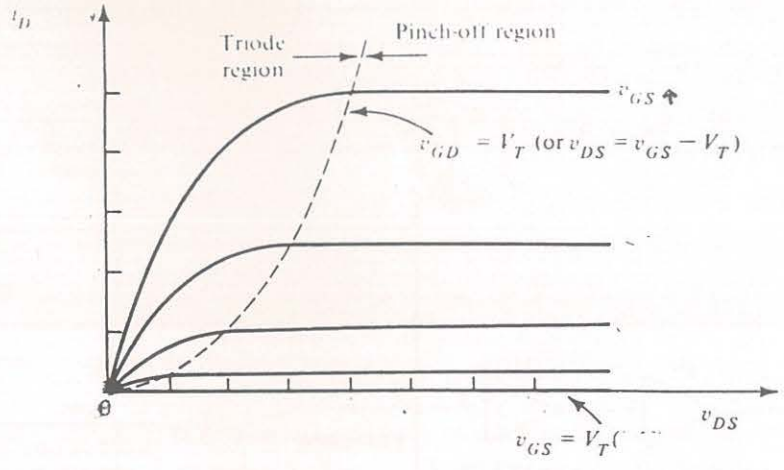


Fig. 2.5 Ideal static I_d vs V_{ds} characteristics for n -channel enhancement type MOSFET

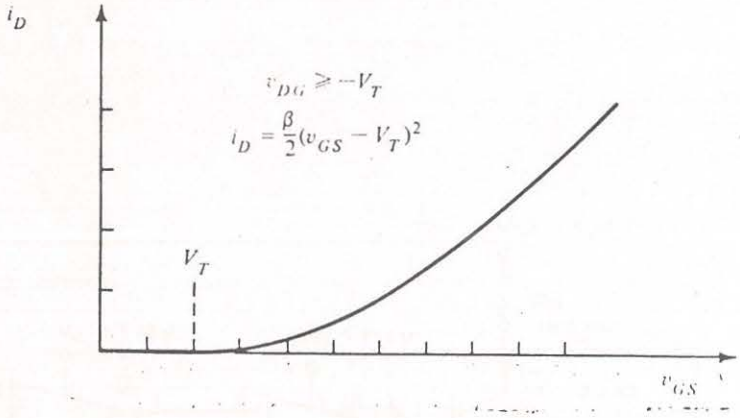


Fig. 2.6 Ideal static I_d vs V_{gs} characteristics for n -channel enhancement type MOSFET

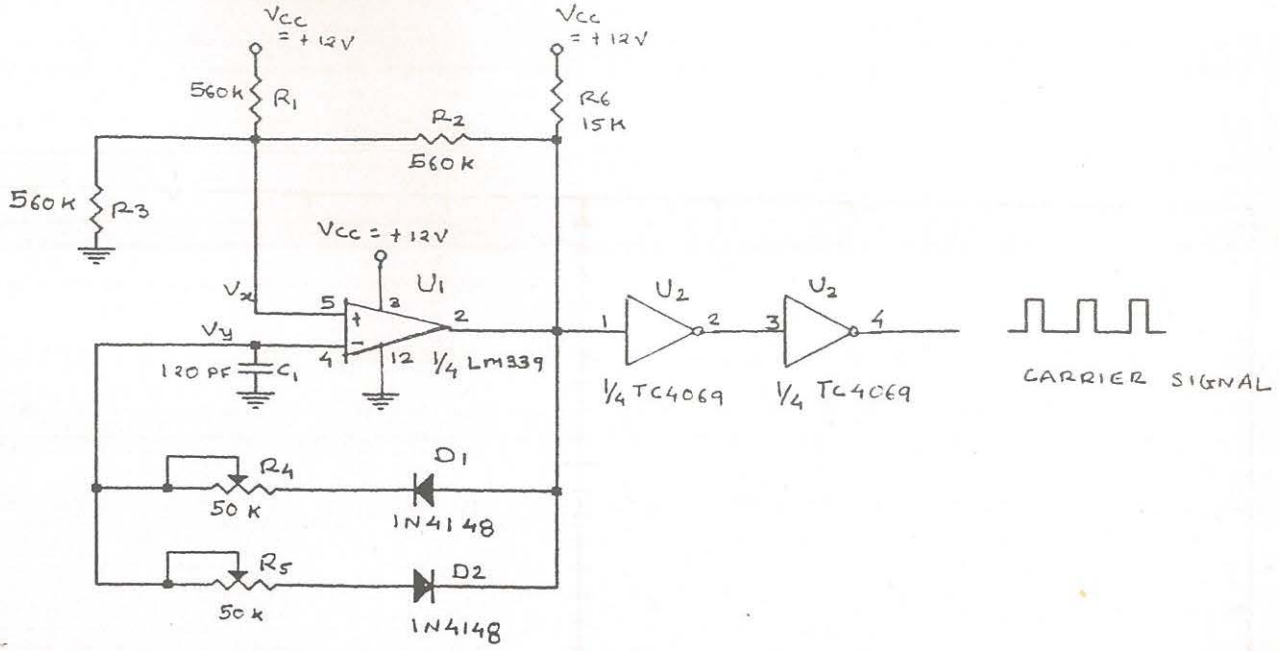


Fig. 2.7 Schematic of carrier signal generator circuit

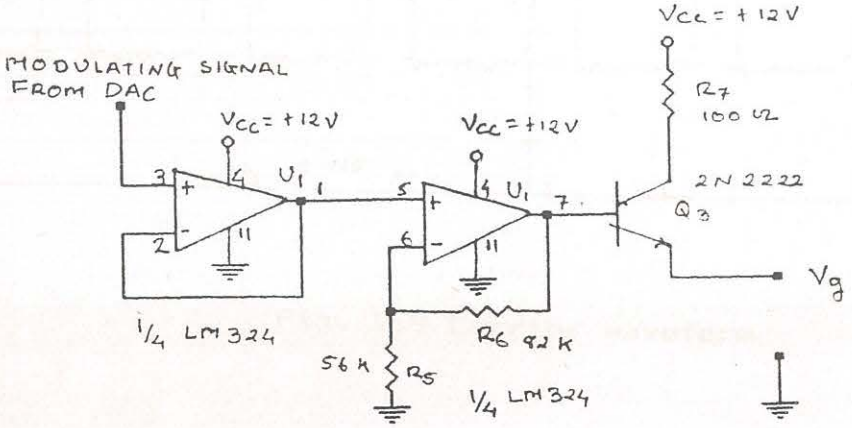


Fig. 2.8 Schematic of gate drive circuit

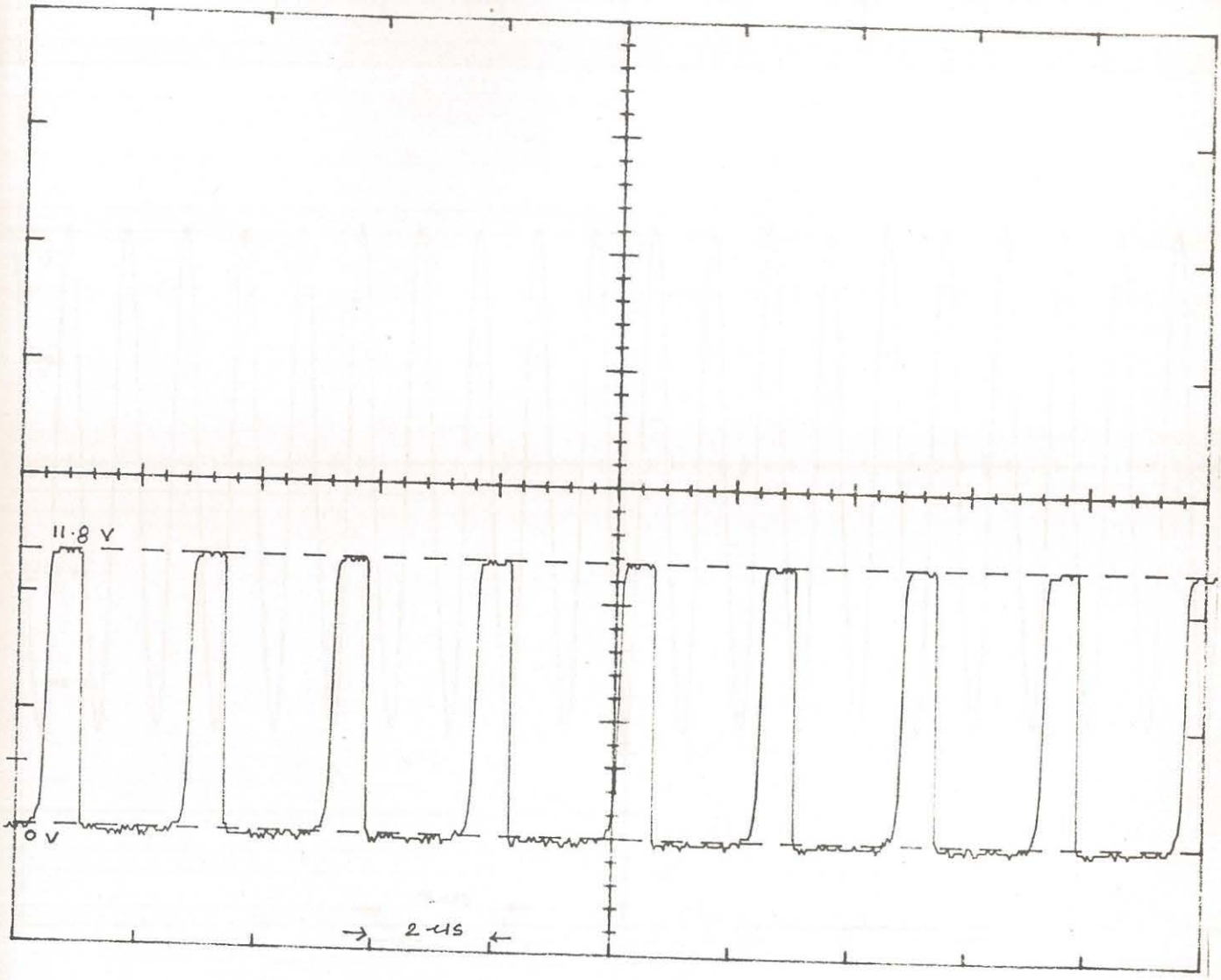


Fig. 2.9 Carrier waveform

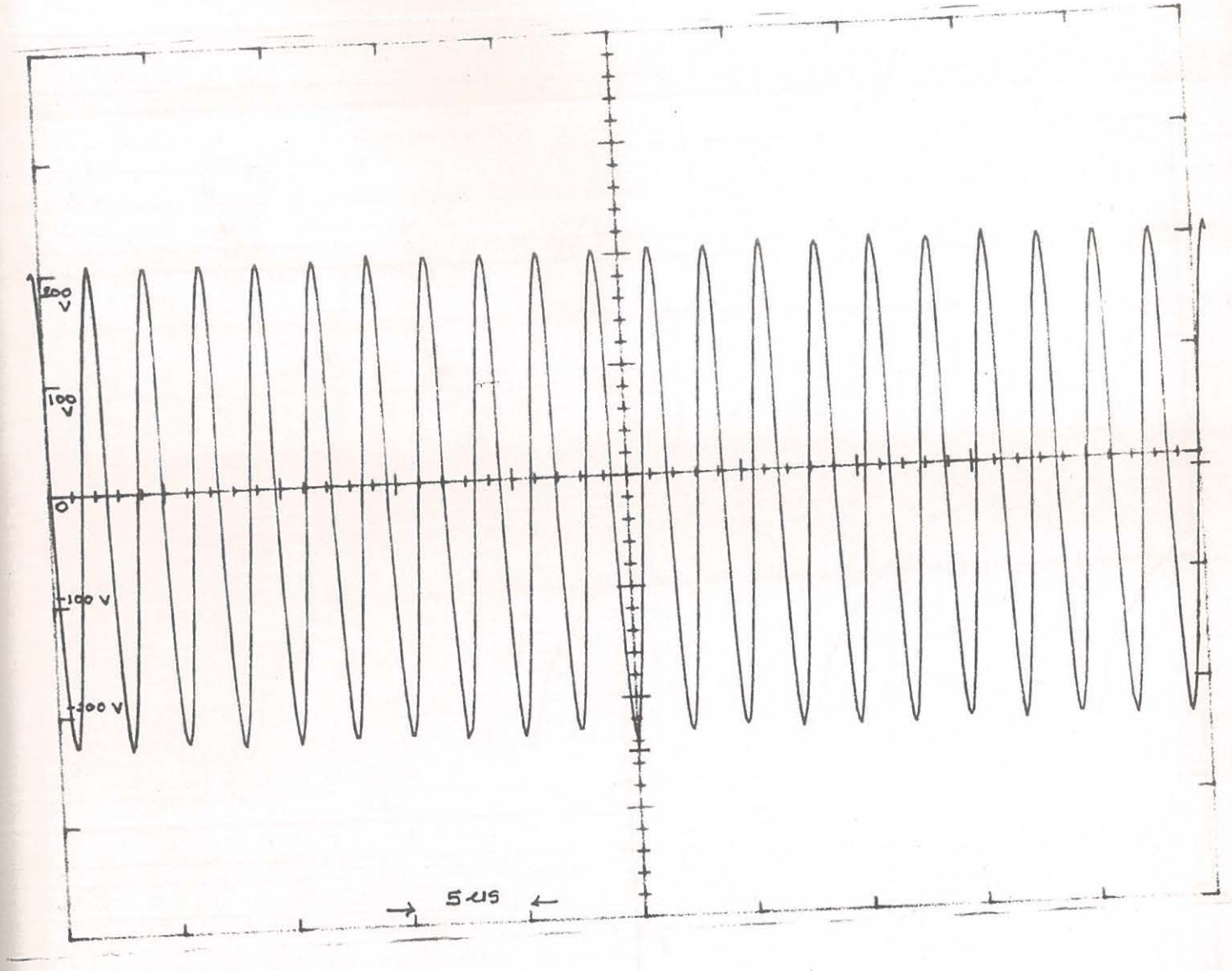


Fig. 2.10 Observed cut waveform without load

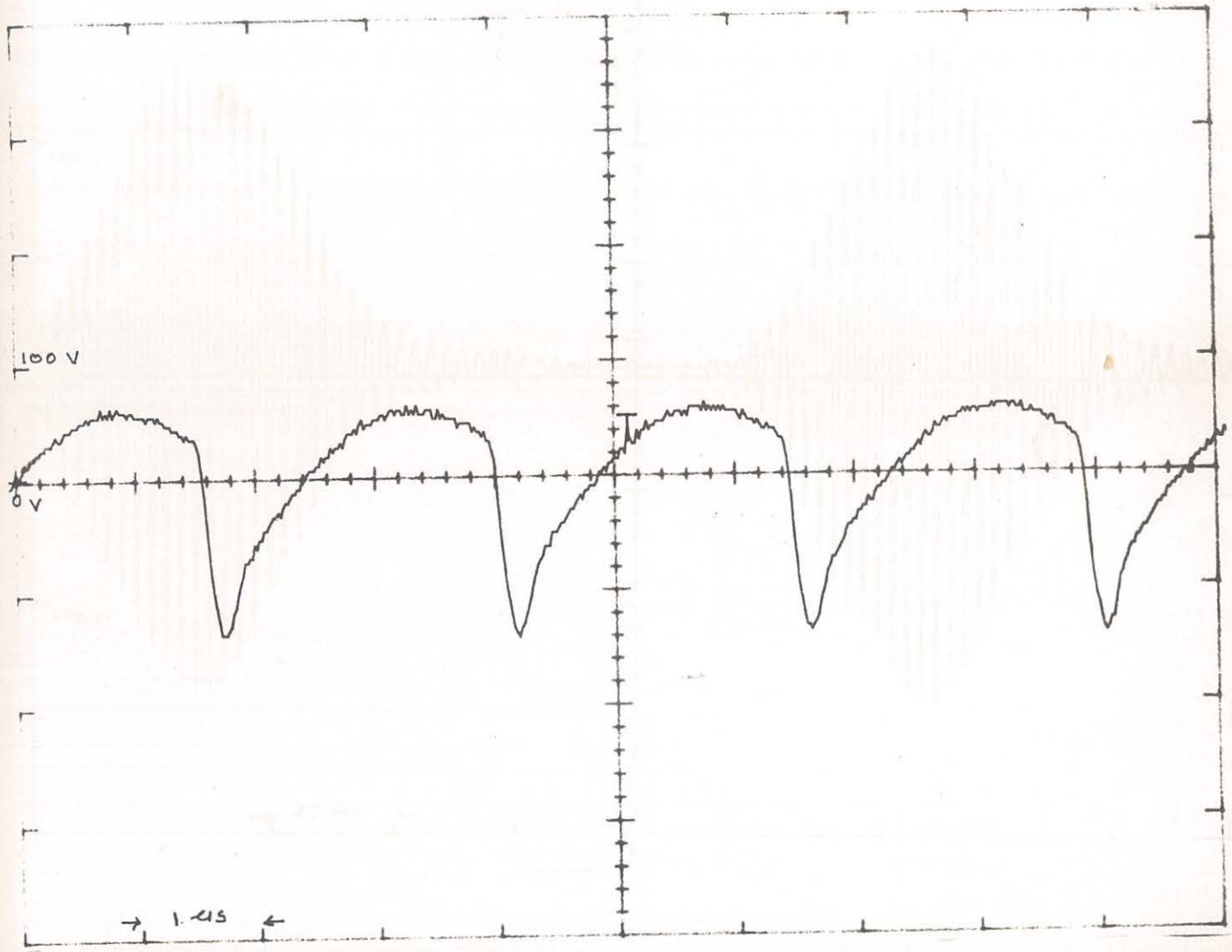


Fig. 2.11 Observed cut waveform with a load
(potato as a load)

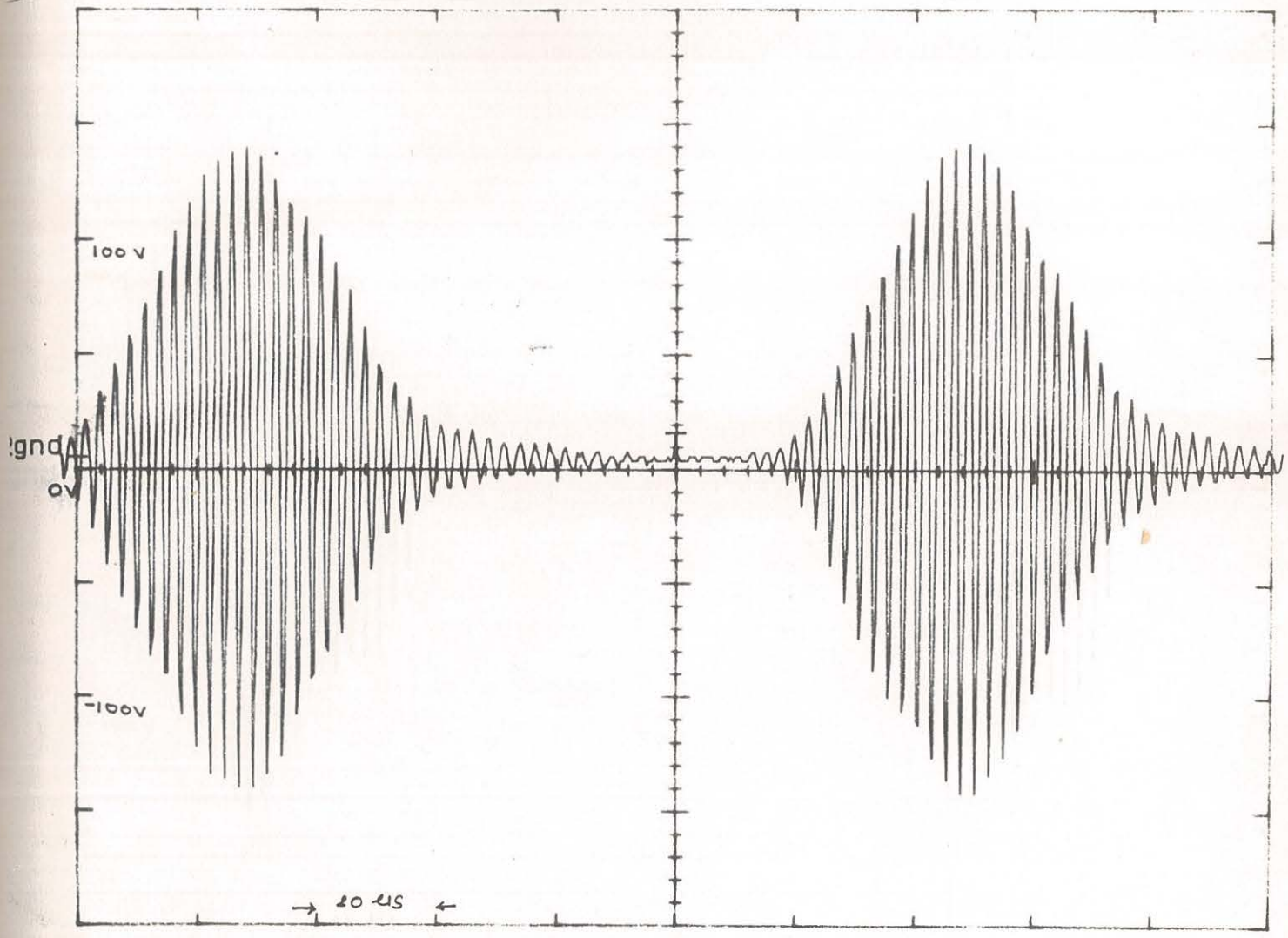


Fig. 2.12 Observed coagulation waveform without load

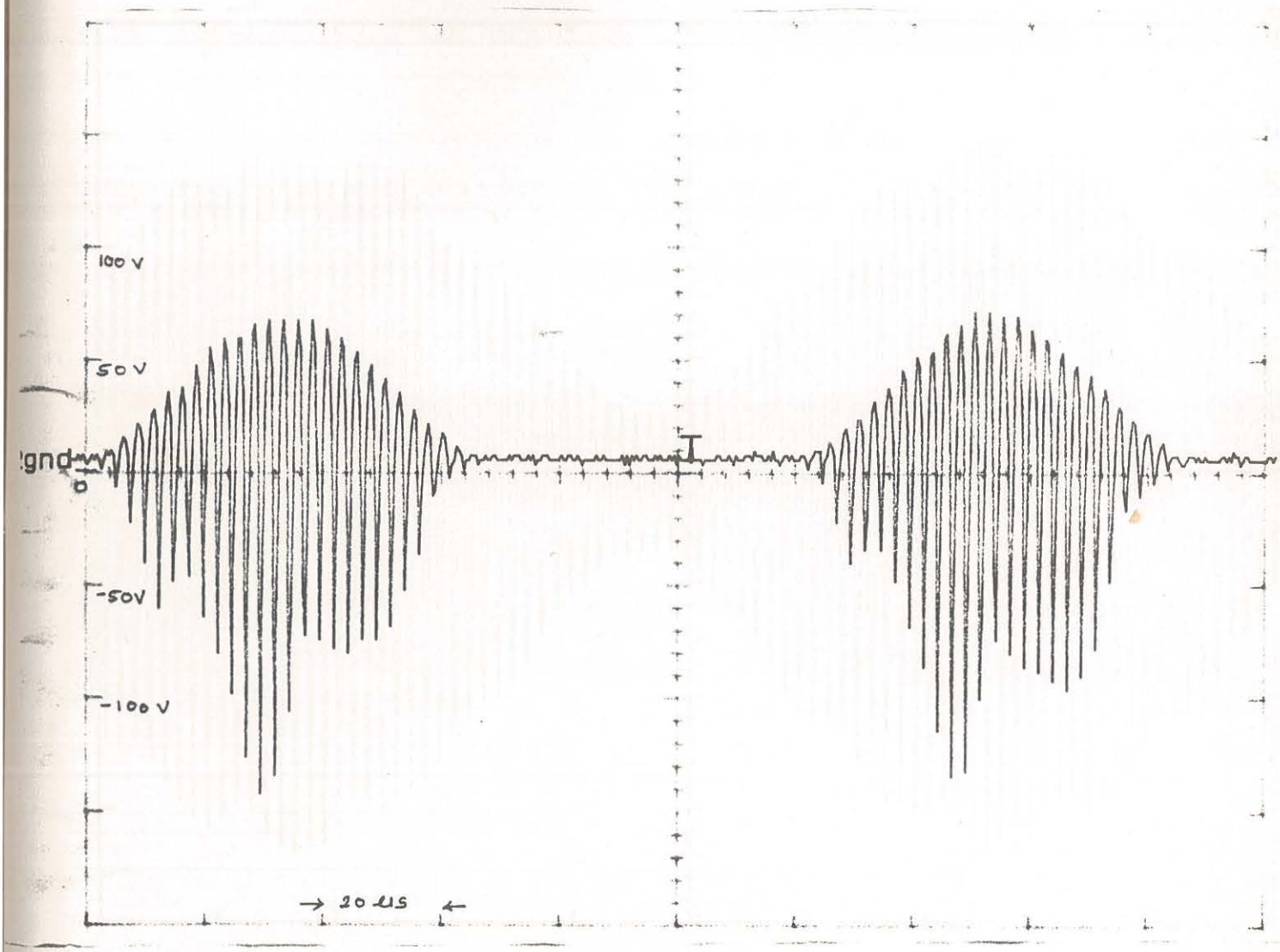


Fig. 2.13 Observed coagulation waveform with a load
(potato as a load)

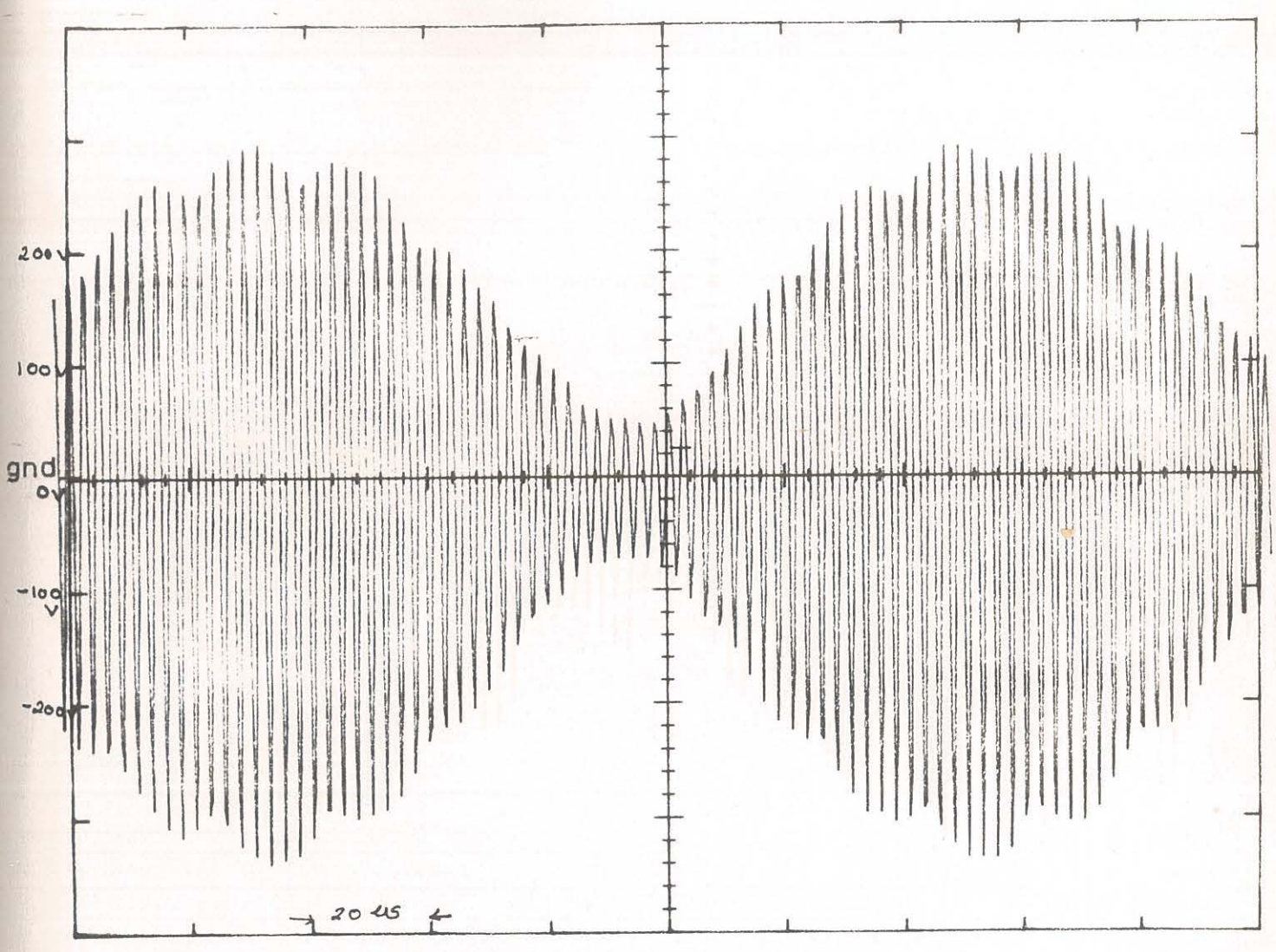


Fig. 2.14 Observed blending waveform without load

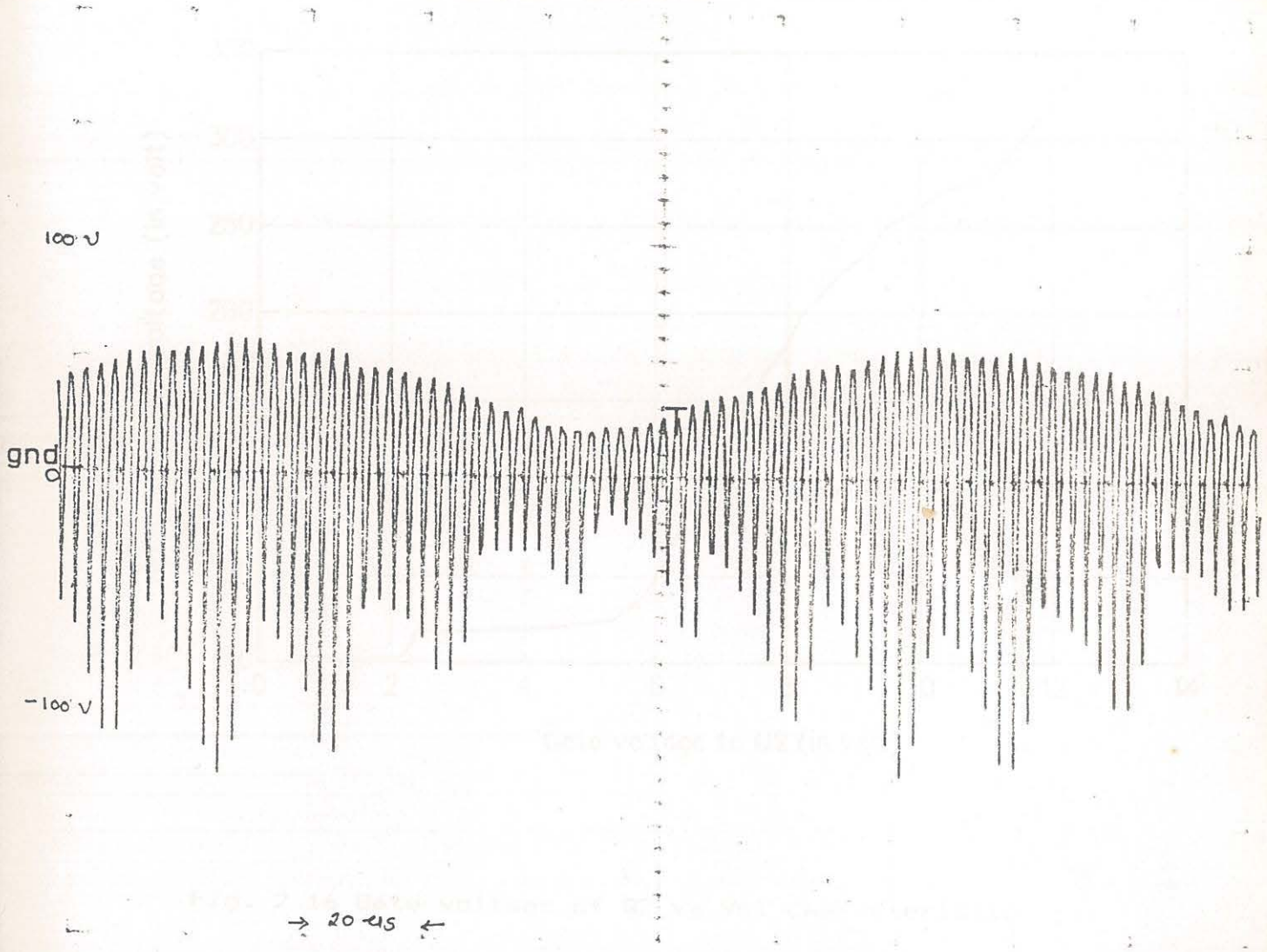


Fig. 2.15 Actual blending waveform with load

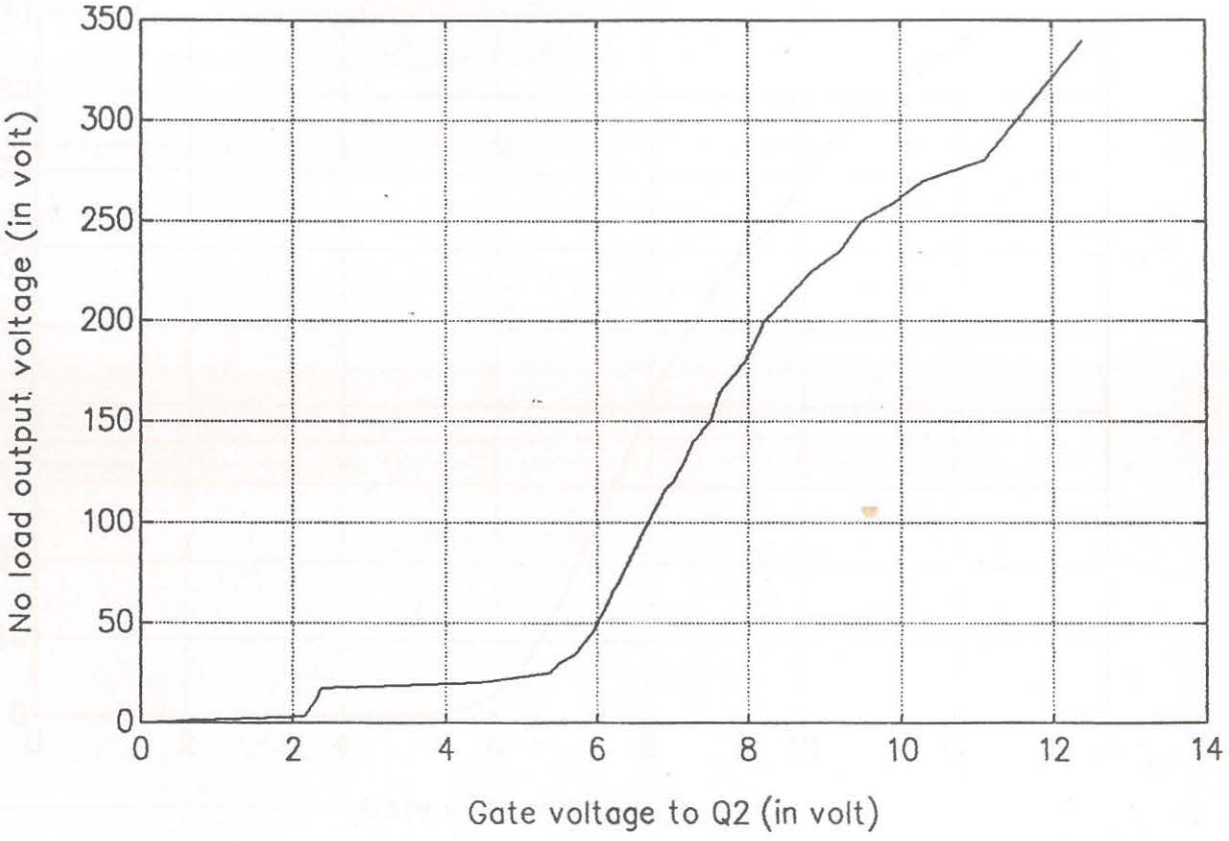


Fig. 2.16 Gate voltage of Q2 vs Vnl characteristic

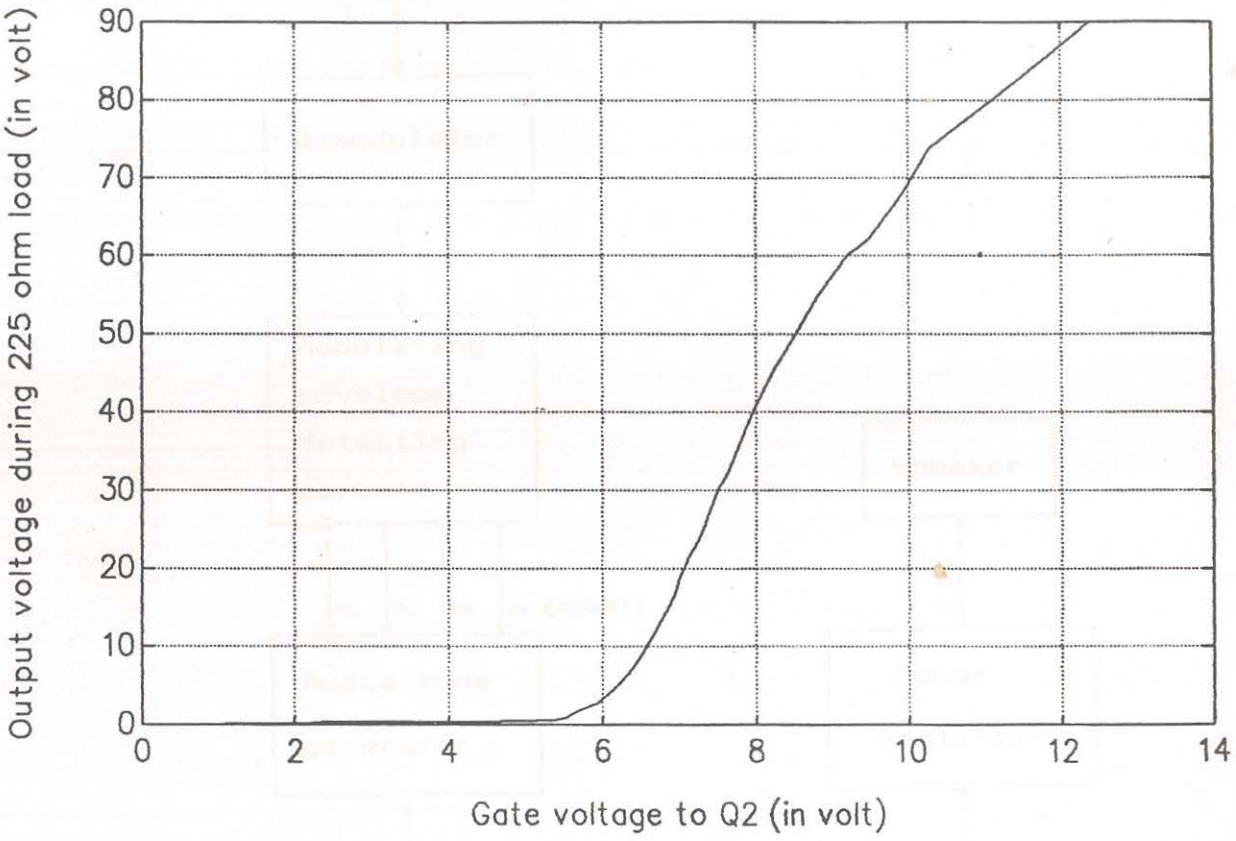


Fig. 2.17 Gate voltage of Q2 Vs Vf1 characteristic

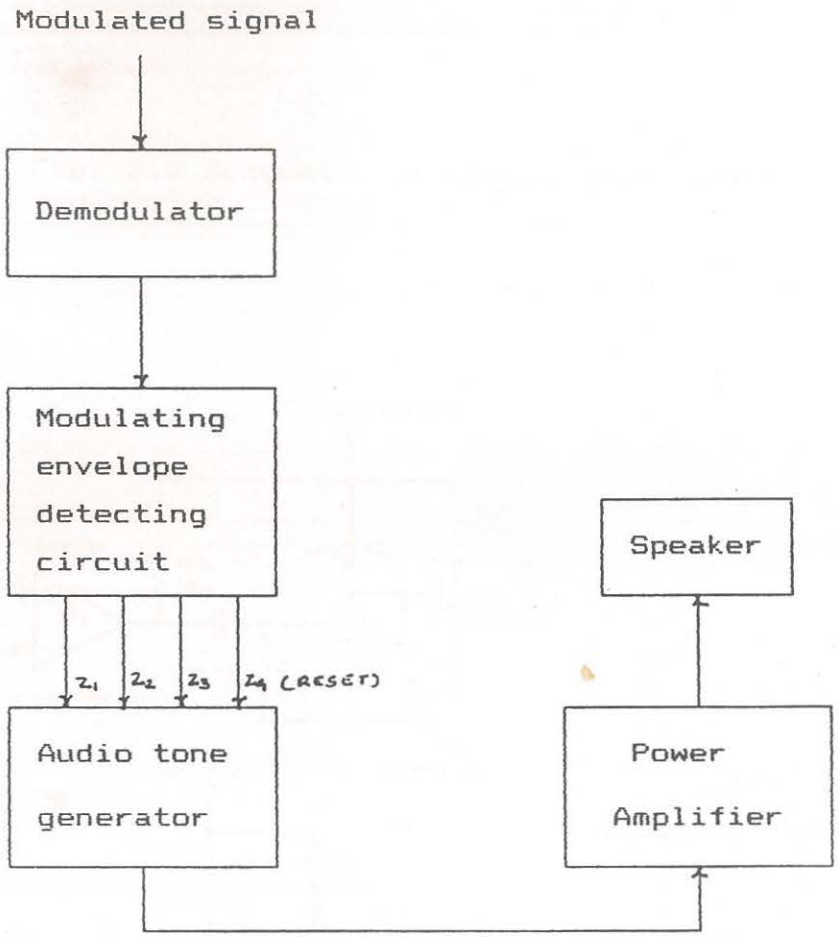


Fig. 3.1 Block diagram of modulator output monitoring

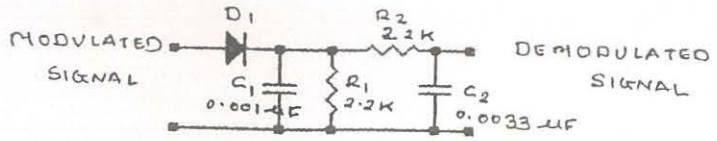


Fig. 3.2 Schematic of demodulator circuit

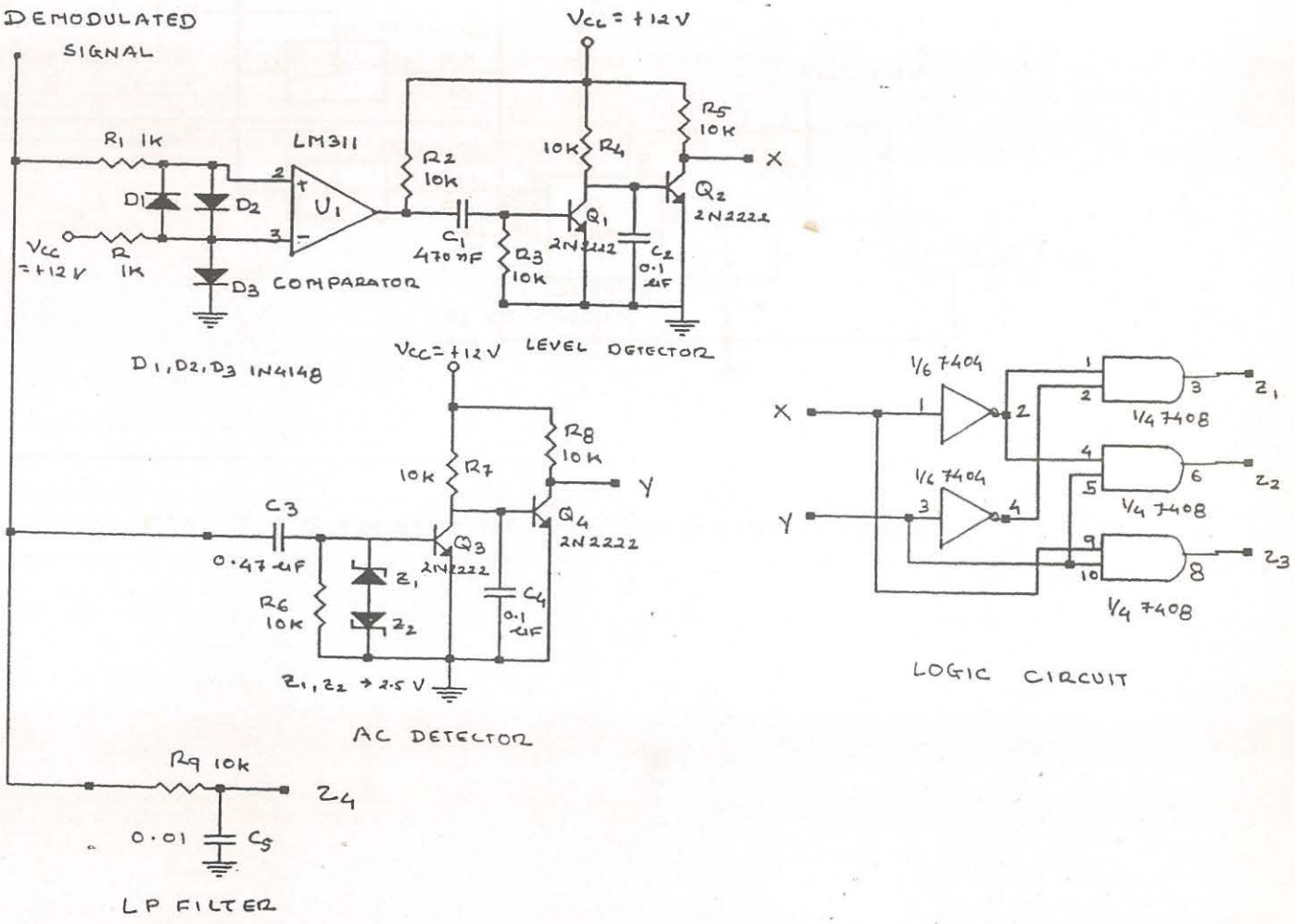


Fig. 3.3 Schematic of envelope classifier circuit

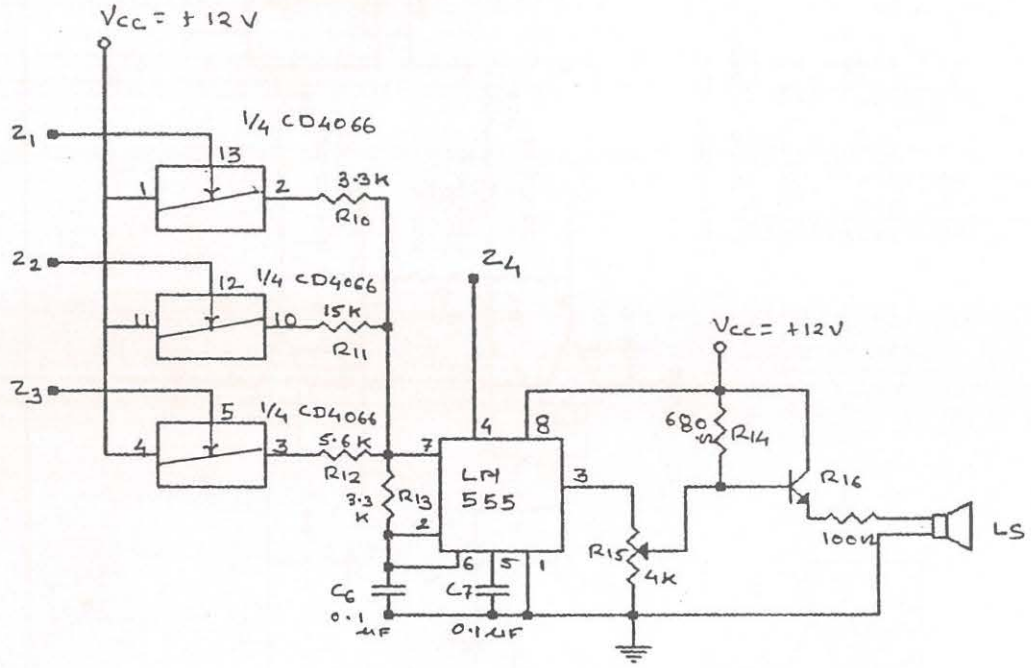


Fig. 3.4 Schematic of tone generator circuit

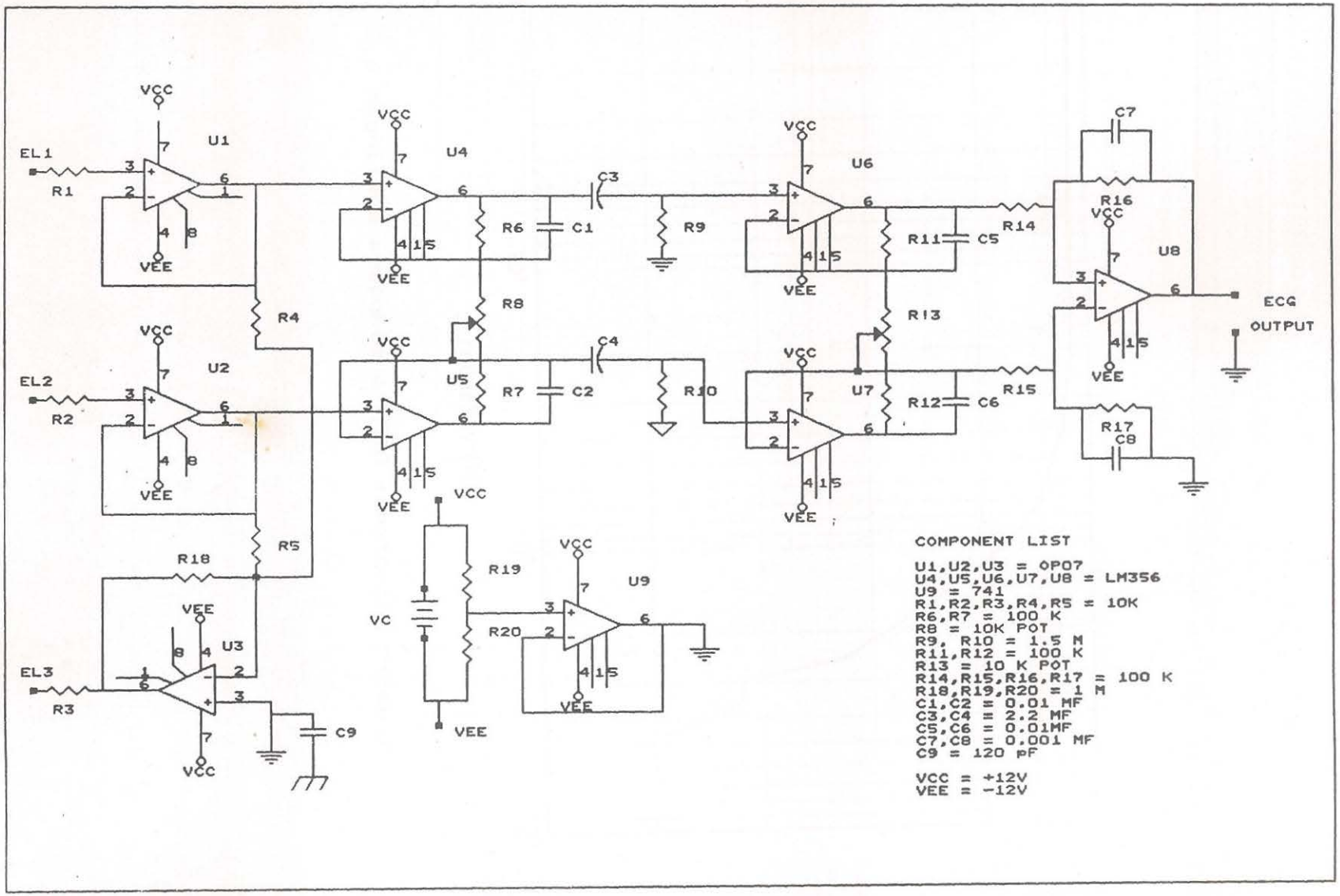


Fig. 3.5 Schematic of ECG monitoring circuit

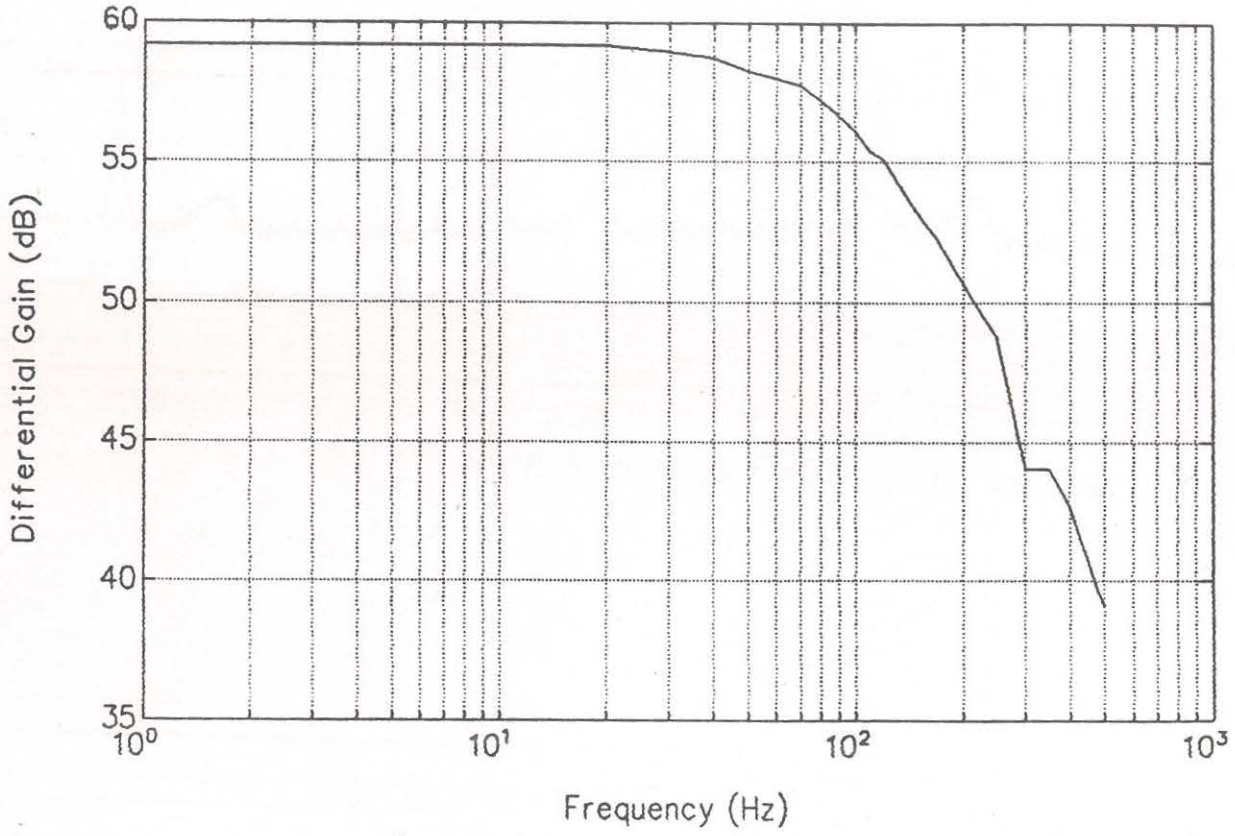


Fig. 3.6 Magnitude response of ECG monitoring circuit

Fig. 3.7 Observed output from ECG monitoring circuit

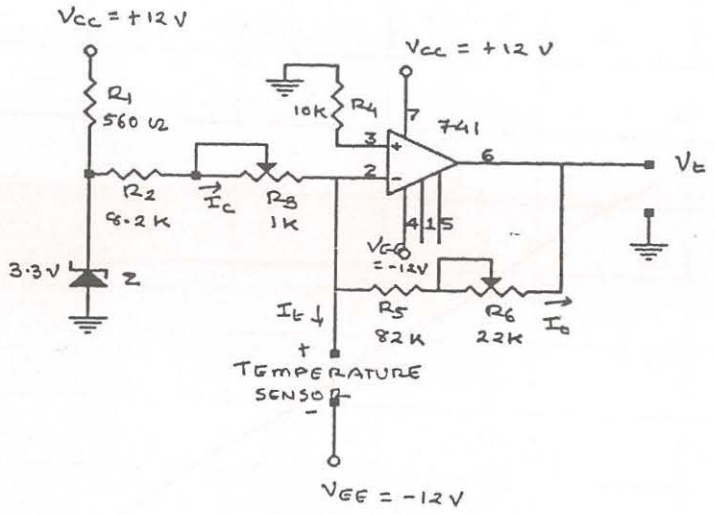


Fig. 3.8 Schematic of temperature monitoring circuit

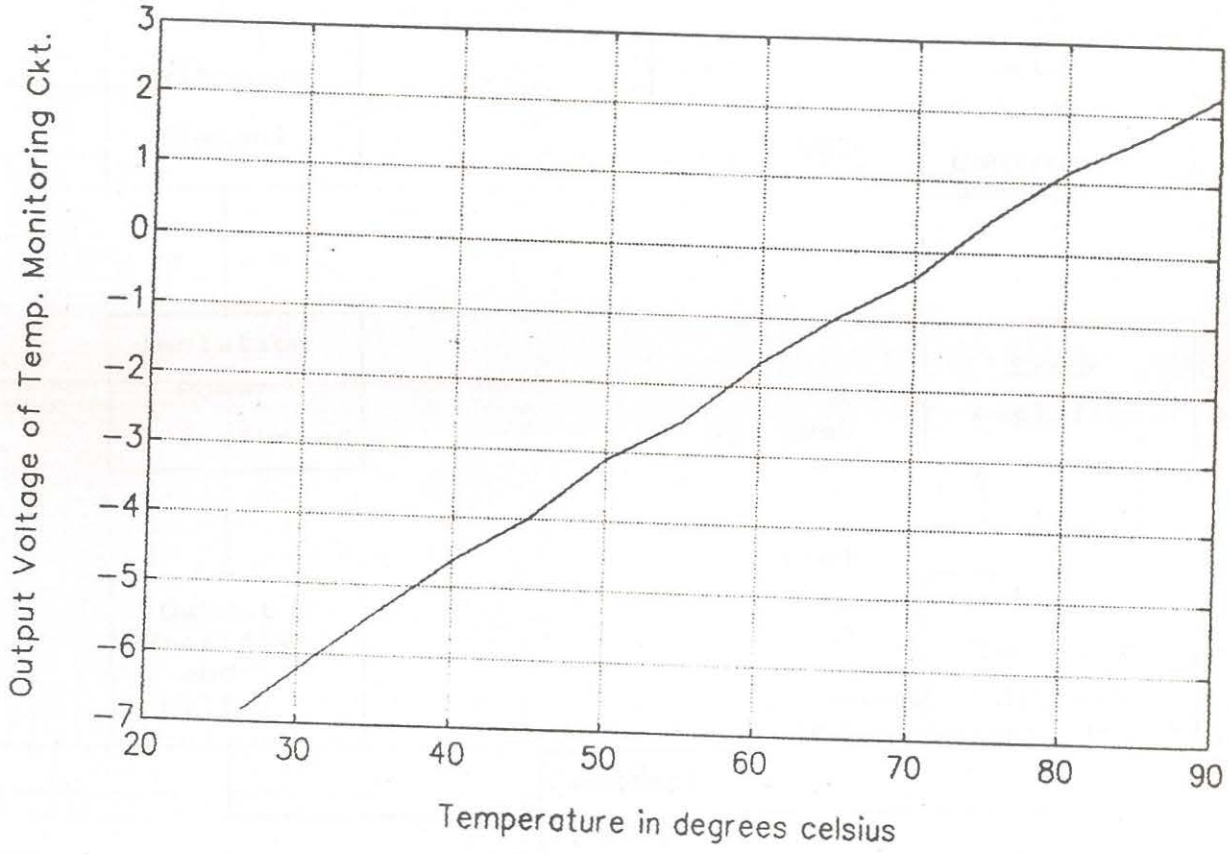


Fig. 3.9 output voltage vs temperature (°C) characteristic for temperature monitoring circuit

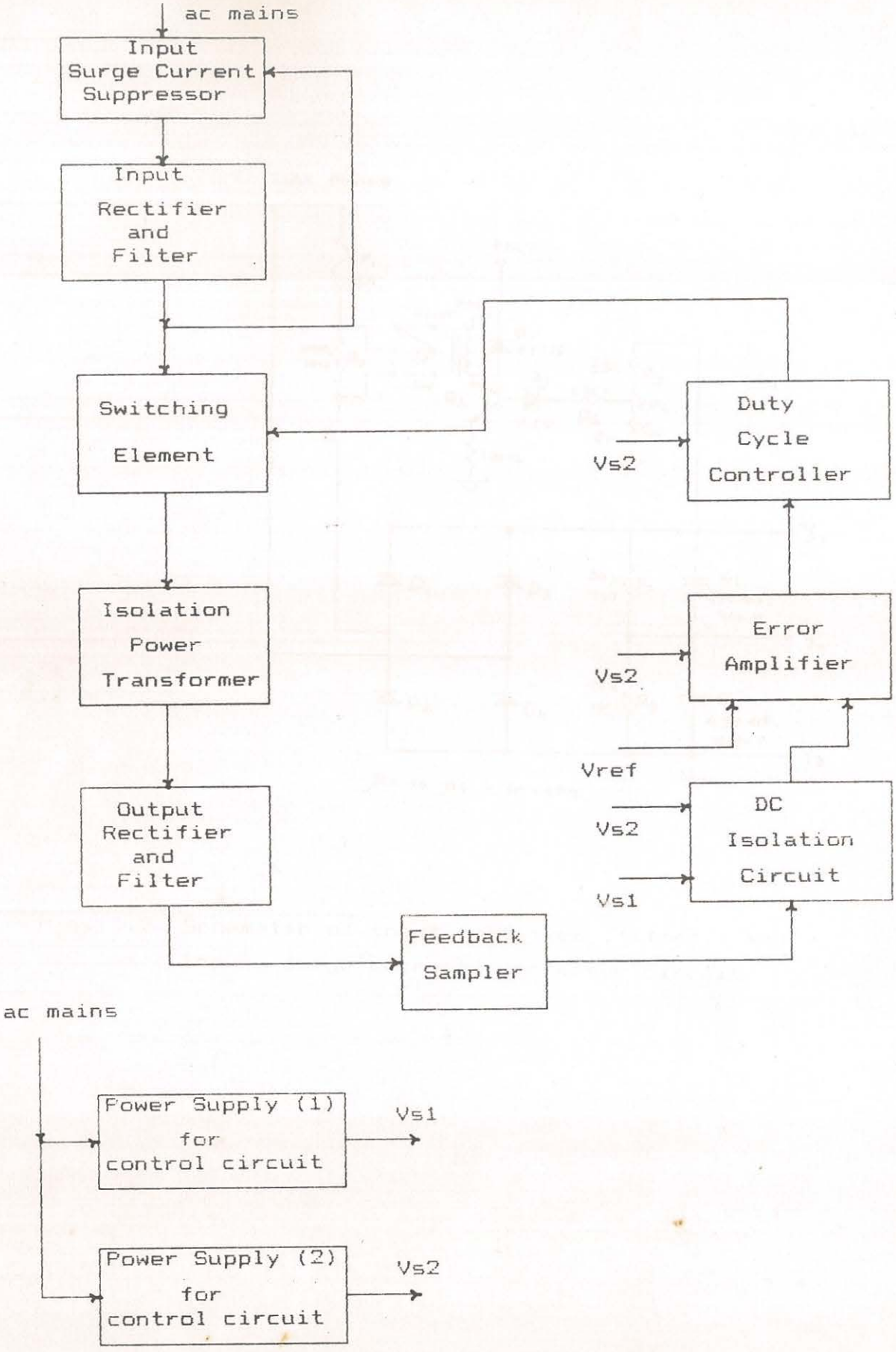


Fig. 5.1 Block diagram of switching mode power supply

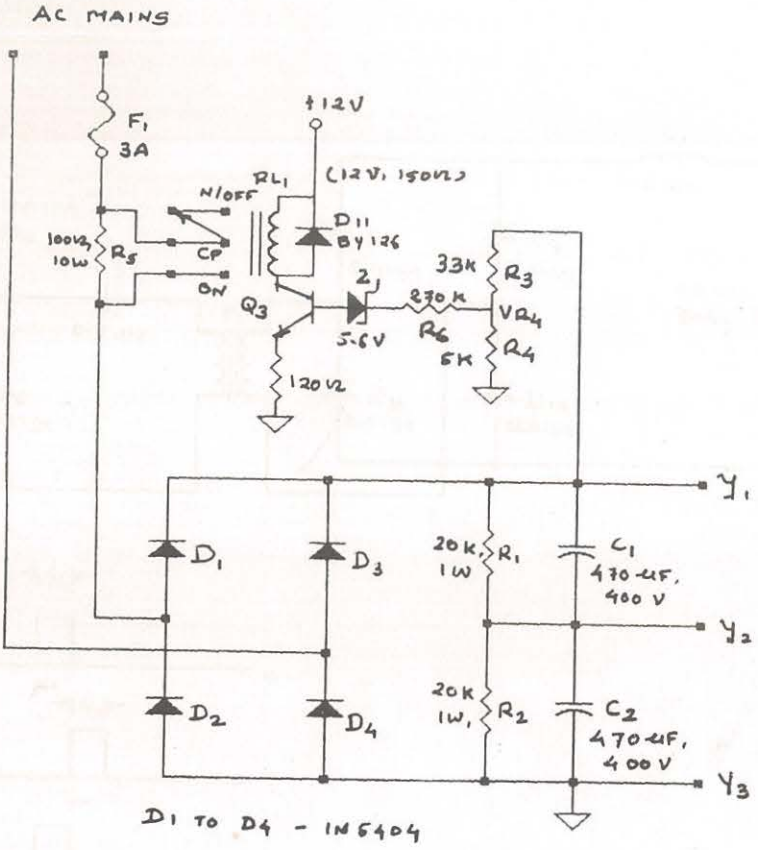


Fig. 5.2 Schematic of input rectifier ,filter, and input surge current suppressor circuit

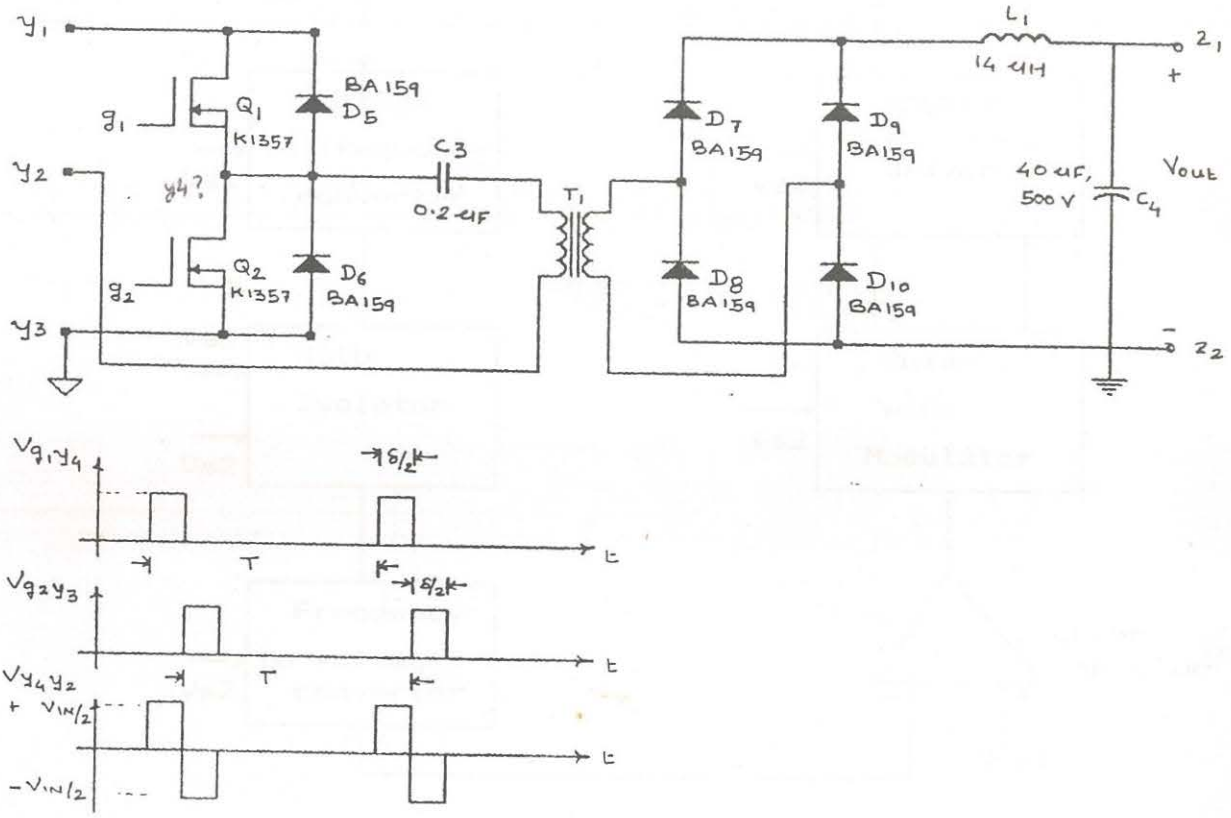
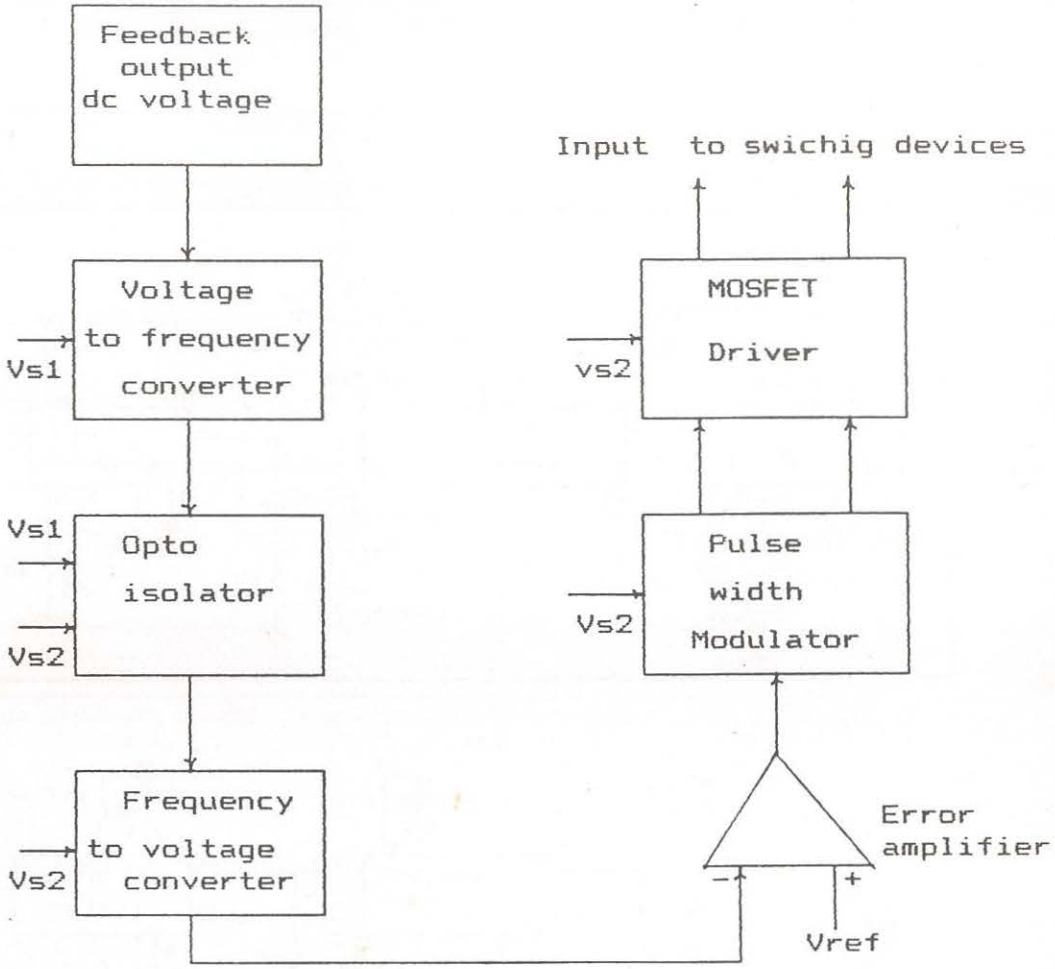


Fig. 5.3 Schematic of half bridge converter circuit. Also shown are the typical waveforms at the transformer primary under ideal condition. T is the switching cycle duration, while $\delta/2$ is the time for which Q1 and Q2 remain on. y_3 is the reference point for the converter and its gate drive circuit (Fig. 5.5)



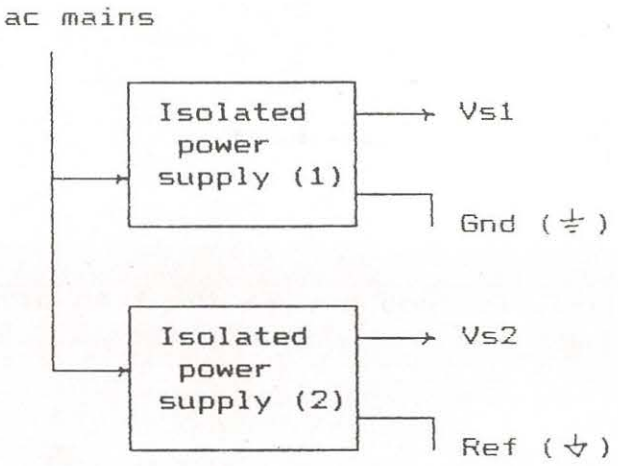


Fig. 5.4 Block diagram of feedback and control circuit

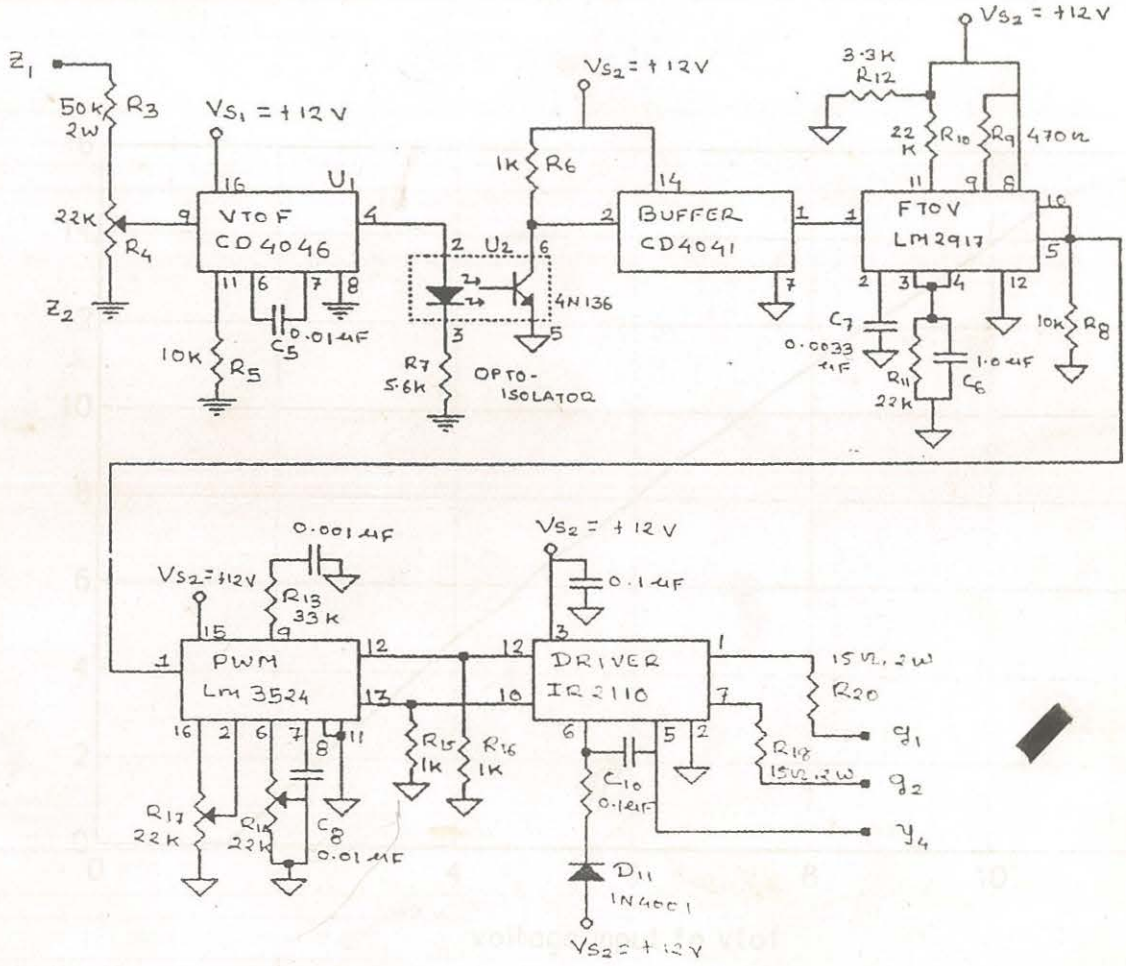


Fig. 5.5 Schematic of feedback and control circuit

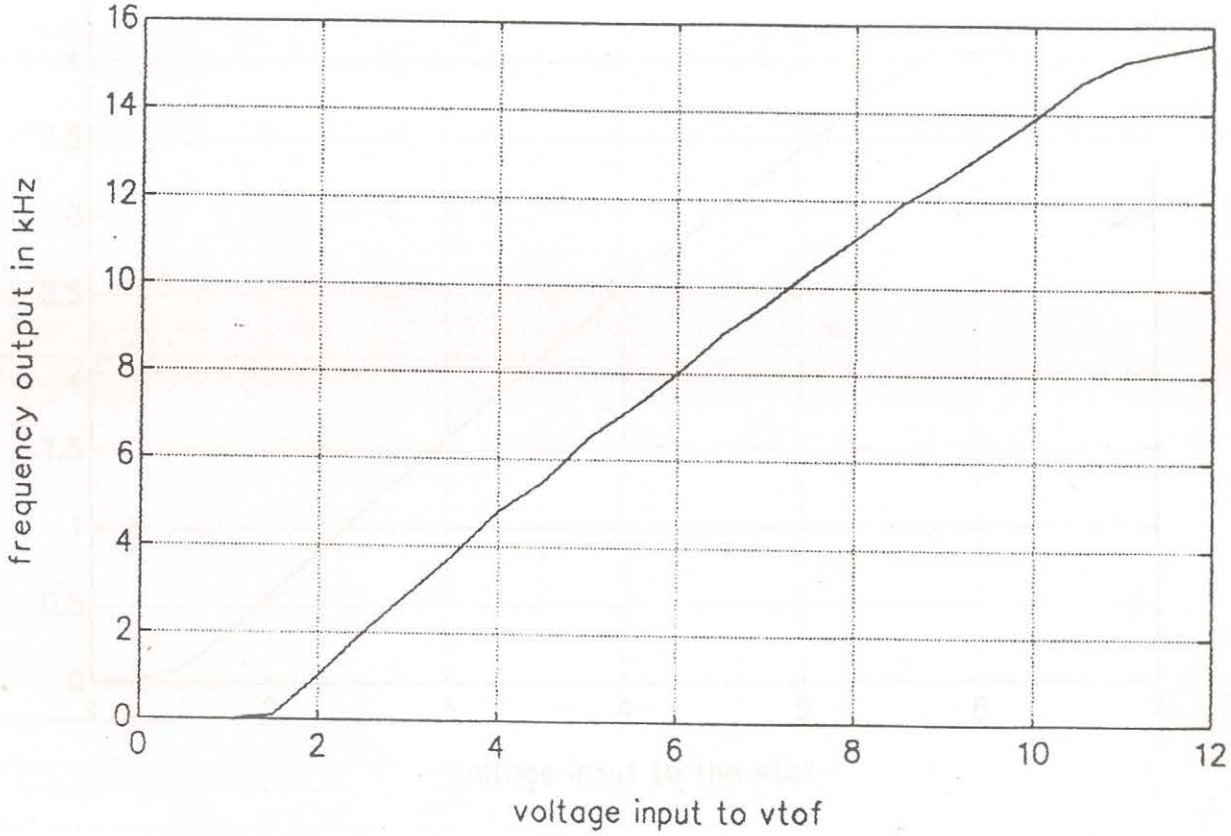


Fig. 5.6 frequency vs voltage characteristic for Voltage-to-frequency converter

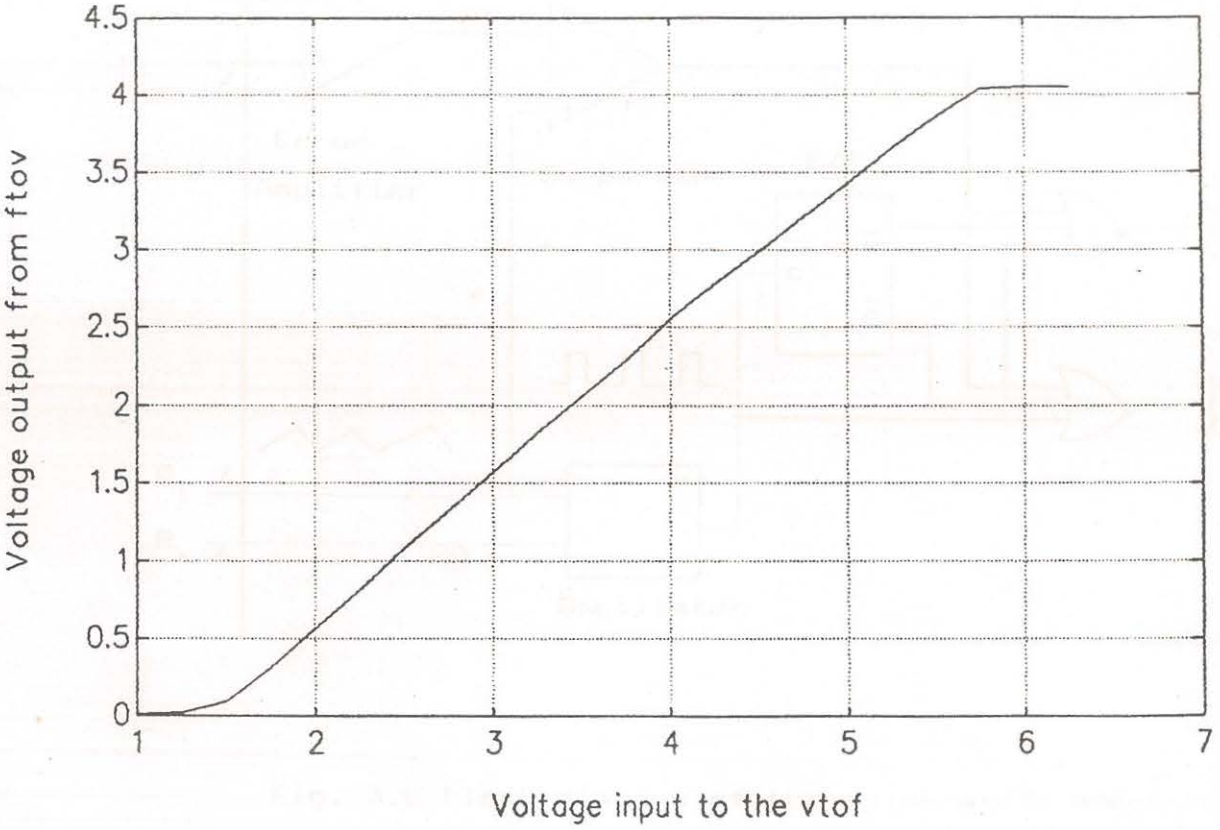


Fig. 5.7 Output voltage of ftov vs input voltage to vtof characteristic

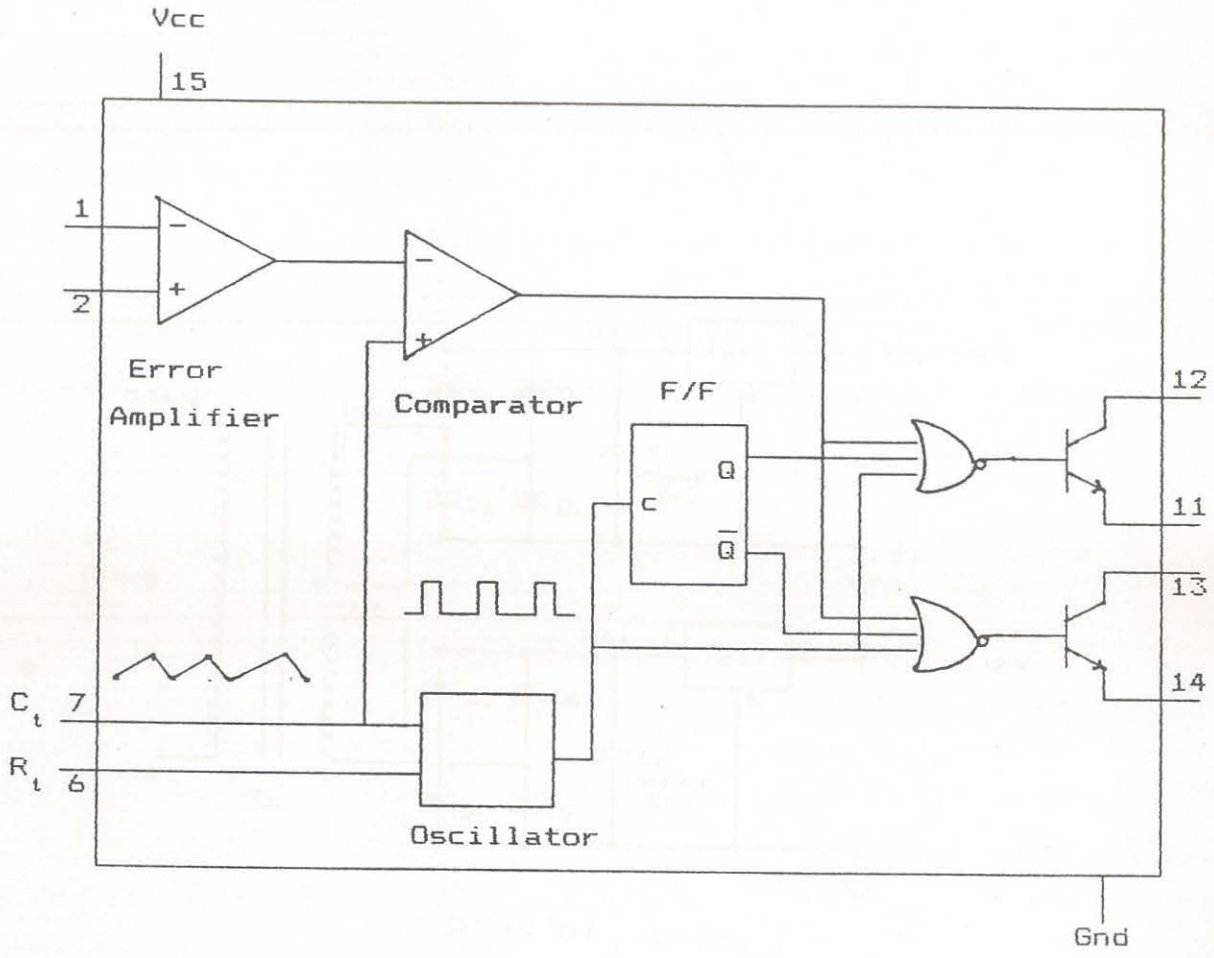


Fig. 5.8 Block diagram of the pulse width modulator

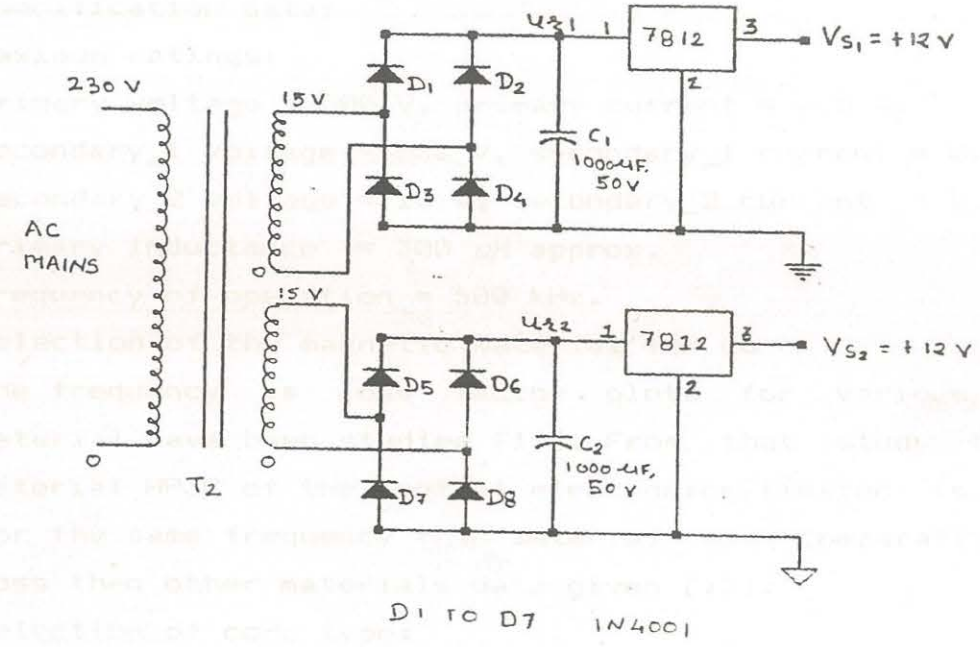


Fig. 5.9 Schematic of power supply circuit for feedback and control circuit

APPENDIX A

HIGH FREQUENCY TRANSFORMER

The step by step design procedure for designing a high frequency transformer is given in the reference [28]. In our application this transformer is used in the tank circuit of the power modulator. The design procedure with our specification is given below:

1. Specification data:

   Maximum ratings:

   Primary voltage = 500 V, primary current = 0.5 A.

   Secondary_1 voltage = 500 V, secondary_1 current = 0.5 A.

   Secondary_2 voltage = 25 V, secondary_2 current = 0.1 A.

   Primary inductance = 300 μH approx.

   Frequency of operation = 500 kHz.

2. Selection of the magnetic material for core:

   The frequency vs loss factor plots for various magnetic material have been studied [15]. From that study the ferrite material HP3C of the Central electronics limited is selected. For the same frequency this material has comparatively lower loss then other materials data given [15].

3. Selection of core type:

   From relative study of different core construction [15] the pot core 30/19 is selected. The magnetic characteristics of this core is given below.

   Core factor : l_e/A_e = 0.33 mm^{-1}

   Effective length : l_e = 45 mm

   Effective Area : A_e = 136 mm^2

   Effective Volume : V_e = 6120 mm^3

   Appx. weight : = 36 gms/set

   AL value : = 1250 ($\pm$ 25 %)

   μi : = 2300

   Curie temperature : $\geq$ 130 $^{\circ}$C

Flux density : B = 3900 mT

4. Number of turns

AL value = L / N^2 Where L is the inductance in neno Henry and N is the number of turns. For primary the inductance specified is 300 μH approximately. Taking this figure into account for give AL value N is coming out to be 16 turns. With taking $\pm$25 % tolerance of AL into account the namer of turn selected for primary is = 20 turns. Also care has taken such that max flux density can rise half of the maximum specified, to avoid saturation effect of core material. The maximum flux density is given as

$$B_{max} = \frac{E_{rms} * 10^8}{4.44\ N\ Ae\ f}$$ A_e in square cm, f in hertz, E_{rms} in volts.

For our case N = 20, Ae = 136 mm^2, f = 500 kHz, E_{rms}=500 V. With these data B_{max}= 828 gauss = 82.8 mT. It is less then maximum flux density specified.

$$\text{Secondary turns} = \frac{\text{primary turns} * \text{secondary voltage}}{\text{primary voltage}}$$

From this equation the secondary_1 turns are selected equal to 20 and secondary_2 turns are selected equal to 1.

5. Insulation used: due to high primary and secondary voltages for good isolation mylar material is used between primary and secondary winding.

An another high frequency transformer is also used in

he

switching mode power supply. Which has EE -type (E-42 X 21 X 9) ferrite core of HP_3C material.The magnetic characteristics of it, is given below:

Core factor	l_e/A_e	= 1.01 mm^{-1}
Effective Length	l_e	= 108.6 mm
Effective Area	Ae	= 107.5 mm^2
Effective Volume	V_e	= 11674.5 mm^3

Approximate Weight	= 51 gms/set
AL value	= 2613 ($\pm$ 25 %)
μi	= 2300
Curie temperature	$\geq$ 130 ^{o}C
Flux density	= 3900 mT

APPENDIX B

SPECIFICATIONS FOR DATA ACQUISITION CARD PCL- 208.

Analog Input (A/D Converter)

Channels : 16 single-ended or 8 differential.
Resolution : 12 Bits.
Input range : Unipolar : +10V, +5V, +2V, +1V.
Bipolar : +/-10V, +/-5V, +/-2.5V, +/-1V, +/-0.5V
Conversion type : Successive approximation.
Conversion speed: 60 kHz.
Accuracy : +/-(0.001% of reading) +/- 1 bit.
Linearity : +/- 1 bit.

Analog Output (D/A Converter)

Channels : 2 channels.
Resolution : 12 Bits.
Output Range : 0 t0 +5V with on-board -5V reference.
Conversion type : 12 bit monolithic multiplying.
Linearity : +/- 1/2 bit.
output drive : +/-5mA max.
Settling time : 5 microseconds.

Programmable Timer/Counter

Device : INTEL 8254.
Counters : 3 channels, 16 Bit. 2 Channels permanently configured as programmable pacer.
Time base : Pacer (channel 1 and 2); 10 MHz or 1 MHz.
Pacer Output : 0.00023 Hz to 2.5 MHz.

Interrupt Channel

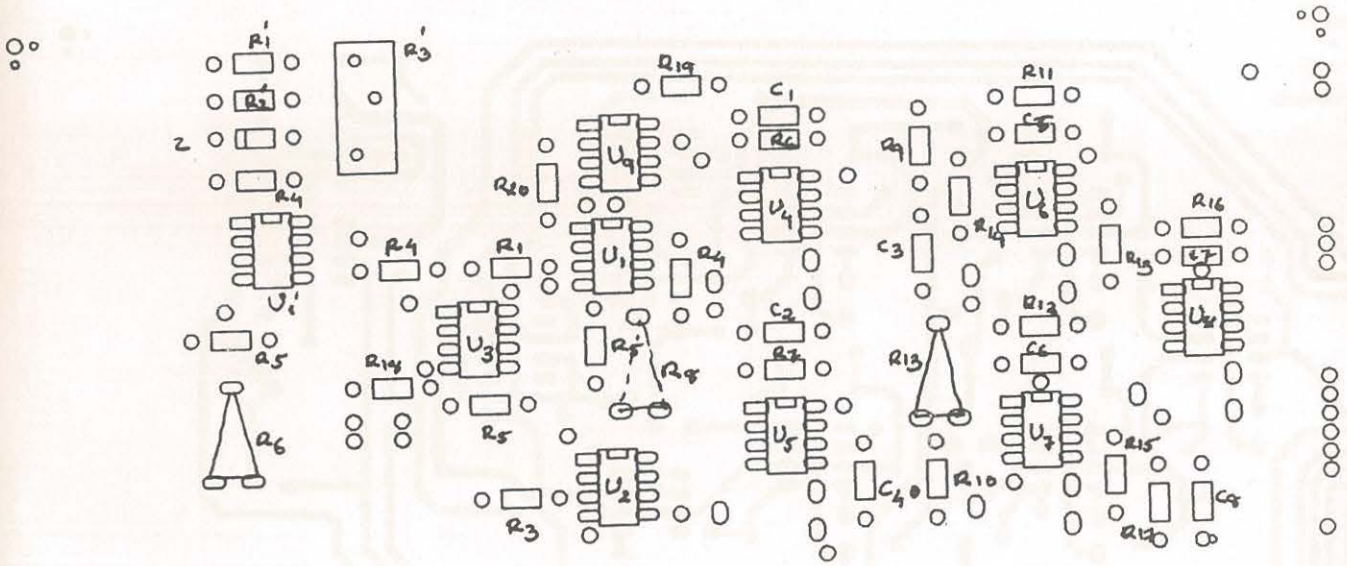
Level : IRQ 2 to 7.

APPENDIX C

PCB LAYOUTS

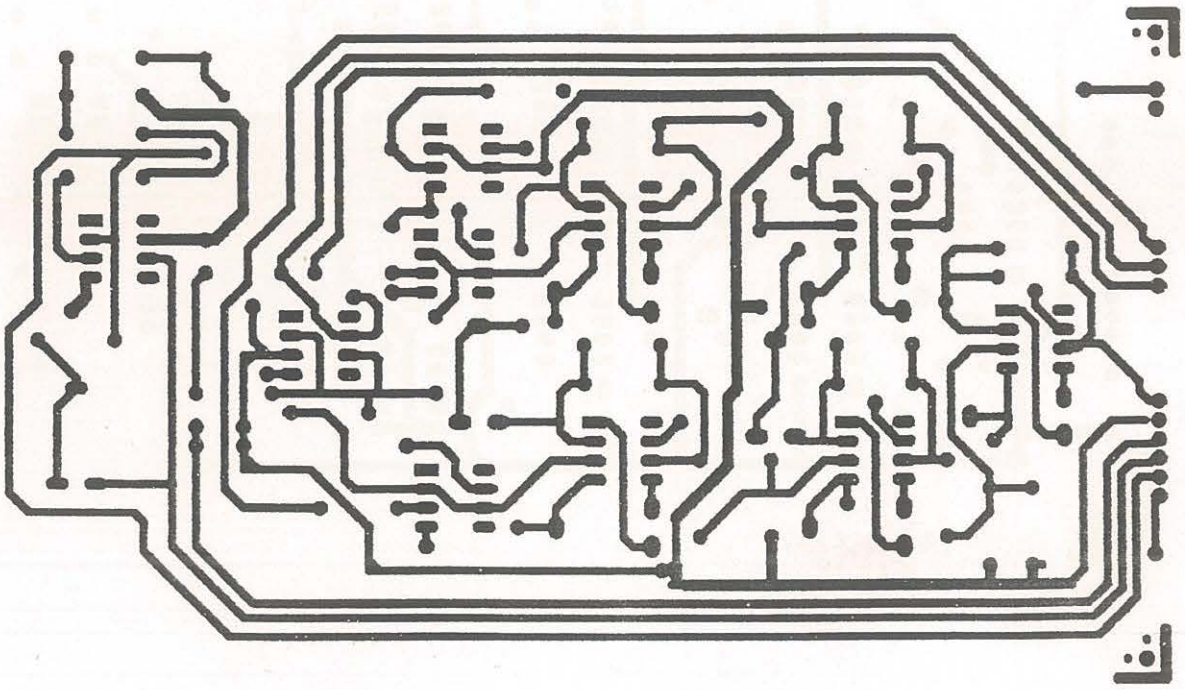
1. Pcb layouts for ECG

(a) Silk side

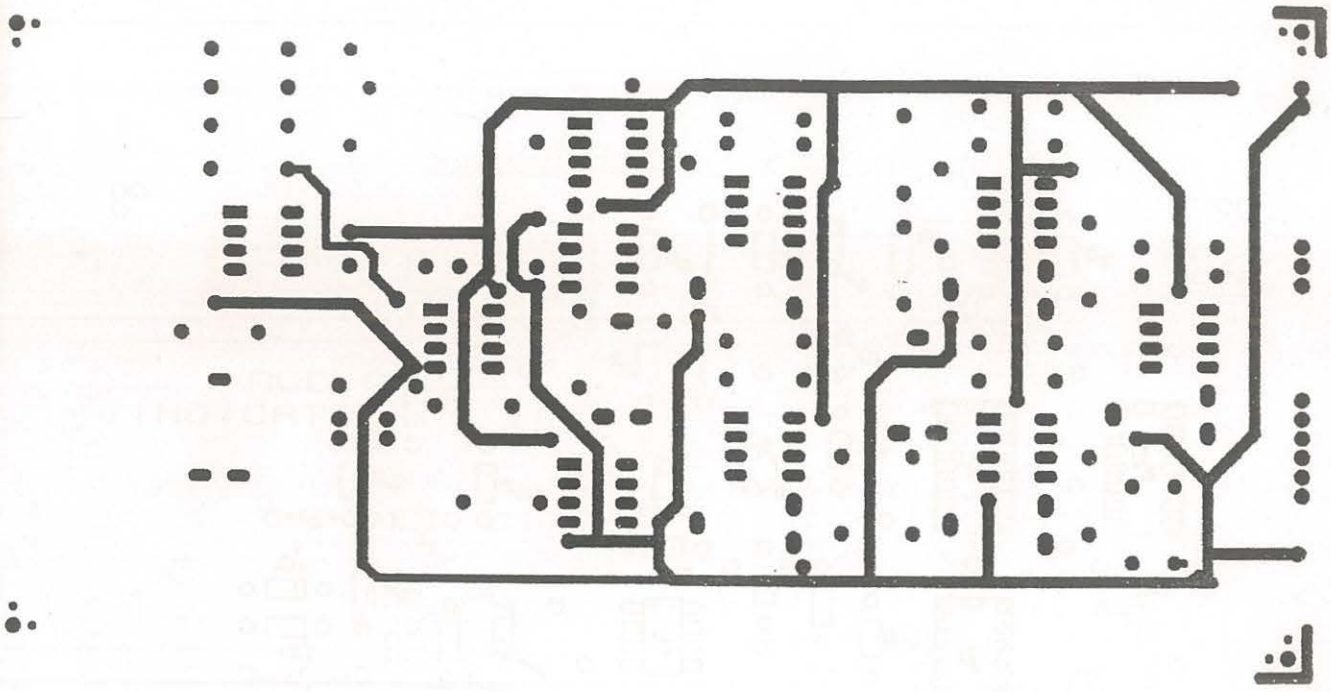


ECG & TC

(b) Solder side

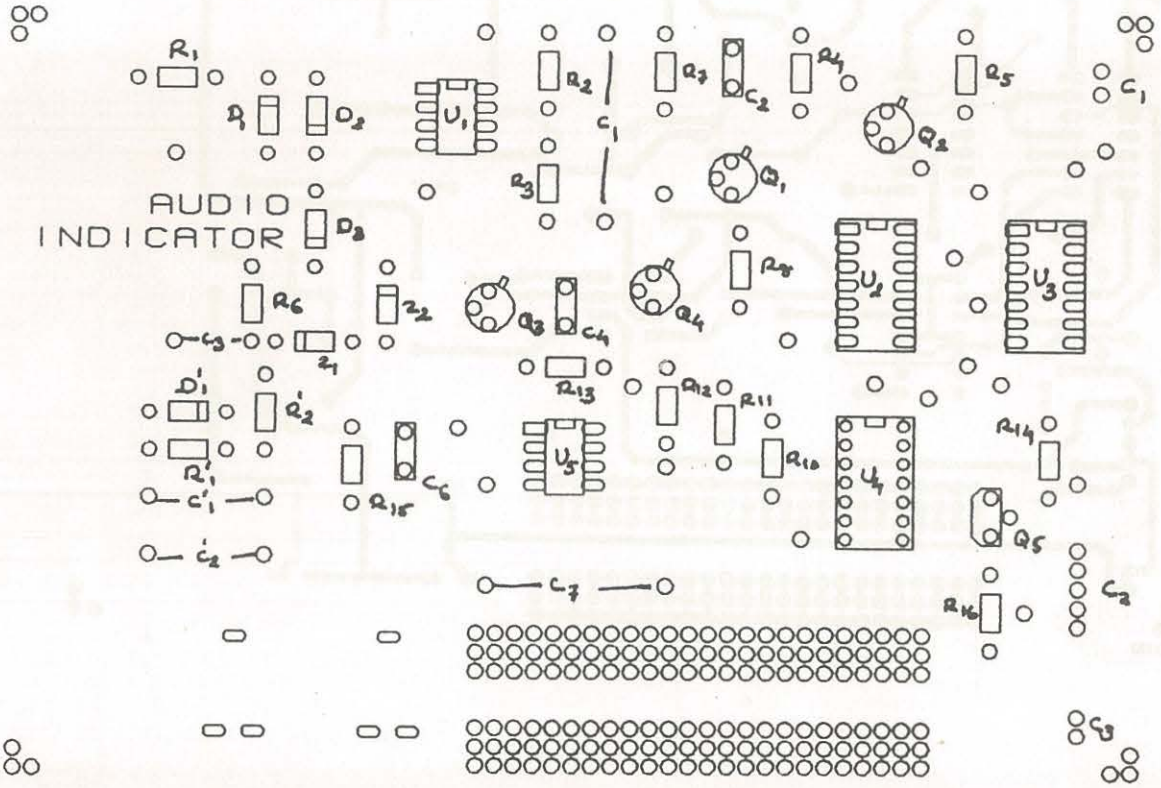


(c) Component side

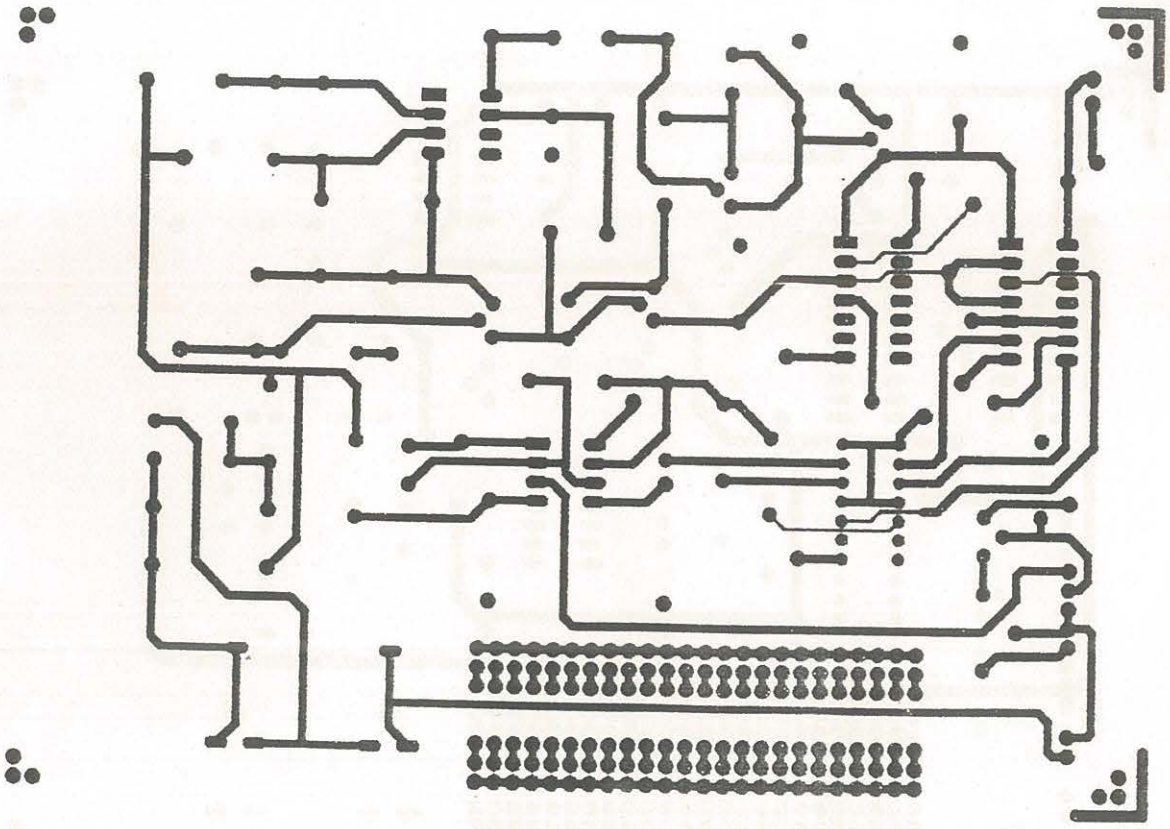


2. Pcb layouts for audio indicator

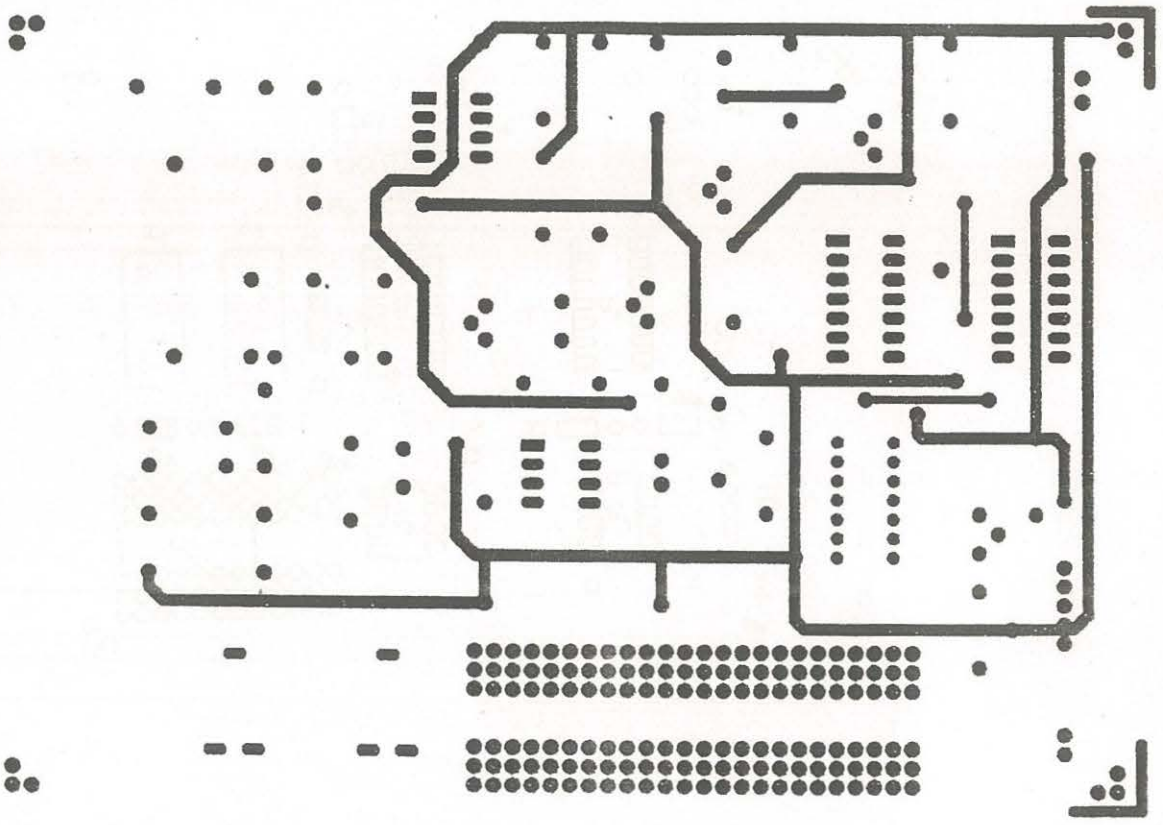
(a) Silk side



(b) Solder side

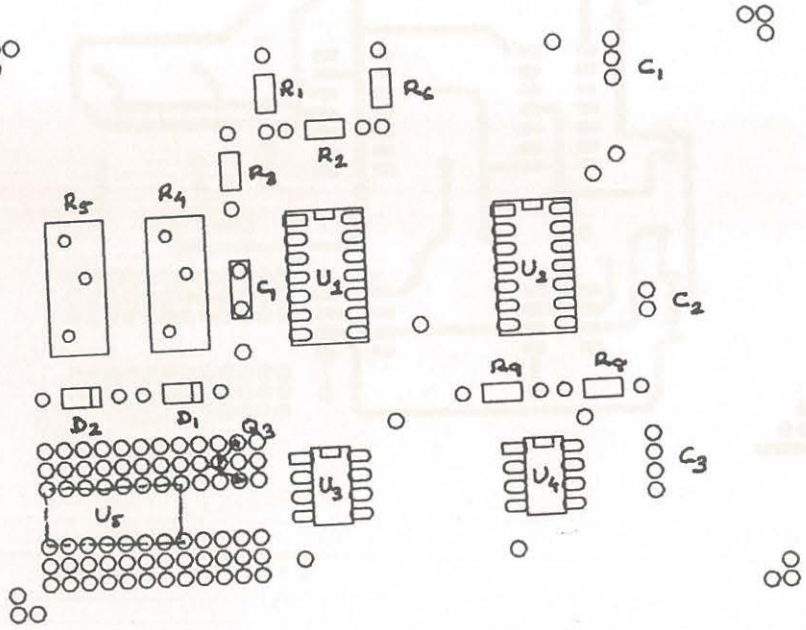


(c) Component side

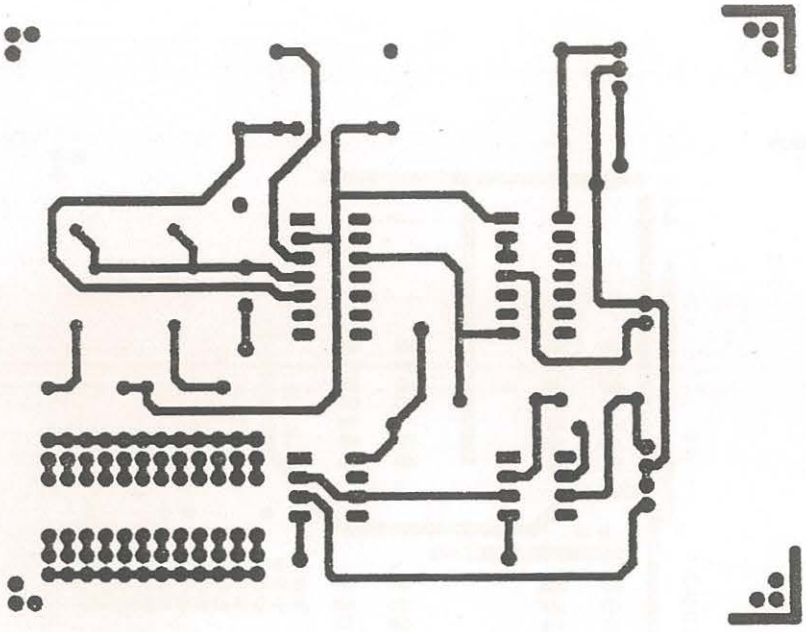


3. Pcb layouts for carrier signal generator

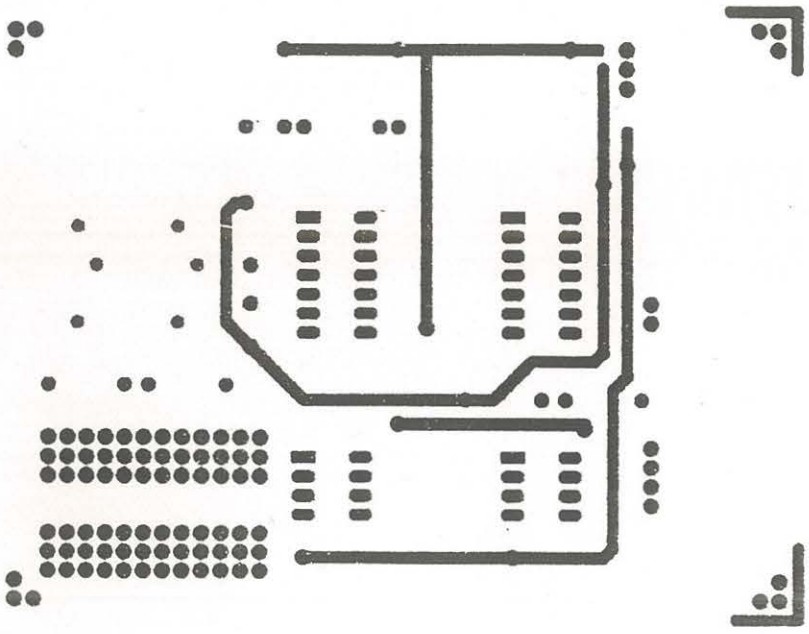
(a) Silk side



(b) Solder side



(c) Component side



APPENDIX D

DATA SHEETS

INTERSIL

AD590

Temperature Transdu

FEATURES

- Linear current output: 1 μA/°K
- Wide range: −55°C to +150°C
- Two-terminal device: Voltage in/current out
- Laser trimmed to ±0.5°C calibration accuracy (AD590M)
- Excellent linearity: ±0.5°C over full range (AD590M)
- Wide power supply range: +4V to +30V
- Sensor isolation from case
- Low cost

GENERAL DESCRIPTION

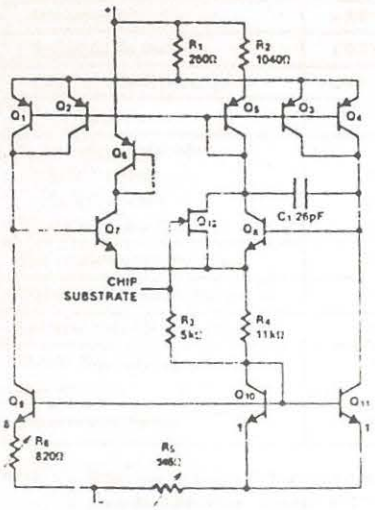
The AD590 is an integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature-sensing application between −55°C and +150°C (0°C and 70°C for TO-92) in which conventional electrical temperatur currently employed. The inherent low cost o integrated circuit combined with the elimination circuitry makes the AD590 an attractive alterna temperature measurement situations. Linear cuitry, precision voltage amplifiers, resistance circuitry and cold-junction compensation are not applying the AD590. In the simplest application, power source and any voltmeter can be used, to temperature.

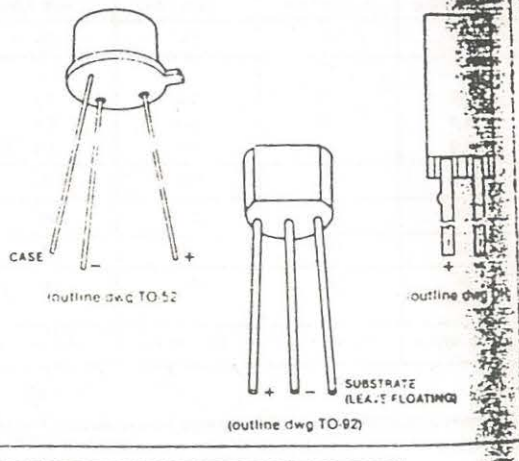
In addition to temperature measurement, applica clude temperature compensation or correction of components, and biasing proportional to absolute ture. The AD590 is available in chip form making it for hybrid circuits and fast temperature measurem protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over lines due to its high-impedance current output. Any insulated twisted pair is sufficient for operation hundred feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

SCHEMATIC DIAGRAM



PIN CONFIGURATIONS



ORDERING INFORMATION

TO-52 and Ceramic Package:
Operate −55°C to +150°C
TO-92:
Operate 0°C to +70°C

NON-LINEARITY (°C)	TO-52 PACKAGE	CERAMIC PACKAGE	TO-92 PACKAGE
±3.0	AD590IH	AD590IF	AD590IZR
±1.5	AD590JH	AD590JF	AD590JZR
±0.8	AD590KH	AD590KF	AD590KZR
±0.4	AD590LH	AD590LF	—
±0.3	AD590MH	AD590MF	—

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Forward Voltage (V^+ to V^-) ..... +44V
Reverse Voltage (V^+ to V^-) ..... −20V
Breakdown Voltage (Case to V^+ or V^-) ..... ±200V
Storage Temperature Range ..... −65°C to +175°C

Rated Performance Temperature Range
TO-92 ..... 0°C to +70°C
TO-52 Ceramic ..... −55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (Typical values at T_A = +25°C, V^+ = 5V unless otherwise noted)

CHARACTERISTICS	AD590I	AD590J	AD590K	AD590L	AD590M	UNITS
Output Nominal Output Current @ +25°C (298.2°K)	298.2	298.2	298.2	298.2	298.2	μA
Nominal Temperature Coefficient	1.0	1.0	1.0	1.0	1.0	μA/°K
Calibration Error @ +25°C (Notes)	±10.0 max	±5.0 max	±2.5 max	±1.0 max	±0.5 max	°C
Absolute Error (−55°C to +150°C) Without External Calibration Adjustment	±20.0 max	±10.0 max	±5.5 max	±3.0 max	±1.7 max	°C
With External Calibration Adjustment	±5.8 max	±3.0 max	±2.0 max	±1.6 max	±1.0 max	°C
Non-Linearity	±3.0 max	±1.5 max	±0.8 max	±0.4 max	±0.3 max	°C
Repeatability (Note 2)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C
Long Term Drift (Note 3)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C/month
Current Noise	40	40	40	40	40	pA/$\sqrt{Hz}$
Power Supply Rejection +4 < V^+ < +5V	0.5	0.5	0.5	0.5	0.5	μA/V
+5 < V^+ < +15V	0.2	0.2	0.2	0.2	0.2	μA/V
+15V < V^+ < +30V	0.1	0.1	0.1	0.1	0.1	μA/V
Case Isolation to Either Lead	10^{10}	10^{10}	10^{10}	10^{10}	10^{10}	Ω
Effective Shunt Capacitance	100	100	100	100	100	pF
Electrical Turn-On Time (Note 1)	20	20	20	20	20	μs
Reverse Bias Leakage Current (Note 4)	10	10	10	10	10	pA
Power Supply Range	+4 to +30	+4 to +30	+4 to +30	+4 to +30	+4 to +30	V

Notes
1. Does not include self heating effects.
2. Maximum deviation between +25°C reading after temperature cycling between −55°C and +150°C (0°C and 70°C for TO-92).
3. Conditions: Constant +5V, constant +125°C.
4. Leakage current doubles every +10°C.
5. Mechanical strain on package (especially TO-92) may disturb calibration of device

IRF430 ■ IRF431 ■ IRF832 ■ IRF833
IRF830 ■ IRF831

IRF430 ■ IRF431 ■ IRF432 ■ IRF433
IRF830 ■ IRF831 ■ IRF832 ■ IRF833

Siliconix

500V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for offline switching regulators, converters, solenoid and relay drivers.

FEATURES

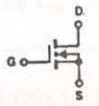
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$r_{DS(ON)}$	I_D	Package
IRF430	500V	1.5Ω	4.5A	TO-3
IRF431	450V			
IRF432	500V	2.0Ω	4A	
IRF433	450V			
IRF830	500V	1.5Ω	4.5A	TO-220AB
IRF831	450V			
IRF832	500V	2.0Ω	4A	
IRF833	450V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- IRF430, 432, 830, 832 ..... 500V
- IRF431, 433, 831, 833 ..... 450V

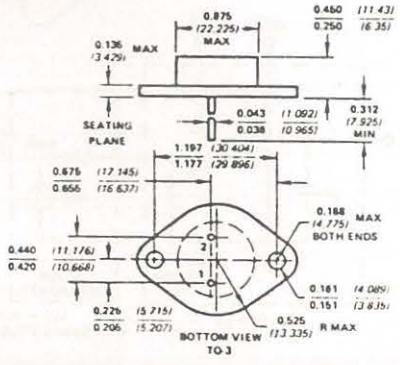
Drain-Gate Voltage
- IRF430, 432, 830, 832 ..... 500V
- IRF431, 433, 831, 833 ..... 450V

Continuous Drain Current, T_C = 25°C[1]
- IRF430, 431, 830, 831 ..... ± 4.5A
- IRF432, 433, 832, 833 ..... ±4A

Pulsed Drain Current[2] ..... ± 18A
Gate-Source Voltage ..... ± 40V
Maximum Power Dissipation 75W
Linear Derating Factor ..... 0.6 W/°C
Operating and Storage Temperature ..... – 55 to 150°C

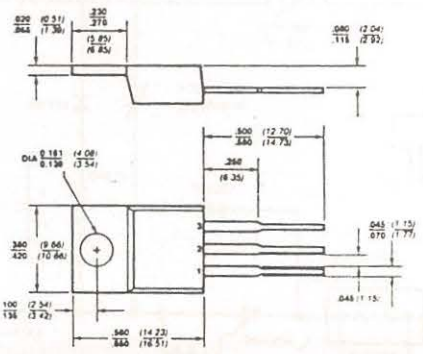
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

TO-204AA (TO-3)



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	IRF430, 2 IRF830, 2	500		V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF431, 3 IRF831, 3	450			
$V_{GS(th)}$	Gate Threshold Voltage	All	2	4		$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	IRF430, 1 IRF830, 1	4.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
		IRF431, 3 IRF831, 3	4.0			
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF430, 1 IRF830, 1		1.5	Ω	$V_{GS} = 10V$, $I_D = 2.5A$ (Note 1)
		IRF432, 3 IRF832, 3		2.0		
Dynamic						
g_{fs}	Forward Transconductance	All	2.5		S	$V_{DS} = 100V$, $I_D = 2.5A$ (Note 1)
C_{iss}	Input Capacitance	All		800	pF	$V_{GS} = 0$, $V_{DS} = 25V$, $f = 1$ MHz
C_{oss}	Output Capacitance			200		
C_{rss}	Reverse Transfer Capacitance			60		
$t_{d(on)}$	Turn-On Delay Time	All		30	ns	$V_{DD} = 200V$, $I_D \approx 2.5A$, $R_L = 80\Omega$, $R_g = 10\Omega$ (Fig. 1)
t_r	Rise Time	All		30		
$t_{d(off)}$	Turn-Off Delay Time	All		55		
t_f	Fall Time	All		30		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward On Voltage	All	−1.2		V	$I_S = -4.5A$ $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All	400		ns	$I_F = I_R = -4.5A$, $V_{GS} = 0$(Fig. 2)

Note:
1. Pulse test: 80 μs-300 μs, 1% duty cycle.

Refer to VNDA50 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

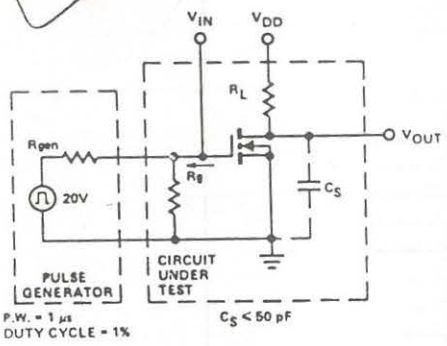
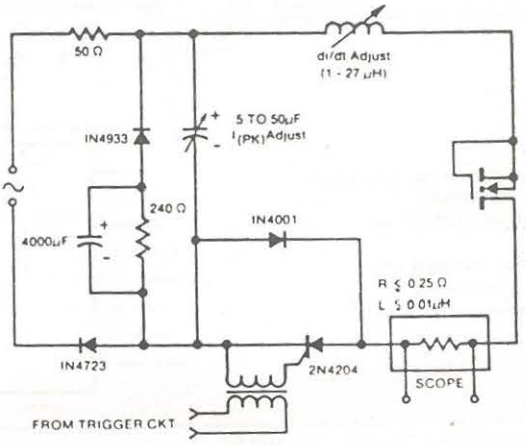


FIGURE 2 JEDEC Reverse Recovery Circuit



LM1524/LM2524/LM3524 Regulating Pulse Width Modulator

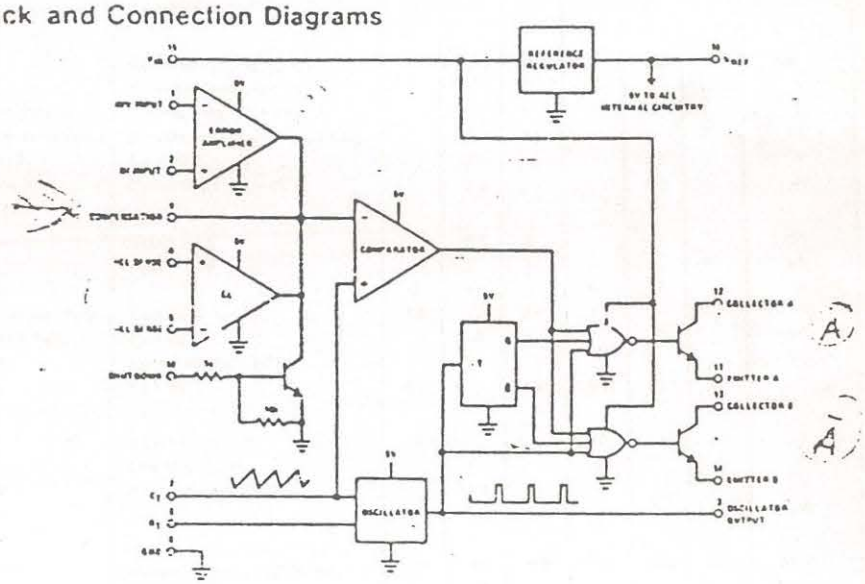
General Description

The LM1524 series of regulating pulse width modulators contains all of the control circuitry necessary to implement switching regulators of either polarity, transformer coupled DC to DC converters, transformerless polarity converters and voltage doublers, as well as other power control applications. This device includes a 5V voltage regulator capable of supplying up to 50 mA to external circuitry, a control amplifier, oscillator, a pulse width modulator, a phase splitting flip-flop, dual alternating output switch transistors, and current limiting and shut down circuitry. Both the regulator output transistor and each output switch are internally current limited and, to limit junction temperature, an internal thermal shutdown circuit is employed. The LM1524 is rated for operation from −55°C to +125°C and is packaged in a hermetic 16-lead DIP (J). The LM2524 and LM3524 are rated for operation from 0°C to +70°C and are packaged in either a hermetic 16-lead DIP (J) or 16-lead molded DIP (N).

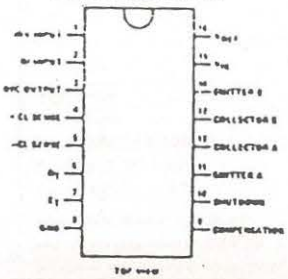
Features

- Complete PWM power control circuitry
- Frequency adjustable to greater than 100 kHz
- 2% frequency stability with temperature
- Total quiescent current less than 10 mA
- Dual alternating output switches for both push pull or single-ended applications
- Current limit amplifier provides external component protection
- On chip protection against excessive junction temperature and output current
- 5V, 50 mA linear regulator output available to user

Block and Connection Diagrams



Dual-In-Line Package



Order Number LM1524J, LM2524J or LM3524J
See NS Package J16A

Order Number LM2524N or LM3524N
See NS Package N16A

[illegible]	40V
[illegible]	6V
Reference Output Current	50 mA
Output Current (Each Output)	100 mA
Oscillator Charging Current (Pin 6 or 7)	5 mA
Internal Power Dissipation (Note 1)	1W
Operating Temperature Range	
LM1524	−55°C to +125°C
LM2524/LM3524	0°C to +70°C
Maximum [illegible]	
(J Package)	
(N Package)	
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the LM1524 and 0°C to +70°C for the LM2524 and LM3524. V_{IN} = 20V, and f = 20 kHz. Typical values other than temperature coefficients, are at T_A = 25°C.

PARAMETER	CONDITIONS	LM1524/ LM2524			LM3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8–40V		10	20		10	30	mV
Load Regulation	I_L = 0–20 mA		20	50		20	50	mV
Ripple Rejection	f = 120 Hz, T_A = 25°C		66			66		dB
Short-Circuit Output Current	V_{REF} = 0, T_A = 25°C		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	T_A = 25°C		20			20		mV/kHr
Oscillator Section								
Maximum Frequency	C_T = 0.001 µF, R_T = 2 kΩ		350			350		kHz
Initial Accuracy	R_T and C_T constant		5			5		%
Frequency Change with Voltage	V_{IN} = 8–40V, T_A = 25°C			1			1	%
Frequency Change with Temperature	Over Operating Temperature Range			2			2	%
Output Amplitude (Pin 3)	T_A = 25°C		3.5			3.5		V
Output Pulse Width (Pin 3)	C_T = 0.01 µF, T_A = 25°C		0.5			0.5		µs
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
Input Bias Current	V_{CM} = 2.5V		2	10		2	10	µA
Open Loop Voltage Gain		72	80		60	80		dB
Common-Mode Input Voltage Range	T_A = 25°C	1.8		3.4	1.8		3.4	V
Common-Mode Rejection Ratio	T_A = 25°C		70			70		dB
Small Signal Bandwidth	A_V = 0 dB, T_A = 25°C		3			3		MHz
Output Voltage Swing	T_A = 25°C	0.5		3.8	0.5		3.8	V
Comparator Section								
Maximum Duty Cycle	% Each Output ON	45			45			%
Input Threshold (Pin 9)	Zero Duty Cycle		1			1		V
Input Threshold (Pin 9)	Maximum Duty Cycle		3.5			3.5		V
Input Bias Current			−1			−1		µA
Current Limiting Section								
Sense Voltage	$V_{(Pin\ 2)} - V_{(Pin\ 1)} \geq 50$ mV, Pin 9 = 2V, T_A = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/°C
Common-Mode Voltage		−0.7		1	−0.7		1	V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_{CE} = 40V		0.1	50		0.1	50	µA
Saturation Voltage	I_C = 50 mA		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V, I_E = −250 µA	17	18		17	18		V
Rise Time (10% to 90%)	R_C = 2 kΩ, T_A = 25°C		0.2			0.2		µs
Fall Time (90% to 10%)	R_C = 2 kΩ, T_A = 25°C		0.1			0.1		µs
Total Standby Current	V_{IN} = 40V, Pins 1, 4, 7, 8, 11 and 14 are grounded, Pin 2 = 2V, All Other Inputs and Outputs Open		5	10		5	10	mA

Note 1: For operation at elevated temperatures, devices in the J package must be derated based on a thermal resistance of 100°C/W, junction to ambient, and devices in the N package must be derated based on a thermal resistance of 160°C/W junction to ambient.

Preliminary Data Sheet No. PD-6.011

INTERNATIONAL RECTIFIER IOR

HIGH VOLTAGE BRIDGE DRIVER

IR2110

14-PIN MOLDED DIP PACKAGE

General Description

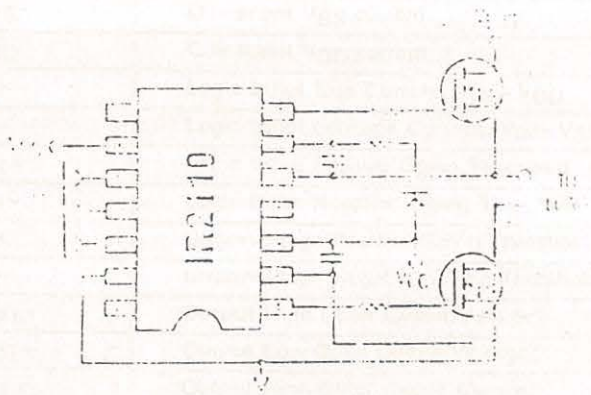
The IR2110 is a monolithic high voltage and high speed dual driver with independent floating rail high side and fixed rail low side referenced output channels. The device inputs are compatible with standard CMOS outputs or with LSTTL outputs using pullup resistors. Unique HVIC technology and circuit design enable high speed and low dissipation translation of the logic level inputs into corresponding low impedance output swings with respect to the floating and the fixed supply rail. The floating channel can be configured to drive an n-channel power MOSFET or IGBT whose source voltage is up to 500 volts from the IR2110 common pin.

The IR2110 is typically used to drive high voltage switching power MOSFETs or IGBTs in half-bridge, push-forward or other topologies. Applications include switching power supplies, motor controls, inverters, [illegible] audio amplifiers and high energy pulse circuits.

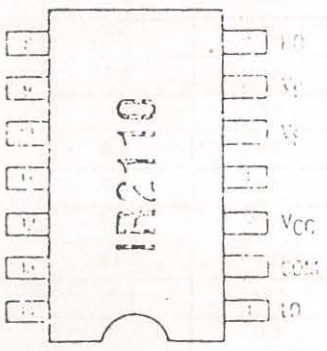
Features

- 500V rated floating supply offset voltage
- 10V/ns floating supply dv/dt immunity
- 2A peak output current capability per channel
- 25ns switching time with 1000pf load
- 100ns propagation delay time
- 1 to 5 MHz maximum repetitive rate depending on power dissipation
- CMOS Schmitt-triggered inputs with hysteresis
- 10 to 20V output drive operating voltage range
- 15mW total quiescent power dissipation with 15V supply
- Under-voltage lockout

Typical Connection



Pinout Assignment



For mechanical specifications see back page

Absolute DC Ratings①

(Refer to the Functional Block Diagram section for the definitions and references of the parameters.)

Symbol	Parameters	Min	Max	Unit
V_S	Offset Supply Voltage	–	500	V
V_{BS}	Floating Supply Voltage	– 0.5	25	
V_{HO}	High Side Channel Output Voltage	– 0.5	V_{BS} + 0.5	
V_{CC}	Fixed Supply Voltage	– 0.5	25	
V_{LO}	Low Side Channel Output Voltage	– 0.5	V_{CC} + 0.5	
V_{DD}	Logic Supply Voltage	– 0.5	25	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	– 0.5	V_{DD} + 0.5	

Recommended DC Operating Conditions

Symbol	Parameters	Min	Max	Unit
V_{BS}	Floating Supply Voltage	10	20	V
V_{HO}	High Side Channel Output Voltage	0	V_B	
V_{CC}	Fixed Supply Voltage	10	20	
V_{LO}	Low Side Channel Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	3	V_{CC}	
V_{IN}	Logic Input Voltage (HIN, LIN, SD)	0	V_{DD}	
V_{SS}	Logic Supply Offset Voltage	– 1.0	1.0	

Maximum Transient Conditions

Symbol	Parameters	Max	Unit
dV_{BS}/dt	Floating Supply Startup Transient②	75	V/us
dV_S/dt	Offset Supply Operating Transient③	10	V/ns

Thermal Characteristics

Symbol	Parameters	Min	Max	Unit
P_D	Package Power Dissipation @ T_A < = 25 C	—	1500	mW
R_{thJA}	Thermal Resistance, Junction to Ambient	—	70	C/W
T_{Jmax}	Maximum Junction Temperature	—	150	C
T_S	Storage Temperature	– 55	150	
T_L	Lead Temperature (soldering, 10 seconds)	–	300	
T_A	Operating Ambient Temperature	– 40	125	

Static Electrical Characteristics④

(V_{CC} = V_{BS} = V_{DD} = 15V, COM = V_{SS} = 0V and T_A = 25°C unless otherwise specified)

Symbol	Parameters	Min	Typ	Max	Unit
I_{QCC}	Quiescent V_{CC} current	100	300	600	uA
I_{QBS}	Quiescent V_{BS} current	300	500	600	
I_{QDD}	Quiescent V_{DD} current	–	15	30	
I_{IN+}	Logic Input Bias Current, V_{IN} = V_{DD}	–	7.5	15	
I_{IN-}	Logic Input Leakage Current, V_{IN} = V_{SS}	–	–	0.1	
V_{TH+}	Logic Input Positive Going Threshold	8.2	8.7	9.2	V
V_{TH-}	Logic Input Negative Going Threshold	7.0	7.5	8.0	
UV_+	Undervoltage Positive Going Threshold	9.2	9.6	10.0	
UV_-	Undervoltage Negative Going Threshold	8.2	8.6	9.0	
V_{OUT+}	Output High Open Circuit Voltage⑤	13.5	14.0	14.5	
V_{OUT-}	Output Low Open Circuit Voltage⑤	–	—	0.1	
I_{OUT+}	Output High Short Circuit Current⑤	–	2.0	–	A
I_{OUT-}	Output Low Short Circuit Current⑤	–	2.0	–	

Notes See Next Page

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