INSTRUMENTATION FOR

IMPEDANCE CARDIOGRAPHY

A dissertation submitted in

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by

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ABSTRACT

Impedance cardiography is a non-invasive method for estimating the stroke volume and cardiac output by sensing the variation in thoracic impedance during the cardiac cycle. The project objective is to develop an impedance cardiograph, based on earlier reported developments as well as by investigating new circuits for improving the performance. The impedance cardiography hardware involves new approaches to the excitation source as well as the demodulator for sensing the small variation in thoracic impedance. Modified Howland current source is used for the voltage-to-current conversion. For stable sinusoidal excitation with a selectable frequency, a DDS chip is used. Two DDS chips are synchronized to provide outputs with settable phase shift, one DDS providing input to the voltage-to-current converter while the output of the other DDS is used as reference for synchronous demodulation. For high sensitivity, low distortion, and low noise demodulation, a slicing amplifier and sample-and-hold based circuit is devised and tested. The overall circuit is controlled by a microcontroller, providing flexibility in selection of the frequency, current level, the phase shift of the demodulator reference, and the base impedance to be subtracted from the sensed impedance. A thorax simulator for testing and calibration of an impedance cardiograph using microcontroller and digital potentiometers has been developed and prototyped.

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Chapter 1
INTRODUCTION

1.1 Background

Sensing of the variation in the bioimpedance across a body segment can be used for noninvasive monitoring of the changes in the fluid volume or underlying physiological events [1]-[12]. Impedance cardiography is a noninvasive method for estimating the stroke volume and cardiac output by sensing the variation in thoracic impedance during the cardiac cycle. The bioimpedance is generally measured by passing an alternating current through a pair of surface electrodes (spot or band electrodes). The voltage resulting across the body segment, sensed using the same or another pair of electrodes, gets amplitude modulated due to the impedance variation. This voltage is demodulated to get the impedance signal. In order to avoid any physiological effects, the measurements of bio-impedances is carried out using a low-level current (<5 mA) in the frequency range of 20 kHz to 1 MHz [1], [3]. Higher the frequency used; easier it is to eliminate the carrier ripple from the demodulated output. For impedance cardiography, the frequency used is generally in the range of 50 kHz to 500 kHz, and most commonly about 100 kHz [4]-[8]. In this frequency range, the tissues are not excitable (except possibly at very high current levels) and the impedance is nearly resistive. The basal impedance of the thorax is about 20 Ω to 200 Ω and the change in the impedance is less than 2 %.

1.2 Project objective

Work for developing impedance cardiography instrumentation has been carried out earlier at IIT Bombay [13]-[16]. Objective of the project is to develop a prototype by investigating the limitations of earlier designs and improving them. A thorax simulator is developed for testing and calibration of the ECG and the ICG hardware. Earlier developed hardware blocks of the impedance cardiographs are studied. The ICG hardware consists of a current source realized using an oscillator and a voltage-to-current converter and the amplitude demodulator section in the impedance detector. To provide the flexibility of using a variable excitation frequency, a programmable waveform generator based on direct digital synthesizer (DDS) is tested. Several voltage-to-current converter circuits are tested. The demodulator should provide noise rejection, carrier ripple rejection, and high sensitivity. A

slicing amplifier with a sample-and-hold based demodulator circuit is developed for this purpose. Finally the impedance cardiography instrument is prototyped using modified and existing circuit blocks.

1.3 Report outline

Chapter 2 covers basics of the impedance cardiography. Chapter 3 includes basics of thorax simulator model and circuit design. The fourth chapter describes details of the hardware for impedance cardiography. In Chapter 5, test and results are discussed. Summary and conclusion are given in the last chapter, and supplementary information is provided in the appendix.

Chapter 2

BASICS OF IMPEDANCE CARDIOGRAPHY

2.1 Cardiac cycle, stroke volume, and cardiac output

The time period between two successive contractions of the heart is known as the cardiac cycle [18]. Each cycle consists of diastole (the relaxation phase) and systole (the contraction phase). The different events like the various pressure changes, the change in the ventricular volume, the electrocardiogram, and the phonocardiogram during the cardiac cycle are shown in Fig. 2.1. As the ventricular contraction starts, the A–V valve closes. The ventricular pressure exceeds the aortic pressure, the aortic valves opens and the blood is delivered to the aorta. When the ventricular pressure drops below the aortic pressure, the aortic valve closes.

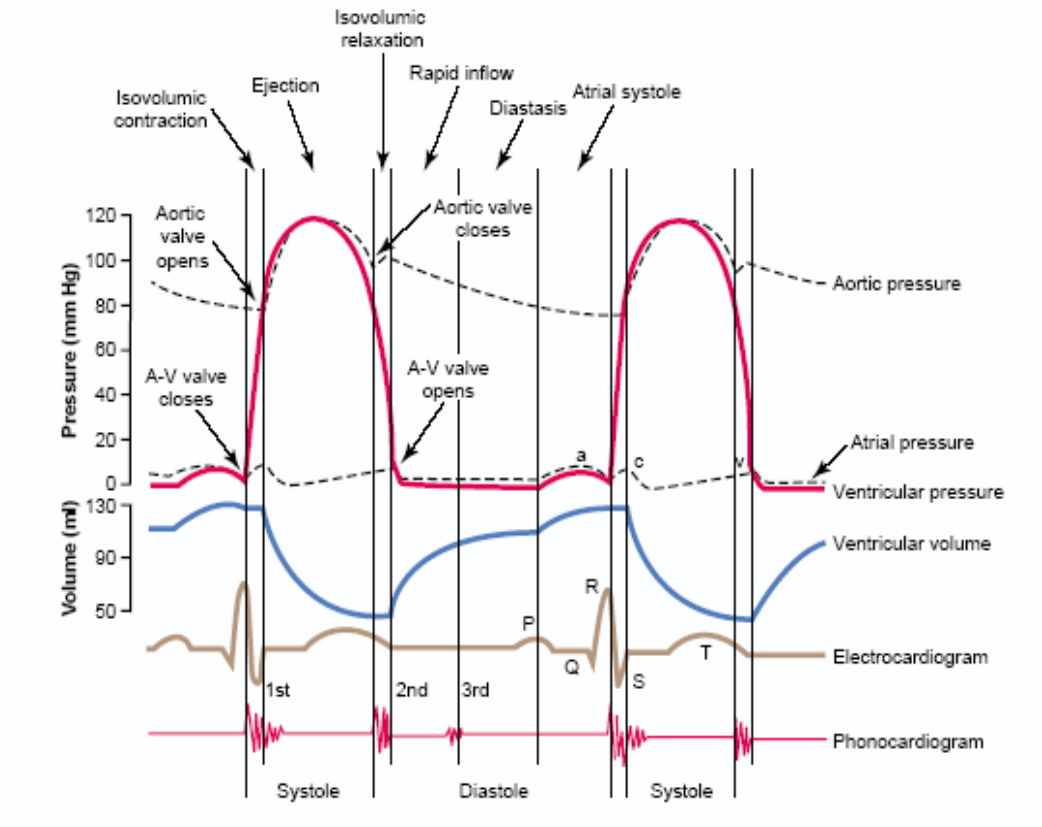

Fig. 2.1 Various events during the cardiac cycle [18].

The electrical potential generated by the heart may be recorded using surface electrodes as the electrocardiogram, while the sound produced by the heart valves can be recorded as the phonocardiogram.

The stroke volume (SV) is the amount of blood ejected by the ventricle in each beat. It is calculated by subtracting the end-systolic volume of the blood from the end-diastolic volume. The cardiac output (CO) is a measure of the amount of the blood ejected each minute. It is calculated by multiplying the heart rate (beats/minute) with the stroke volume. The average stroke volume for a healthy adult is about 70 mL/beat. With the heart rate of about 72 beats/min, the CO is 5.04 L/min.

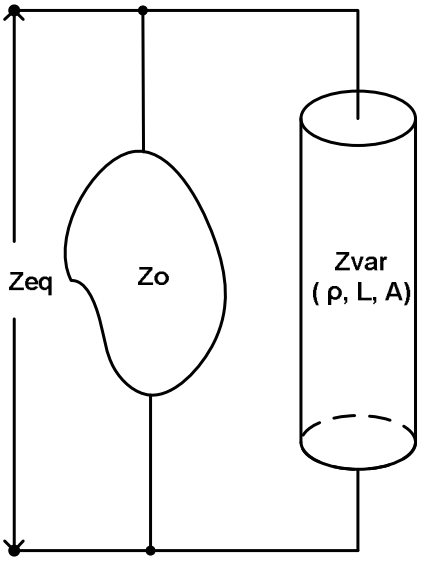

Fig. 2.2 Parallel column impedance model [1], [4]

2.2 Impedance Cardiography

The impedance cardiography is a non–invasive method to measure the cardiac output. The method is based on the principle that the thoracic impedance varies during ventricular contraction due to inflow of blood in the thorax region. The variation in the impedance is sensed by injecting a high frequency (50 kHz – 500 kHz) low amplitude (< 5 mA) current through a pair of electrodes and sensing the resulting amplitude modulated voltage using another pair placed in between the current injecting electrodes. Thus the CO can be estimated by measuring the change in the thoracic impedance.

It may be noted that the impedance sensed is almost resistive. In the modeling of the thorax region, the term impedance has become established in the literature, but it basically reference to resistance. The two parallel columns impedance model of the thoracic region was proposed by Kubicek *et. al.* [4] to obtain the formula relating change in the thoracic impedance to the SV. The model is shown in Fig. 2.2. The impedance Z_o represent fixed base impedance and Z_{var} represents variable impedance with the following parameters,

ρ = Resistivity,

L = Length of conductor,

A = Cross sectional area.

The equivalent impedance of the parallel column is given by,

$$Z_{eq}(t) = Z_o \| Z_{var}(t) \tag{2.1}$$

The change in the impedance is given by,

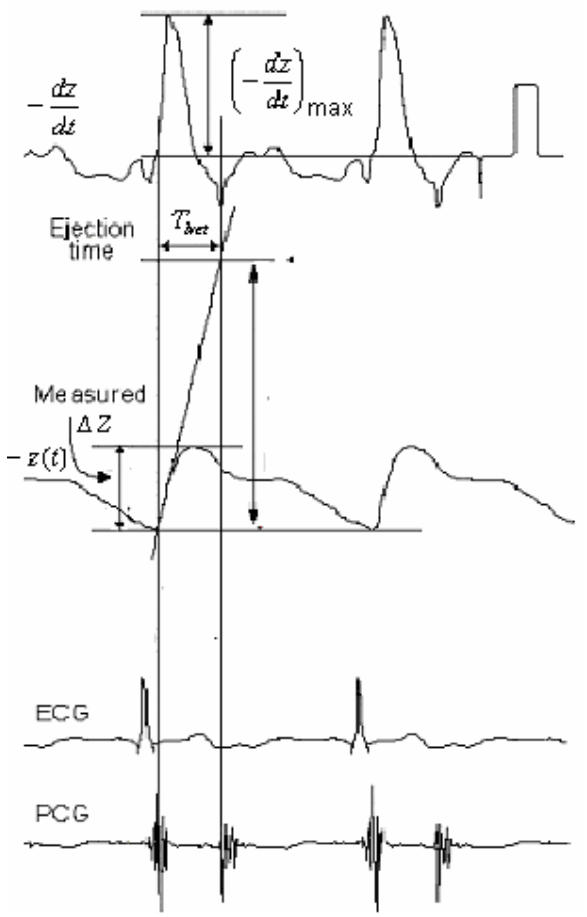

Fig. 2.3 Impedance variation signal and impedance cardiogram [6]

$$z(t)=Z_{eq}(t)-Z_o=-\frac{Z_o^2}{Z_o+Z_{var}(t)} \tag{2.2}$$

As, $Z_{var}(t) >> Z_o$, Z_o in the denominator can be neglected.

$$z(t)=-\frac{Z_o^2}{Z_{var}(t)} \tag{2.3}$$

The impedance $Z_{var}(t)$ can be written as,

$$Z_{var}(t)=\frac{\rho L}{A(t)}$$

$$=\frac{\rho L^2}{V(t)} \tag{2.4}$$

where, $V(t)$ = volume of the cylindrical conductor. Substituting $Z_{var}(t)$ in Eq. 2.3 gives,

$$z(t) = -\left(\frac{Z_o{}^2}{\rho L^2}\right) V(t) \tag{2.5}$$

It was assumed in the model that the inflow of the blood in the thorax during systole is the source of the impedance change and the volume of the variable impedance column is zero before the systole. During systole, the impedance starts decreasing as the volume of the cylindrical column changes. The maximum change in the impedance corresponds to the maximum change in the volume during the systole assuming no blood leaves the thorax. The maximum decrease in the resistance ΔZ and the maximum increase in the volume ΔV can be related as,

$$\Delta V = \frac{\rho L^2}{Z_o{}^2} \Delta Z \tag{2.6}$$

To take into account the blood that leaves the thorax during the later part of the systole, the forward extrapolation technique was used as shown in Fig. 2.3 [6]. The impedance variation signal is plotted as $-Z(t)$. The first derivative of the impedance variation signal ($-dz/dt$) is known as the impedance cardiogram. The most negative deflection $(-dz/dt)_{max}$ is used for the calculation of the stroke volume. Thus the stroke volume (SV) is given as**,**

$$\mathrm{SV} = \left(\frac{\rho \times L^2}{Z_o{}^2}\right)\left(-\frac{dz}{dt}\right)_{max} T_{lvet} \tag{2.7}$$

The left ventricular ejection time (T_{lvet}) is the difference between the last upward zero crossing time and the time at which most downward deflection of the impedance cardiogram takes place.

2.3 Electrode configuration

The impedance measurement is carried out using two- or four-electrode configuration [6], [7]. In the two-electrode configuration, the same set of electrodes is used for current injection and voltage sensing. The current density is higher near the electrodes than elsewhere in the tissue and the measured impedance generally becomes more dependent on the tissue near the electrodes. In the four-electrode configuration, the current is passed between the two outer electrodes, while the voltage is sensed across the inner electrodes. It generally provides a more uniform current density and also reduces the effect of skin-electrode impedance in the sensed voltage.

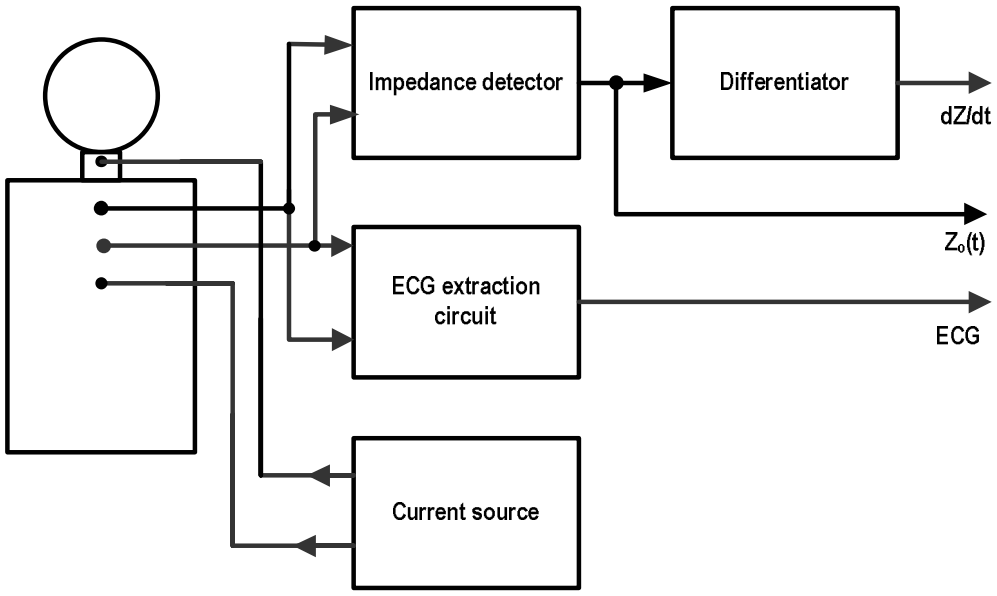

Fig. 2.4 Block diagram of impedance cardiograph

2.4 Impedance cardiograph

An instrument for the impedance cardiography [7]-[16] generally consists of a current source, an impedance detector, an ECG extraction module, current injecting electrodes, voltage sensing electrodes, and contact impedance indicator as shown in Fig. 2.4. The impedance detector mainly includes a voltage sense amplifier, a demodulator, and a drift cancellation circuit. It extracts the impedance variation signal. The ECG extraction circuit extracts the ECG signal which is used as the reference signal. The sensed impedance consists of basal impedance, a time-varying component related to the physiological phenomenon of interest, and various physiological and non-physiological artifacts. For satisfactory operation of the instrument, the impedance detector should have appropriate sensitivity and frequency response. The measurement of the variation in the impedance should not be affected by variation in the basal impedance, the skin-electrode contact impedances, the artifacts, and the external interferences. The cardiograph instruments generally have the facility for connecting an internal resistance across the electrode terminals [19] for calibration of the current source. The current may be amplitude modulated to simulate the modulation of the sensed voltage due to time varying impedance [20]. For a thorough testing and calibration of the instrument, a thorax simulator [19] can be used.

Chapter 3
THORAX SIMULATOR

3.1 Introduction

The thorax simulator is needed for testing and calibration of the ICG and ECG modules of the impedance cardiography instruments. It has two pairs of terminals for connecting to the current and voltage electrodes of the instrument. It has to generate signals of known magnitude and frequency in common mode and in differential mode for testing of ECG extraction circuit. The signals can be used to test the CMRR and the gain of the ECG amplifier. For testing of the ICG extraction circuit, the circuit provides a small settable periodic resistance variation over a base resistance. It is used for finding sensitivity and bandwidth of the ICG extraction circuit. The bioimpedance simulator developed earlier by Manigandan [14] used an astable multivibrator and analog switches for square wave variation in the resistance for testing of the ICG module. The circuit also provided a square wave voltage for measuring the common mode or differential mode gains of the ECG module. It could be used in one of these modes at a time. Manual switches and potentiometers were used for setting the controls. In order to reduce the wiring related pickups and to improve the operational flexibility, Naidu [15] redesigned the hardware, by introducing a microcontroller for controlling the analog switches and two keys and LCD for setting the modes and parameters. All the basic features remained the same as in the earlier circuit. Venkatachalam [16] developed another instrument in which the analog switch based step variation in resistance was replaced with a digital potentiometer based circuit, for providing step, sinusoidal, and other type of resistance variations. Simulated ECG was a square wave like in the earlier two circuits.

After studying the requirements for testing and calibration of impedance cardiograph, it was decided to redesign the simulator for introducing the following features

1. Several wave shapes (sine, square, triangular, etc) for the simulated resistance variation and the ECG.
2. Simultaneous simulation of resistance variation and ECG.
3. Extension of the frequency range of the waveform for permitting the use of the simulator in applications involving measurement of other bioimpedances, e.g., impedance glottography.

3.2 Thorax simulator model

For the purpose of impedance cardiography, the thorax can be modeled by a network as shown in Fig. 3.1 [19]. It represents the basal resistance, variation in the resistance related to the cardiac cycle, ECG voltage, electrode-tissue contact resistances, and externally introduced common mode interference [19]. The terminals I1 and I2 are the current injection terminals and the voltage drop is sensed across the terminals E1 and E2. The resistances R_e's represent tissue-electrode impedances, while R_s's (R_{s1}, R_{s2}) represent the impedances outside the segment across which the voltage is sensed. The impedance of the thoracic segment contributing to the sensed voltage is $R_s \| R_O$. The resistance R_s varies with the cardiac cycle. The voltage sources V_d and V_c represent the difference and the common mode voltages from the internal bioelectric sources. In order to represent common mode voltage with respect to an internal reference point, the resistance R_o is represented as two resistances in series. The voltage source V_p in series with resistance R_p represents the common mode interference from external sources.

The thorax model of Fig. 3.1 has two voltage sources without a common node. For realizing it as a circuit without using transformers, the model can be modified to the schematic shown in Fig. 3.2. The sources Vx1 and Vx2 are kept in phase and out of

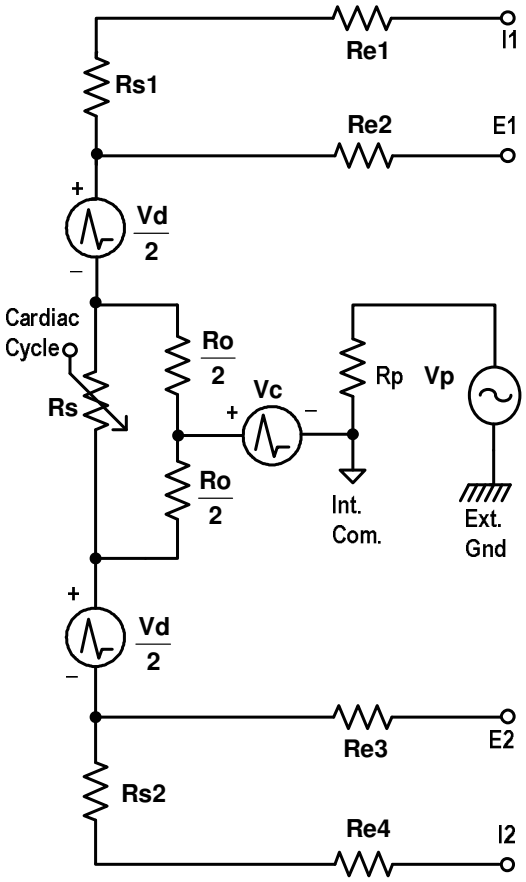

Fig. 3.1 Thorax model

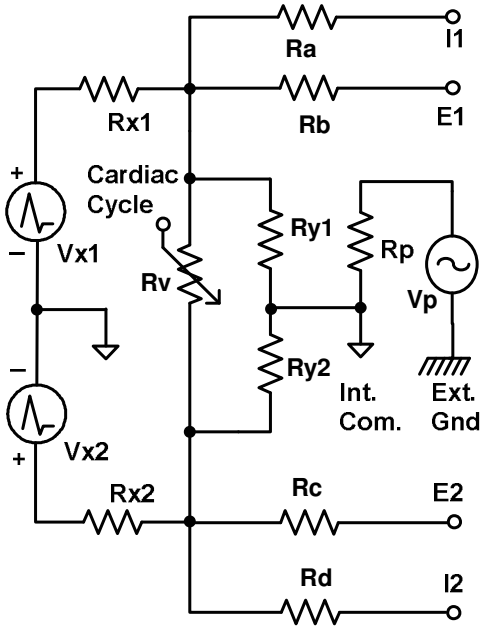

Fig.3.2 Schematic of the thorax simulator

phase for realizing Vc and Vd respectively. The relations between the component values in the thorax model of Fig. 3.1 and those of the schematic shown in Fig. 3.2 are as the following,

$$R_{s1} + R_{e1} = R_a \tag{3.1}$$

$$R_{e2} = R_b \tag{3.2}$$

$$R_{e3} = R_c \tag{3.3}$$

$$R_{s2} + R_{e4} = R_d \tag{3.4}$$

$$R_0 \,||\, R_s = R_v \,||\, \left(\left(R_{x1} \,||\, R_{y1} \right) + \left(R_{x2} \,||\, R_{y2} \right) \right) \tag{3.5}$$

$$V_c + V_d / 2 = \left(R'_{y1} / \left(R_{x1} + R'_{y1} \right) \right) V_{x1} \tag{3.6}$$

$$V_c - V_d / 2 = \left(R'_{y2} / \left(R_{x2} + R'_{y2} \right) \right) V_{x2} \tag{3.7}$$

where $R'_{y1} = R_{y1} \,||\, \left(R_v + \left(R_{x2} \,||\, R_{y2} \right) \right)$

$R'_{y2} = R_{y2} \,||\, \left(R_v + \left(R_{x1} \,||\, R_{y1} \right) \right)$

With $R_{x1} = R_{x2} = R_x$ and $R_{y1} = R_{y2} = R_y$

$$R_0 \,||\, R_s = R_v \,||\, \left(2 \left(R_x \,||\, R_y \right) \right) \tag{3.8}$$

$$V_c + V_d / 2 = \left(R'_y / \left(R_x + R'_y \right) \right) V_{x1} \tag{3.9}$$

$$V_c - V_d / 2 = \left(R'_y / \left(R_x + R'_y \right) \right) V_{x2} \tag{3.10}$$

where $R'_{y1} = R_y \,||\, \left(R_v + \left(R_x \,||\, R_y \right) \right)$

$R'_{y2} = R_y \,||\, \left(R_v + \left(R_x \,||\, R_y \right) \right)$

3.3 Simulator circuit

The variation in the thoracic resistance due to cardiovascular activity is a small percentage (< 2 %) of the basal resistance (20 – 200 Ω). For digital control of the variation in the thoracic resistance, it is modeled as a fixed resistance in parallel with a variable resistance with a value much larger than the on-resistance of the analog switches (typically 50 – 200 Ω). For obtaining the frequency response of the impedance detector, a sinusoidal variation in the resistance can be used. For a quick estimation of the response, a square wave variation

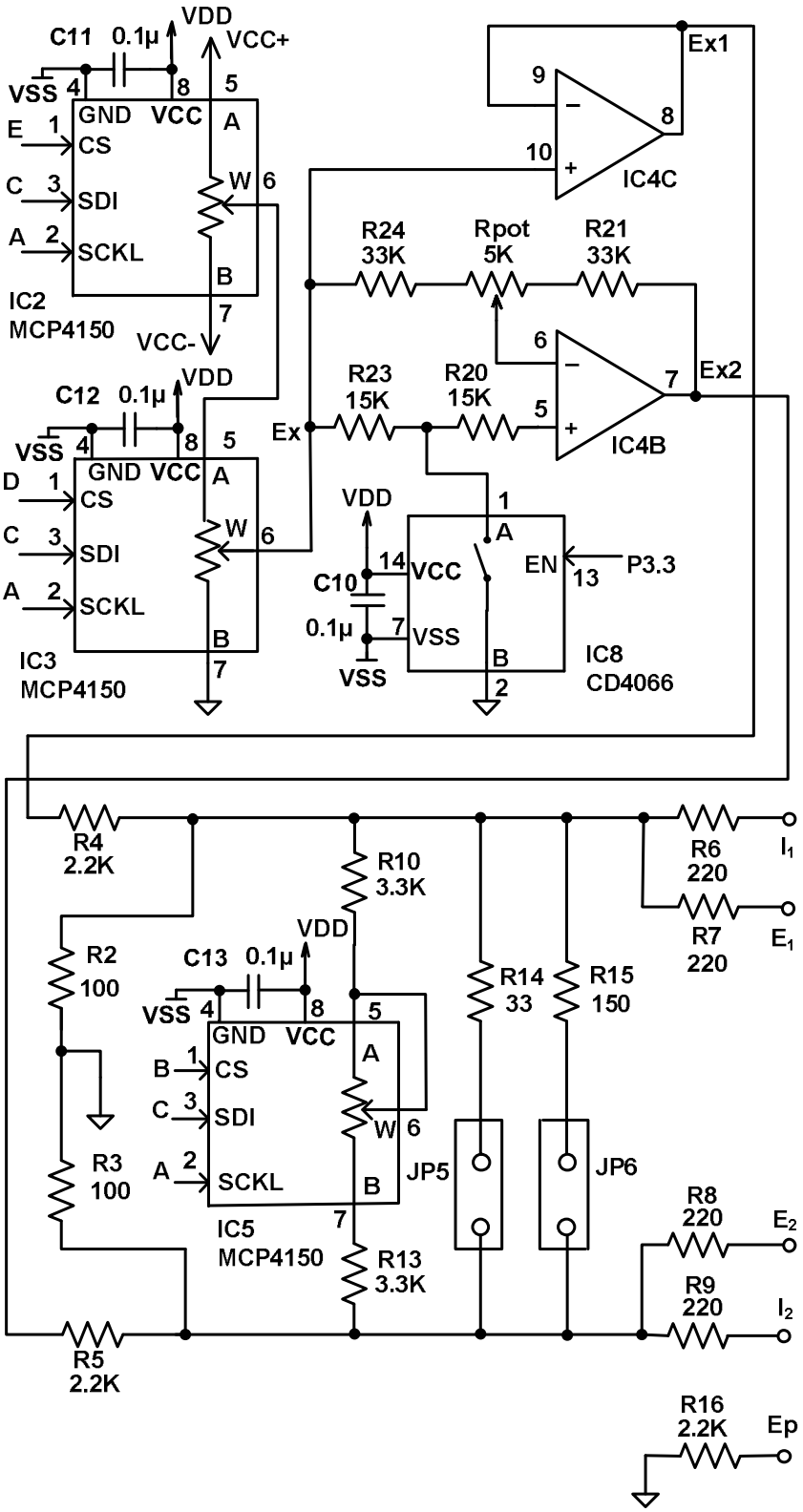

Fig. 3.3 Thorax simulator circuit

can be used [21]. Use of a microcontroller and a digital potentiometer permits us to select the frequency and waveshape of the variation in the resistance.

The circuit of the thorax simulator is shown in Fig. 3.3. The resistance variation is realized using the digital potentiometer IC5 (MCP4150-502E/P). Its resistance can be varied in 256 steps from 0 to 5 kΩ, with a wiper resistance of approximately 75 Ω. The potentiometer is connected in series with R10 and R13 at the two ends. The base resistance values can be selected through jumpers by connecting R14 and R15. The resistance can be varied in accordance with the selected waveshape by providing the appropriate sequence of digital control words to the digital potentiometer. The relation between the values of resistors in the simulator circuit in Fig. 3.3, in the schematic in Fig. 3.2, and those in the model in Fig. 3.1 are as the following,

$$\begin{aligned} R_{s1} + R_{e1} &= R_a \\ &= R_6 \end{aligned} \tag{3.11}$$

$$\begin{aligned} R_{e2} &= R_b \\ &= R_7 \end{aligned} \tag{3.12}$$

$$\begin{aligned} R_{e3} &= R_c \\ &= R_8 \end{aligned} \tag{3.13}$$

$$\begin{aligned} R_{s2} + R_{e4} &= R_d \\ &= R_9 \end{aligned} \tag{3.14}$$

$$\begin{aligned} R_0 \,||\, R_s &= R_v \,||\, \Big(2\big(R_x \,||\, R_y\big)\Big) \\ &= \big(R_{10} + R_{WB} + R_{13}\big) ||\, R_{14} ||\, R_{15} ||\, \Big(\big(R_2 \,||\, R_4\big) + \big(R_3 \,||\, R_5\big)\Big) \end{aligned} \tag{3.15}$$

where R_{WB} = resistance set by the digital potentiometer IC5, and the values R_{14} and R_{15} depend on the jumper settings.

The voltage, representing internal bioelectric sources may be generated using D/A converter. In order to reduce the number of types of components in the circuit, we have used digital potentiometers. The selected waveform is generated by digital potentiometer IC2. Its peak-to-peak amplitude is controlled by the digital potentiometer IC3. With the use of the two digital potentiometers, the same number of quantization steps can be provided in the waveform for different peak-to-peak amplitudes. The common and difference mode voltages in the simulator circuit in Fig. 3.3 in terms of the voltages E_{x1} and E_{x2} are as the following,

$$V_c + V_d / 2 = \Big(R_2^{'} / \big(R_2^{'} + R_4\big)\Big) E_{x1} \tag{3.16}$$

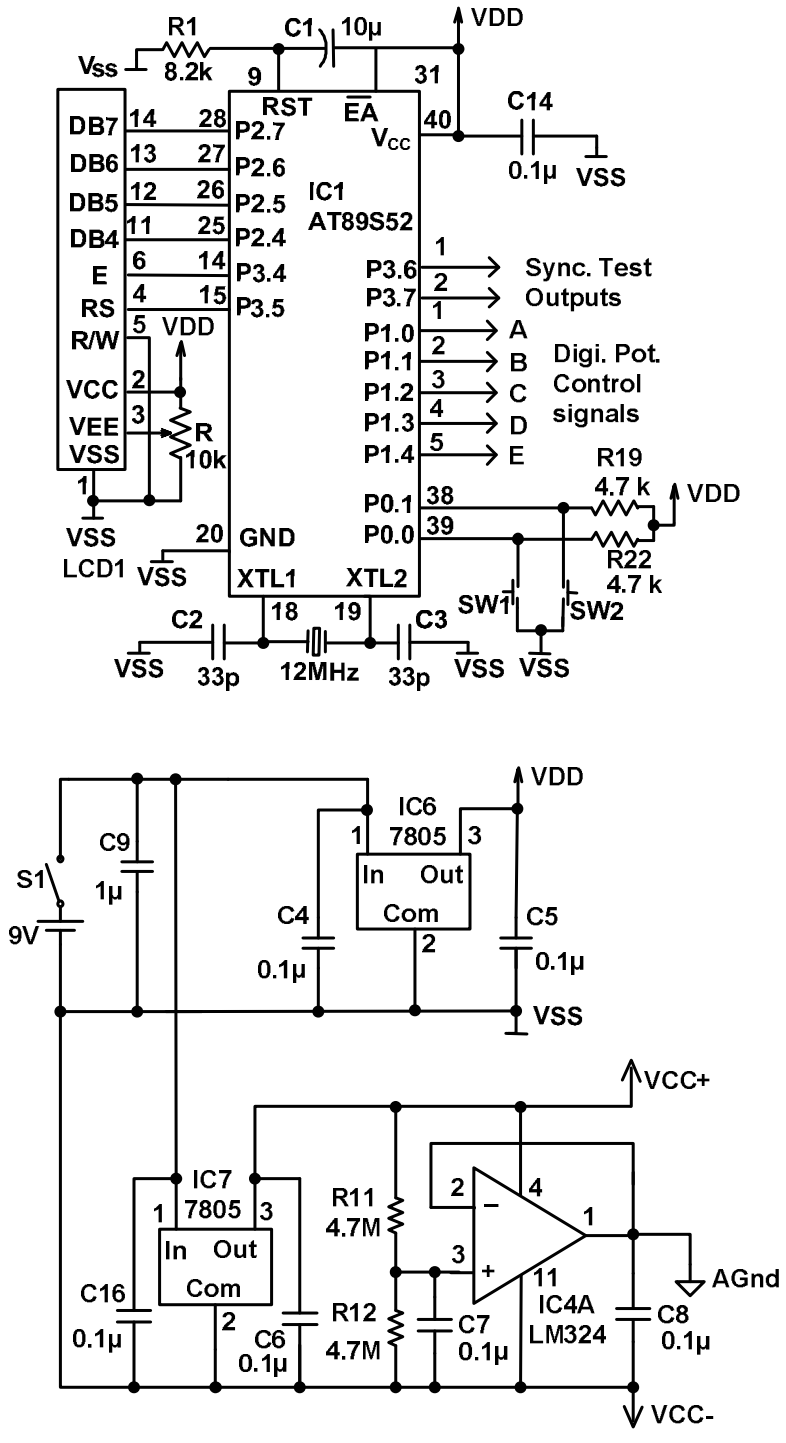

Fig. 3.4 The controller and power supply circuit

$$V_c - V_d / 2 = \left(R_3^{'} / \left(R_3^{'} + R_5 \right) \right) E_{x2} \tag{3.17}$$

where $R_2^{'} = R_2 \,||\, \left(\left(R_3 \,||\, R_5 \right) + \left(\left(R_{10} + R_{WB} + R_{13} \right) || \, R_{14} \,||\, R_{15} \right) \right)$

$R_3^{'} = R_3 \,||\, \left(\left(R_2 \,||\, R_4 \right) + \left(\left(R_{10} + R_{WB} + R_{13} \right) || \, R_{14} \,||\, R_{15} \right) \right)$

A polarity controlled unity gain amplifier, realized using op amp IC4B and analog switch IC8 is used to control the phase relationship between the voltages E_{x1} and E_{x2}. The port pin P3.3 of the microcontroller is used to select the common or difference mode voltages.

The controller and the power supply circuit is shown in Fig. 3.4. The microcontroller IC1 (AT 89S52) is used as the controller of the hardware. The three digital potentiometers are controlled via SPI bus. The various wave shapes like sinusoidal, square, and a typical ECG have been realized using different lookup tables in the microcontroller's memory. The synchronization test outputs are provided on port pins P3.6 and P3.7 of the microcontroller for testing synchronization of the outputs of the ECG amplifier and the impedance detector. The LCD display LCD1 and the two soft keys SW1 and SW2 provide the user interface.

The circuit is powered by a single 9 V supply, with two fixed voltage regulators (IC6, IC7) for the digital and the analog parts of the circuit. The simulator analog ground is at $V_{DD}/2$ with respect to V_{SS} and floating with respect to the earth ground. For testing the rejection of external common mode interference by the impedance detector, the common mode interference can be externally applied between the terminal marked E_P and the circuit ground of the impedance cardiograph.

The various parameters for simulation, type of waveshape (square, sine), the ECG mode (common, differential), frequency (1 – 250 Hz), the amplitude of ECG voltages (0 – 100 mV), and variation in the resistance (0.1 – 1.2 %) are selected using LCD and the two soft keys. The simulator can be used for simultaneous testing of the impedance detector and ECG part of the impedance cardiograph, and also for estimating the effect of external common mode interference on the measurements.

3.4 Software

The microcontroller is programmed to perform following tasks

1. Scan the keys
2. Update the display

3. Keep track of the time and update wiper code of the two digital potentiometers to output the ECG signal of the set frequency and the amplitude, and also update wiper code of the digital potentiometer used in resistance variation

The microcontroller program is written in assembly language. It is divided into two parts: (i) the main program and (ii) the interrupt service routine (ISR) to update wiper codes of the three digital potentiometers

The main program starts by initializing the display, various assigned variables, and timers. Subsequently it periodically scans the input keys, and updates the variables and the display accordingly. Before the generation of the waveform starts, the user can select the basal resistance. For this purpose, Timer 0 of the microcontroller is programmed in Mode 1 to generate an interrupt after a delay of 60 ms. It is used to set a time interval of 1 sec for selection of the basal resistance, using keys and display. After the lapse of this time, the main program goes to the waveform generation mode, with continuous scanning of the input keys and display updating.

The ISR is called periodically by a timer interrupt and it updates the wiper codes of the three digital potentiometers. With 12 MHz clock, the minimum time required for the ISR was calculated to be about 250 μs (and also verified using a CRO). In the ISR, after updating the wiper codes, Timer-1 is programmed in Mode-1 to give an interrupt after a delay of 350 μs, leaving a buffer interval of 100 μs for the main program. It may be noted that the execution time of the single loop of the ISR and the main program limits the update rate of the wiper codes and hence the frequency of the waveforms. The ISR is written from vector address location (001bH) of the Timer1.

The algorithm of the main program and the critical routine are given as follows.

Main program

Step1: Initialize the variables assigned for the various parameters of ECG and resistance variation: ECG mode, type, frequency, the amplitude of ECG voltages, and variation in the resistance.

Step 2: Load timer registers with appropriate count.

Step 3: Initialize LCD display.

Step 4: Introduce a software delay of about 20 ms

Step 5: Input the keys

Step 6: If key press is valid, update the variables stack assigned for the various parameters Go to step 4.

ISR

Step 1: Load Timer 1 for a timer interrupt after a delay of about 350 μs.

Step 2: Select the lookup tables according to the variables stack.

Step 3: Read the codes from selected addresses and update digital potentiometers used for ECG generation and resistance variation.

Step 4: Return to the main program.

Chapter 4
IMPEDANCE CARDIOGRAPHY HARDWARE

4.1 Introduction

An impedance cardiograph generally consists of an impedance sensor, an ECG extraction circuit, and a differentiator [7]-[16]. The impedance is sensed by generating an excitation signal in the frequency range of 50 kHz – 500 kHz. A low amplitude (< 5 mA) output current from a voltage-to-current converter is injected in the thorax region using a pair of electrodes. The resulting amplitude modulated voltage across the voltage sensing electrodes is amplified using a voltage sense amplifier. The output voltage is demodulated to get the bioimpedance signal. The ICG signal is obtained by differentiating the bioimpedance signal.

Hardware developed earlier in our laboratory [13]-[16] (SPI Lab, EE Dept., IIT Bombay) are based on a circuit reported by Qu *et. al.* [7]. The circuit includes a current source, an impedance sensor, a differentiator, an automatic balancing circuit and an ECG extractor. The current source consists of a Wein bridge oscillator and a voltage-to-current converter. The output of the oscillator is stabilized by a FET based circuit. An inverting amplifier based V-to-I converter is used, with one end of the load connected to the op amp output and the other terminal connected to the virtual ground at the inverting input of the op amp. The impedance sensor consists of a highpass filter, an ICG amplifier, and a demodulator. The highpass filter with corner frequency of about 16 kHz rejects the ECG and power-line interference. To amplify the difference between the voltages sensed by the electrodes three-op amp instrumentation amplifier is used. The demodulator consists of a diode based (1N4148) precision rectifier and a lowpass filter with corner frequency of about 28 Hz. A first order lowpass filter with corner frequency of about 0.72 Hz is used to get a basal impedance signal. The output of the demodulator is also given to an automatic balancing circuit followed with a differentiator. A successive approximation technique is used in the automatic balancing circuit. The differentiator is used to get *dz/dt* signal. The ECG extractor has an op amp based difference amplifier with a lowpass filter with corner frequency of about 72 Hz, followed by a highpass filter with corner frequency of about 1.1 Hz. The total gain is around 270. This is followed by a differentiator for removing the offset drift.

Naidu [15] modified the circuit for Wein bridge oscillator for improving the amplitude stability. Sarvaiya [17] used the signal generator IC MAX8038 for the impedance glottography hardware. He found better amplitude stability in comparison with earlier circuits. Venkatachalam [16] used Wein bridge oscillator with introduction of the amplitude stabilization loop which includes a peak detector and an error amplifier. The transformer-less balanced current source was reported by Kuriakose [13]. It was used by Manigandan [14]. Venkatachalam [16] and Sarvaiya [17] used transformer based balanced circuit to avoid effect of the stray current and the external pick-up. Venkatachalam [16] used instrumentation amplifier IC INA128 to replace the three op amp difference amplifier [14] in the impedance sensor and the ECG extraction circuit. Earlier designs [13]-[16] used a diode based precision full-wave rectifier followed by a lowpass filter circuit for demodulation. After testing various demodulator circuits for linearity, Sarvaiya [17] used full-wave rectifier using voltage clamp amplifier IC AD8037. Naidu [15] used vector lock-in amplifier for synchronous detection of in-phase and quadrature phase by using Bubba oscillator. Pandey *et. al.* [22], [23] reported a tracking based baseline restoration for acquisition of bio signals. The circuit was based on amplitude tracking for fast removal of baseline drift.

After studying the earlier designs, the following circuit ideas for the current source and the demodulator are introduced.

1. A programmable waveform generator using a direct digital synthesizer (DDS) chip can be used to generate sinusoidal signal of the desired frequency. Two such synthesizers can be used for obtaining synchronized sinusoidal outputs with a settable phase shift. One of these outputs can be used for the voltage-to-current converter and the other one as reference signal for synchronous demodulation. A microcontroller can be used to set the frequency and the phase shift.
2. To provide the flexibility of using a variable excitation frequency and current level, it is proposed to use a control circuit with a microcontroller, input keys, and LCD. All the controls to the DDS chips and current level control circuit will be from microcontroller port pins. The parameters can also be controlled through a serial interface to the microcontroller. This will avoid any strays due to routing the signal wires to the control panel.
3. The inverting amplifier based current source and the current source with balanced voltage output terminals have one end of the load terminal as op amp inverting input terminal. It causes instability due to stray. To solve this problem, it is proposed to use modified Howland current source, in which one of the load terminal is grounded and hence instability problem is reduced. To avoid the large common mode problem, it is proposed to use a transformer, so that the two current terminals have high impedance with respect to the circuit ground.

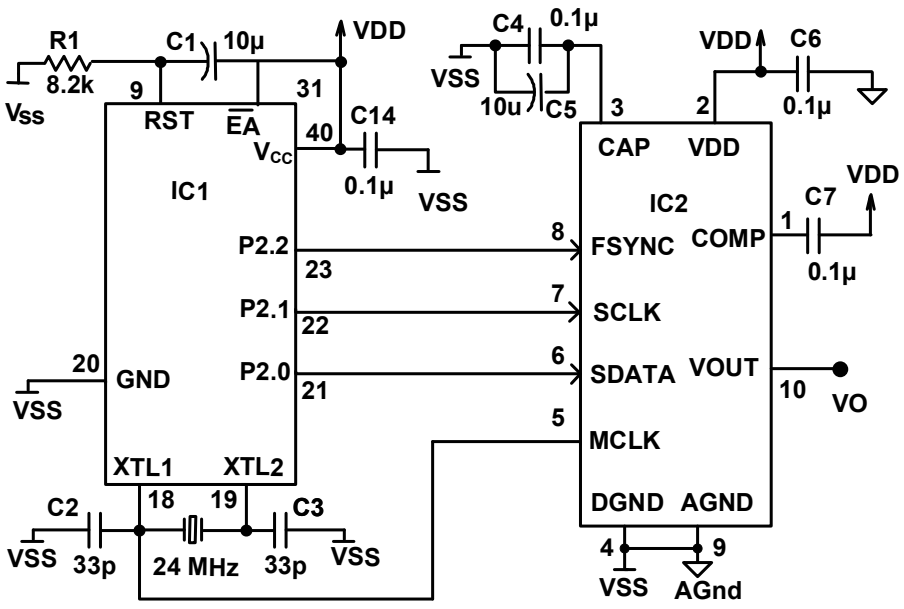

Fig. 4.1 The programmable source using DDS AD9833 [34]

4. The demodulator should provide noise rejection, carrier ripple rejection, and high sensitivity. We propose to use a slicing amplifier with a sample-and-hold circuit for the synchronous detection of the bioimpedance signal.

4.2 Excitation source

The sinusoidal signal can be generated digitally using sine lookup table which can be read at appropriate time for the desired output frequency and the analog output obtained using a digital-to-analog converter. The method permits precise and convenient control of the frequency and good amplitude stability. A number of direct digital synthesizer (DDS) chips can be used for this purpose.

a) The programmable waveform generator

The DDS IC's AD9833 and AD9834 can generate sinusoidal, square, and triangular signals [34], [35]. They have inbuilt memory for the waveform and a digital-to-analog converter with 28-bit frequency control and 12-bit phase control registers. The frequency and the phase of the output can be controlled using synchronous serial interface. The output frequency and the phase are given as,

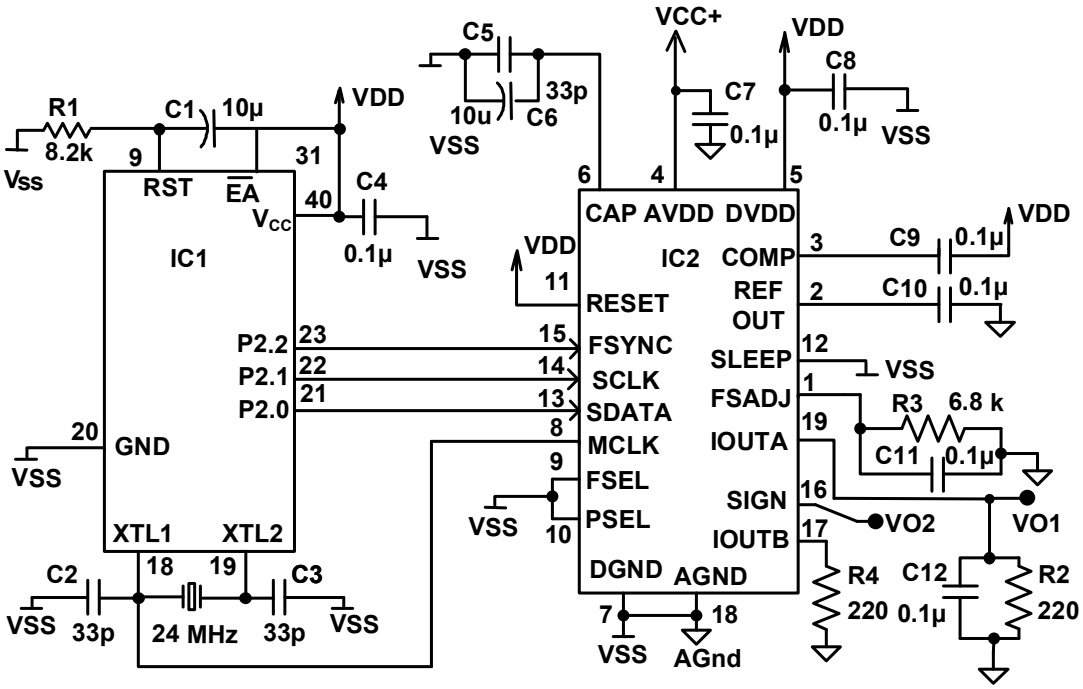

Fig. 4.2 The programmable source using DDS AD9834 [35]

$$f_{out} = \frac{f_{MCLK}}{2^{28}} N_{FREQREG} \tag{4.1}$$

$$\theta_{out} = \frac{2\pi}{2^{12}} N_{PHASEREG} \tag{4.2}$$

where N_{FREQREG} and N_{FREQREG} are the counts loaded in the frequency and the phase registers of the DDS.

The IC AD9833 was tested to generate a sine wave. As shown in Fig. 4.1, it is controlled and programmed by the microcontroller IC AT89S52 [32] via synchronous serial interface. The port pins P2.0, P2.1, and P2.2 are connected to the SDATA, the SCLK, and the FSYNC of the DDS. The serial interface can operate with 40 MHz clock rate. With clock f_c, the DDS can generate a sine wave of frequency of up to $f_c/2$. The IC AD9834 can work with up to 75 MHz clock. The reset, the phase register selection, and the frequency register can be selected either by software or by hardware control, as shown in Fig. 4.2. For the AD9833, the controls are only by software. The IC AD9833 has the voltage output while the IC AD9834 has current output. Both the chips use 2.5 V for powering the digital section of the internal circuit. In case of AD9833, the IC has a single supply terminal. The digital supply is obtained using an internal regulator. The AD9834 also has an internal regulator for its digital section, but the IC has separate analog and digital supply pins. Hence AD9834

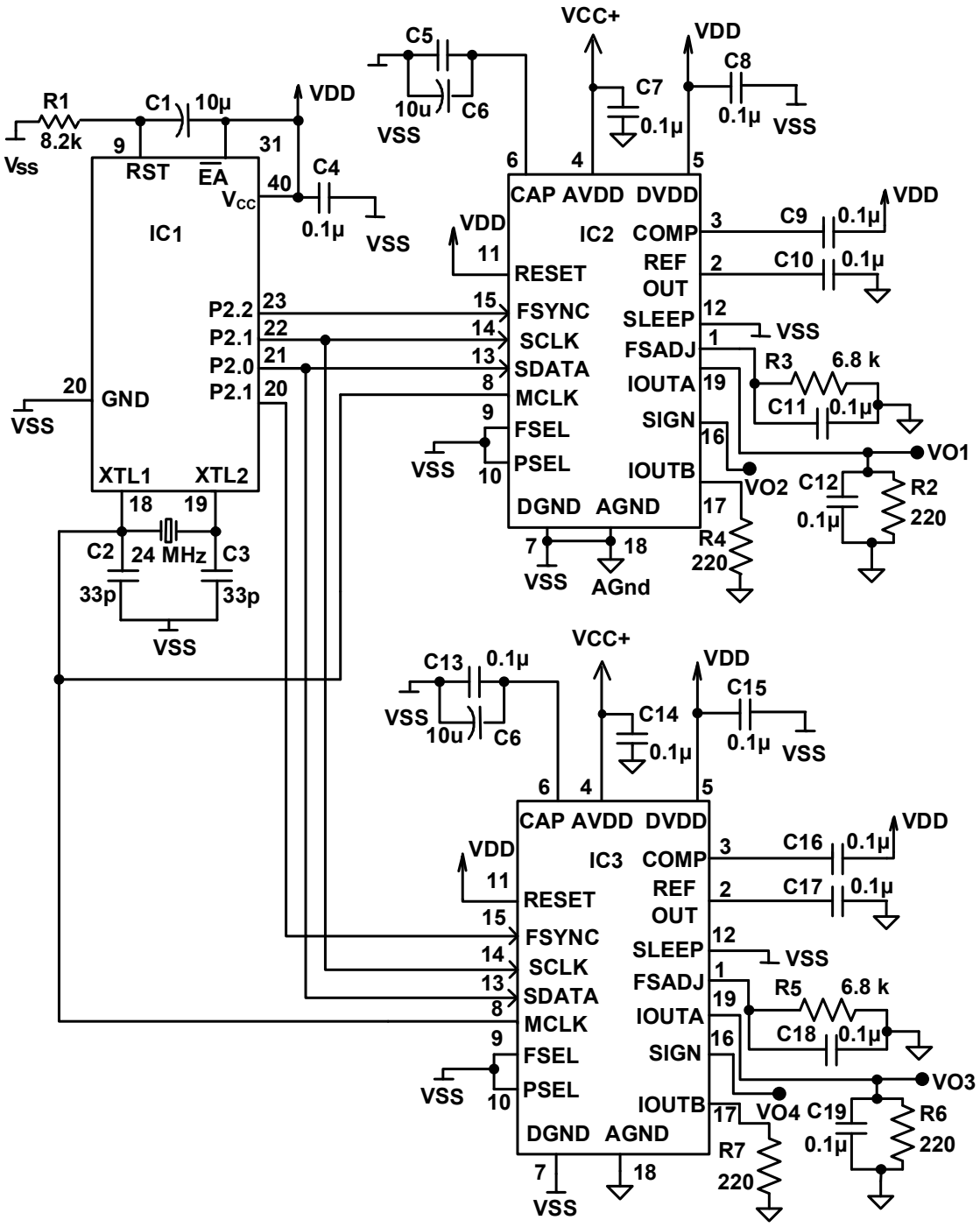

Fig. 4.3 Programmable source using AD9834 for outputs with a settable phase difference

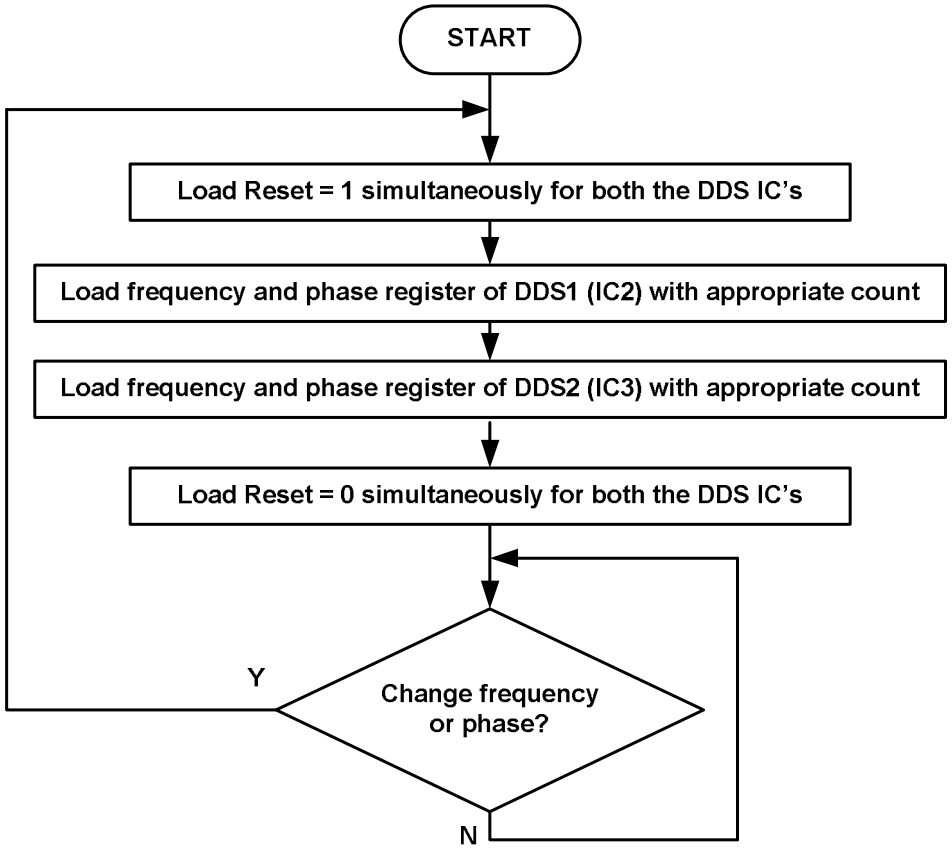

Fig. 4.4 Flowchart of the microcontroller program for DDS synchronization for phase shifted outputs

provides a separation of power supply for the analog and digital circuitry. In case of either of the two IC's, two DDS chips can be synchronized with a programmable phase difference between the outputs. The instant of synchronization can be controlled by software in AD9833. In AD9834, it can be controlled by software or by hardware. We have opted to use IC AD9834 primarily because of power supply separation.

b Synchronizing two DDS.

The output of the two DDS ICs can be synchronized using the circuit as shown in Fig. 4.3. One out of the two DDS outputs can be used as the input to the voltage-to-current converter and the other can be used as the reference for the synchronous demodulation. Both ICs operates on the same clock signal from the oscillator output. The serial data and the serial clock lines are also common. Two separate control signals are connected to the FSYNC pins of the two ICs for permitting transfer of same or different data to the two.

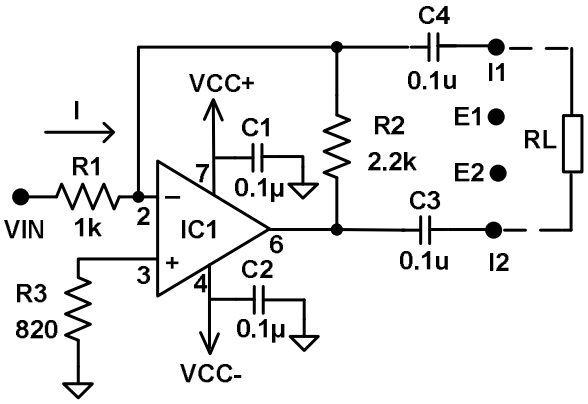

Fig. 4.5 V-to-I converter based on inverting amplifier circuit [16], [27] (IC1: LF 356)

The flowchart for the programming of the two DDS IC's is given in Fig. 4.4. The frequency registers of the two ICs are loaded with the same count to get the output frequency in the range from 20 to 500 kHz. The phase register of IC2 is loaded with the count to get 0° phase shift while the phase register of IC3 is loaded with the count to get the desired phase shift with respect to the other DDS. Both DDS outputs can be synchronized by issuing the simultaneous reset command under the software control. The sinusoidal output of the DDS IC2 is connected to the current source while the "signbit" output of the DDS IC3 is used to generate the waveform for the synchronous demodulation.

4.3 Voltage-to-current converter

A voltage controlled current source can be used for injecting the low amplitude (< 5 mA) current in the thorax. Several realizations of the voltage-to-current converter were examined.

a) Inverting amplifier with load in feedback (floating load converter)

For the circuit shown in Fig. 4.5, the current injected using electrodes I1 and I2 through dc blocking capacitor is given by,

$$I = \frac{V_{IN}}{R_1} \tag{4.3}$$

The blocking capacitors C4 and C3 are used to avoid any DC current through the electrodes. The resistor R2 limits the DC gain and prevents op amp from going into saturation due to loose electrodes contacts. As one of the electrodes of the circuit is at virtual ground, the terminal voltages are unbalanced with respect to ground. Hence there is possibility of the

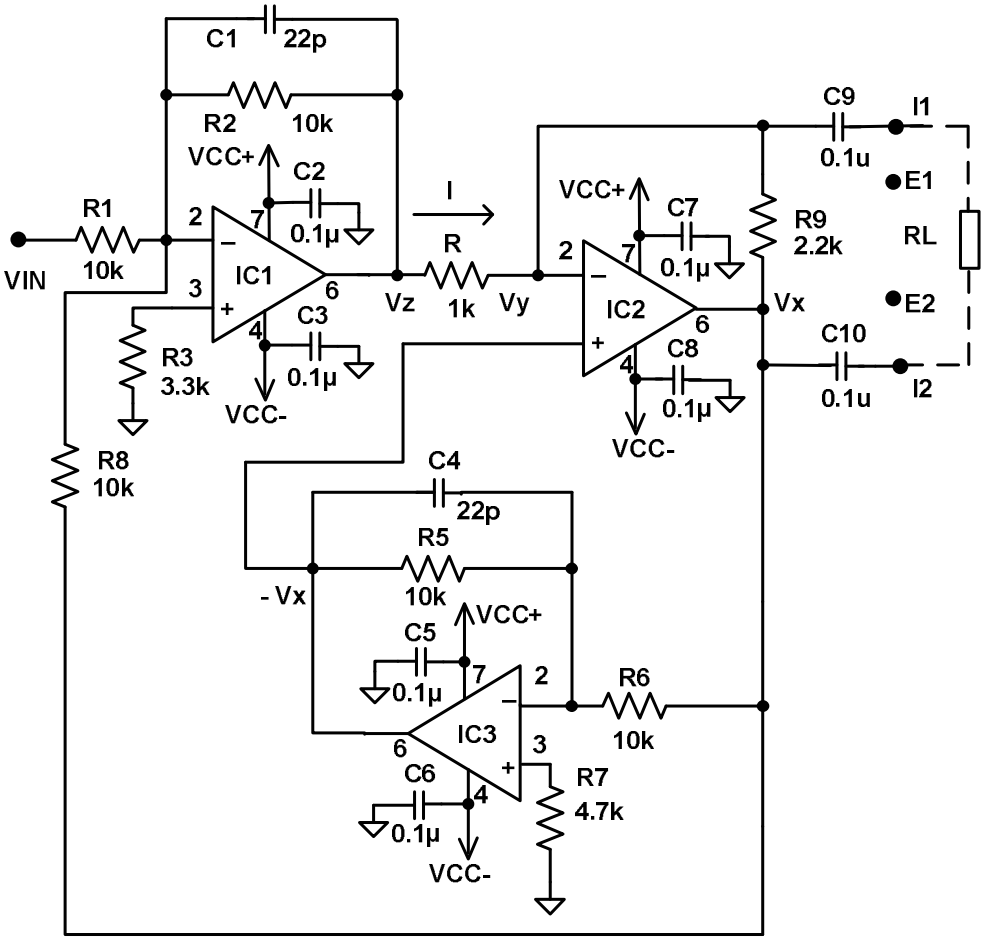

Fig. 4.6 Balanced current source [13], [14]. (IC1 - IC3: LF 356)

stray current and the common mode pick-ups. A transformer based electrically isolated symmetrical current source can be used to avoid the effects of the stray current and the common mode pick-ups [16] [17] [24]. The stray capacitances at the op amp inverting terminal, due to connection of one of the electrode, often leads to instability.

b) Transformerless balanced current source

Kuriakose [13] and Manigandan [14] reported a transformerless balanced current source. The terminal voltages are balanced with respect to the ground. This reduces the stray current into the thorax. For the circuit shown in Fig. 4.6 the terminal voltages V_Y and V_X are as following,

$R_1 = R_2 = R_5 = R_6 = R_8 = 10$ k

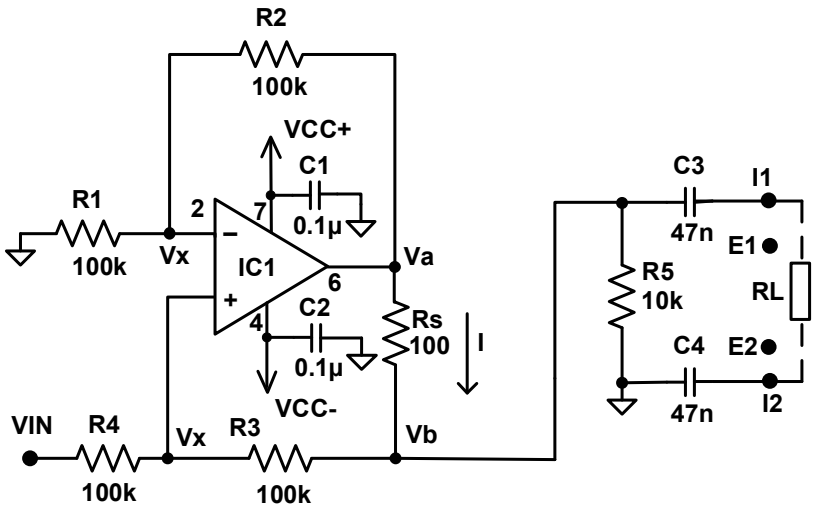

Fig. 4.7 V-to-I converter based on modified Howland current source [25], [26], [27]. (IC1: LF 356)

$$V_z = -V_{IN} - V_X \tag{4.4}$$

$$V_Y = -V_X \tag{4.5}$$

Applying KCL at node Y

$$\frac{V_Y - V_Z}{R} + \frac{V_Y - V_X}{R_L} = 0 \tag{4.6}$$

From Eqs. 4.4, 4.5, and 4.6

$$V_X = 0.5\frac{R_L}{R}V_{IN} \tag{4.7}$$

$$V_Y = -0.5\frac{R_L}{R}V_{IN} \tag{4.8}$$

The load current is given as,

$$I = \frac{V_Z - V_Y}{R} = -\frac{V_{IN}}{R} \tag{4.9}$$

From Eq. 4.7, and Eq. 4.8, the voltages V_Y and V_X are equal in magnitude and opposite in phase. Thus terminal voltages are balanced with respect to the ground. It may be noted that as in the previous circuit load terminal is connected to the inverting terminal of the op amp.

(c) Modified Howland current source

In the modified Howland current source, one end of the load is connected to the circuit ground [25], [26], [27]. For the circuit shown in Fig. 4.7, the voltage across the resistor R_s senses the load current and feedback is used to stabilize the current.

$$V_a - V_b = I\, R_s$$

$$\frac{V_{in} - V_x}{R_4} = \frac{V_x - V_b}{R_3}$$

$$V_x = V_a \frac{R_1}{R_1 + R_2}$$

With $R_1 = R_2$ and $R_3 = R_4$, we get

$$V_x = \frac{V_{in} + V_b}{2} = \frac{V_a}{2}$$

or $V_a - V_b = V_{in}$ (4.10)

Therefore the load current is given as,

$$I_L \approx I = \frac{V_{in}}{R_s} \quad (4.11)$$

The advantage of the modified Howland current source is that its the output impedance depends on the ratio of the resistances R_1, R_2, R_3, and R_4, while in case of the inverting amplifier based V-to-I converter, output impedance is a function of the open loop gain of the op amp [27]. In case of the circuits in Fig. 4.5 and Fig. 4.6, one of the load terminals (one of the current injecting electrodes) is connected to the inverting terminal of the op amp, and stray capacitances at the op amp input often lead to instability. This problem is avoided in the modified Howland current source for V-to-I converter.

The electrostatic pickup on the current carrying cables can be reduced by shielding [24], but it causes signal attenuation. So instead of grounding the shield it can be connected to the buffered transmitting voltage signal. By this arrangement both the core and the shield are at the same potential with zero current flow in between. For increasing the impedance between the current electrodes and circuit ground, a high frequency transformer may be used for connecting the current electrodes to the V-to-I converter.

4.4 Difference amplifier

The difference between the voltages, sensed by the voltage sensing electrodes is amplified as shown in Fig. 4.8. It is decided to use INA128 instrumentation amplifier for the difference amplifier as used by the earlier

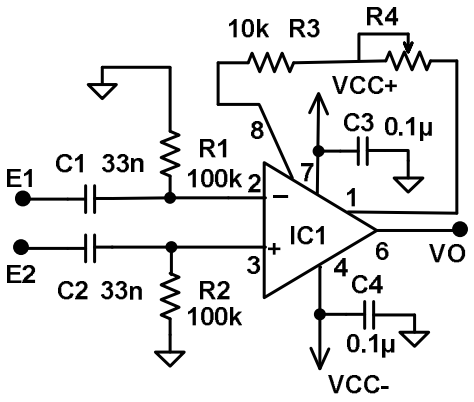

Fig. 4.8 Difference amplifier using INA 128

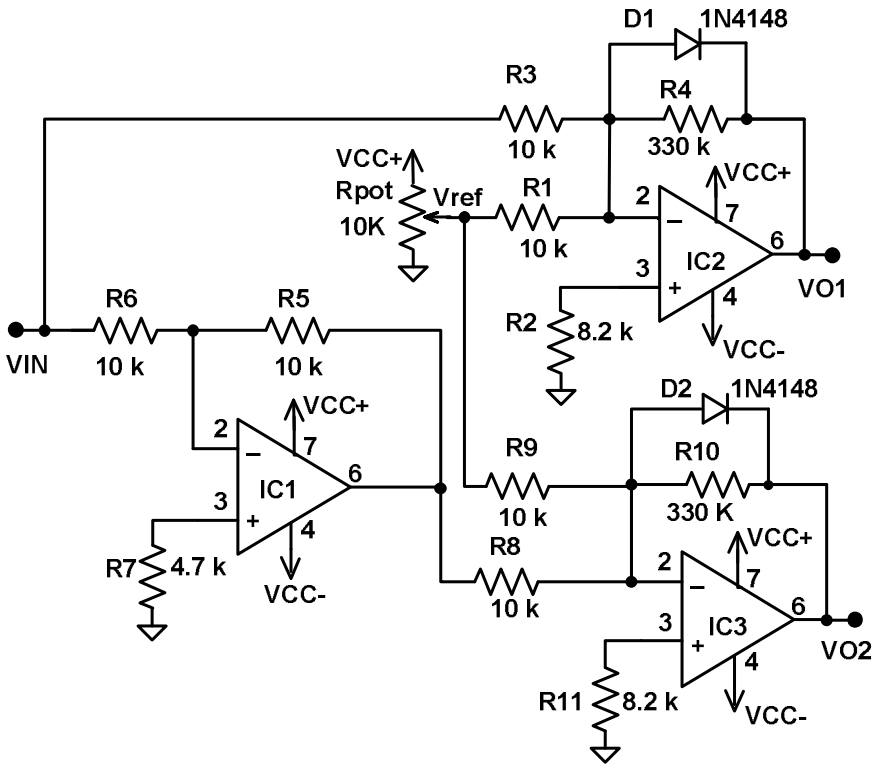

Fig. 4.9 Diode based slicing amplifier (IC1 - IC3: LF 356)

designs [16], [17]. The IC provides a gain of 10 up to700 kHz with a typical common mode rejection ratio of 106 dB [36].

4.5 Demodulator

The output of the difference amplifier needs to be demodulated to get the impedance signal. It can be carried out using a precision rectifier followed by a lowpass filter [13]-[16]. However it has been observed that a diode based rectifier circuit introduces distortion at higher frequencies. After investigating several circuits, Sarvaiya [17] used a precision rectifier based on voltage clamp amplifier IC AD8037 and the circuit gives acceptable operation up to 500 kHz. For removing carrier ripple, a lowpass filter is used, but this filter introduces phase distortion. One of the serious difficulties in the demodulator is that the modulation index is very low (0.2 – 2%) and hence the demodulator output can be amplified only after removal of the dc component. In the design of a laryngograph (an instrument for monitoring the movement of vocal cords by sensing the variation in the impedance across

the thyroid cartilage), Fourcin [28] introduced the use of a slicing amplifier for improving the sensitivity of the demodulator. The top of the amplitude modulated signal can be sliced up to the level of modulation depth followed by an appropriate gain. The slicing amplification increases the demodulator sensitivity, but carrier ripple in the output is increased, requiring a higher order lowpass filter which causes even larger phase distortion. Sampling near the peak of the carrier frequency can be used to detect the bioimpedance signal. Sampling the top of the carrier in short time interval and holding the value till the next peak almost eliminates the carrier ripple. Two circuits are designed to implement the concept.

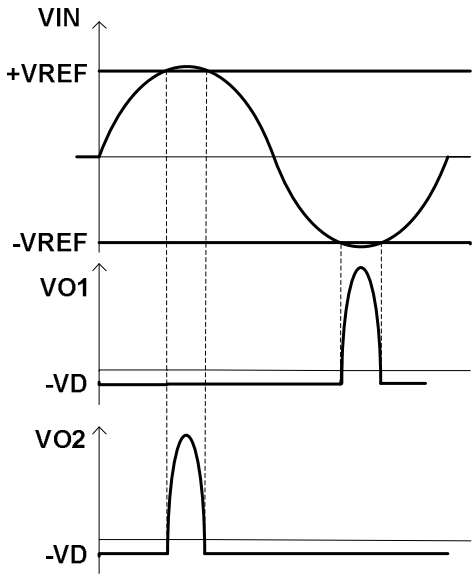

Fig. 4.10 Output waveforms VO1 and VO2 of the of diode based slicing amplifier

a) The diode based slicing amplifier

The positive and negative peaks of the input signal are clipped by subtracting the reference voltage set using a potentiometer. In the circuit shown in Fig. 4.9,

$R_1 = R_2 = R_8 = R_9$, $R_{10} = R_4$, $R_5 = R_6$

The output voltage V_{O1} is amplified version of the input as long as the output is positive as shown in Fig. 4.10. If the input is such that output goes negative, it is clamped by D1.

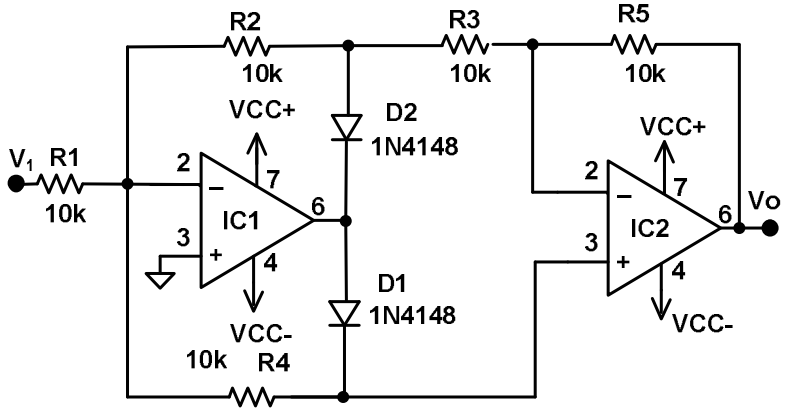

Fig. 4.11 Precision full-wave rectifier (IC1,IC2: LF356) [6], [13]-[16]

Thus it slices negative value below $-V_{ref}$ and amplifies them. The output V_{O1} is given as,

$$V_{O1} = -\frac{R_4}{R_3}\left(V_{in} + V_{ref}\right),$$

If $-V_{in} > V_{ref}$ (4.12)

$V_{O1} = -V_D$, If $-V_{in} < V_{ref}$ (4.13)

Similarly, the output V_{O2} is given as,

$$V_{O2} = \frac{R_4}{R_3}\left(V_{in} - V_{ref}\right),$$

If $V_{in} > V_{ref}$. (4.14)

$V_{O2} = -V_D$, If $V_{in} < V_{ref}$. (4.15)

The gain can be set around 200 with appropriate selection of the resistors.

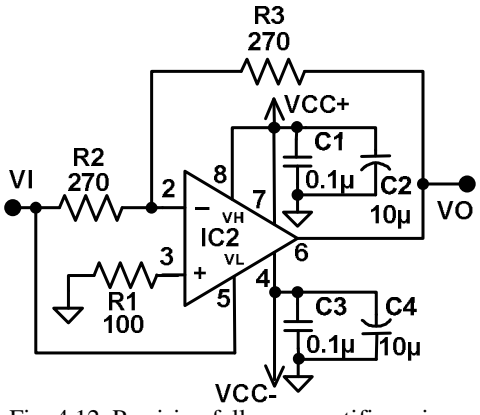

Fig. 4.12 Precision full-wave rectifier using voltage clamp amplifier IC AD8037

b) Slicing amplifier using voltage clamp amplifier

The diode based slicing amplifier introduces nonlinear distortion at higher frequencies. Earlier, Sarvaiya [17] used a full wave rectifier using the voltage clamping amplifier IC AD8037 [33]. The circuit works satisfactory up to 500 kHz. As shown in Fig. 4.12, the

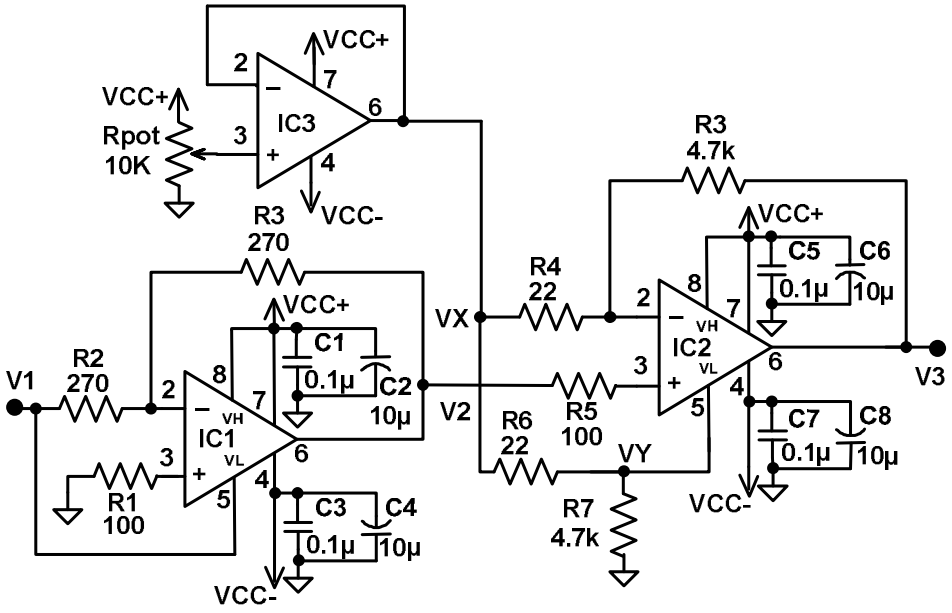

Fig. 4.13 Slicing amplifier using voltage clamp amplifier AD8037
(IC1: LF356, IC2 and IC3: AD8037)

voltage clamp input V_L is connected to the input signal V_I and the input V_H is connected to V_{CC} to get the full wave rectified output. The detailed working of the IC is included in appendix A. The output of the full-wave rectifier can be clipped by setting the lower clamp level to the reference voltage and thus it can be used for realizing a slicing amplifier. The full wave rectifier slicing amplifier circuit using two AD8037's is shown in Fig. 4.13. IC1 is used for full- wave rectification, with its V_L connected to V_I. IC2 provides slicing amplification for the full wave rectified signal V_2, by setting the lower clamp level V_L to the reference voltage V_Y. The sliced peak of the rectified output can be amplified with the gain of around 200 or more. The reference V_Y is obtained from V_X as,

$$V_Y = \frac{R_7}{R_7 + R_6} V_X$$

When $V_2 > V_Y$, the output is given as

$$V_3 = V_2\left(1 + \frac{R_3}{R_4}\right) - \frac{R_3}{R_4} V_X \tag{4.16}$$

With $R_7 = R_3$ and $R_6 = R_4$, Eq. 4.16 can be written as,

$$V_3 = (V_2 - V_Y)\left(1 + \frac{R_3}{R_4}\right) \tag{4.17}$$

for $V_2 < V_Y$, the output is given as

$$V_3 = V_Y\left(1 + \frac{R_3}{R_4}\right) - \frac{R_3}{R_4} V_X$$

$$= 0 \tag{4.18}$$

Thus, we see that for $V_I > V_Y$, the output voltage is the difference between input and reference voltage set using the potentiometer, and the difference voltage is amplified with the gain set by the ratio R_3/R_4. For $V_I < V_Y$, the output is zero. Thus the circuit works as a full-wave rectifier and slicing amplifier with a gain of $1+R_3/R_4$.

c) Sample-and-hold circuit

Slicing amplifier increases the demodulator sensitivity, but it increases the carrier ripple in the output. Use of a sample-and-hold circuit, for sampling the signal near the peak and holding the value until the next peak can be used for eliminating the carrier ripple. Use of the sampling pulses in synchronism with the peak of the carrier results in a synchronous demodulation [29], [30] and hence rejection of noise. The output of the slicing amplifier is sampled near the peak of the carrier frequency. The sample-and-hold circuit is designed

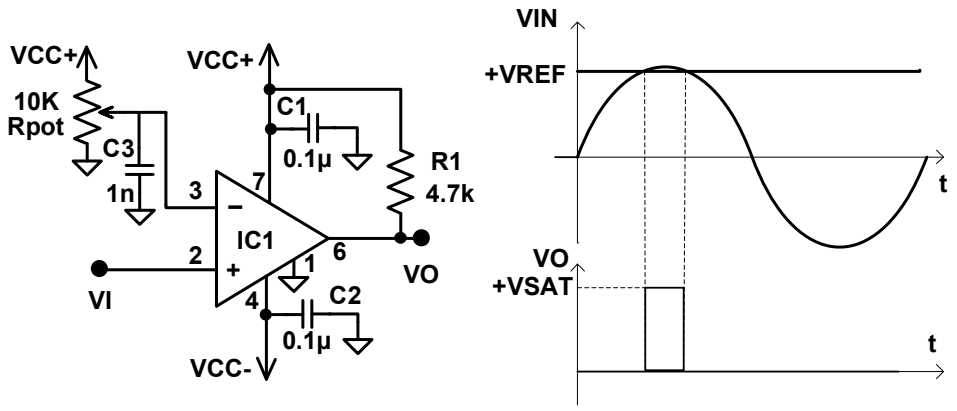

Fig. 4.14 Sampling pulse generator at the positive peak using comparator IC LM311

using IC HA5351. The IC features an acquisition time of 70 ns with a unity gain bandwidth of 40 MHz [37]. For unity gain configuration, no external component is required.

d) Sampling pulse generation circuit

To get the narrow sampling pulses near the peak of the carrier, various circuits were examined.

i) Sampling pulse generation at the positive peak: The top of the carrier can be compared with the fixed reference voltage as shown in Fig. 4.14. The pulse width can be varied by varying the reference voltage. As the slope of the sinusoidal signal is low near the peak, a significant jitter is found in the pulse edges.

ii) Sampling pulse generation at zero crossings: The reference carrier signal is compared with the positive and negative reference voltages set near the ground level, using the two comparator circuit as shown in Fig. 4.15. The open collector outputs of the two comparators are tied together and connected to the pull-up resistor. In the interval when carrier signal is between the two reference voltages, the output pulse is generated. The pulse width can be varied by setting the reference voltages using potentiometers R5 and R6. By varying the potentiometer R2, pulses can be shifted with desired time. The response time of the comparator IC LM311 is of 200 ns which limits the performance of the circuit at higher frequencies. Other limitation is that the comparator introduces noise of around 100 mV in the circuit during output switching.

iii) Sampling pulse generation using monostable multivibrator IC SN74221: The monostable multivibrator IC SN74221 [38] can be used to generate short duration pulse of 70 ns. It has two in-built multivibrators. Each multivibrator has positive transition (B) and negative transition (A) trigger inputs. The "signbit" output of the DDS IC AD9834 is

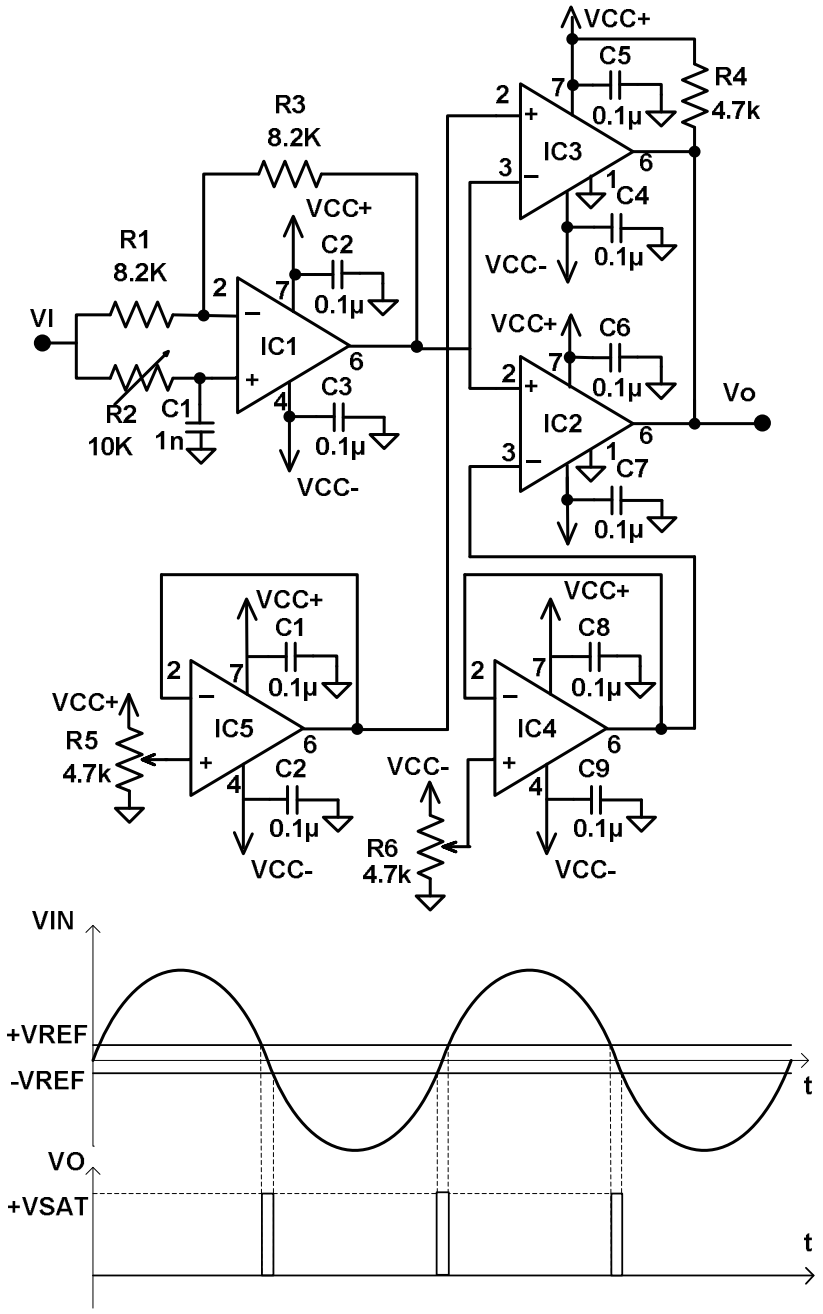

Fig. 4.15 Sampling pulse generation at zero crossing, using IC1, IC4, IC5: LF356, IC2 and IC3:LM311

Table 4.1 Function table of IC SN74221

Multivibrator	CLR	A	B
1	H	↓	H
2	H	L	↑

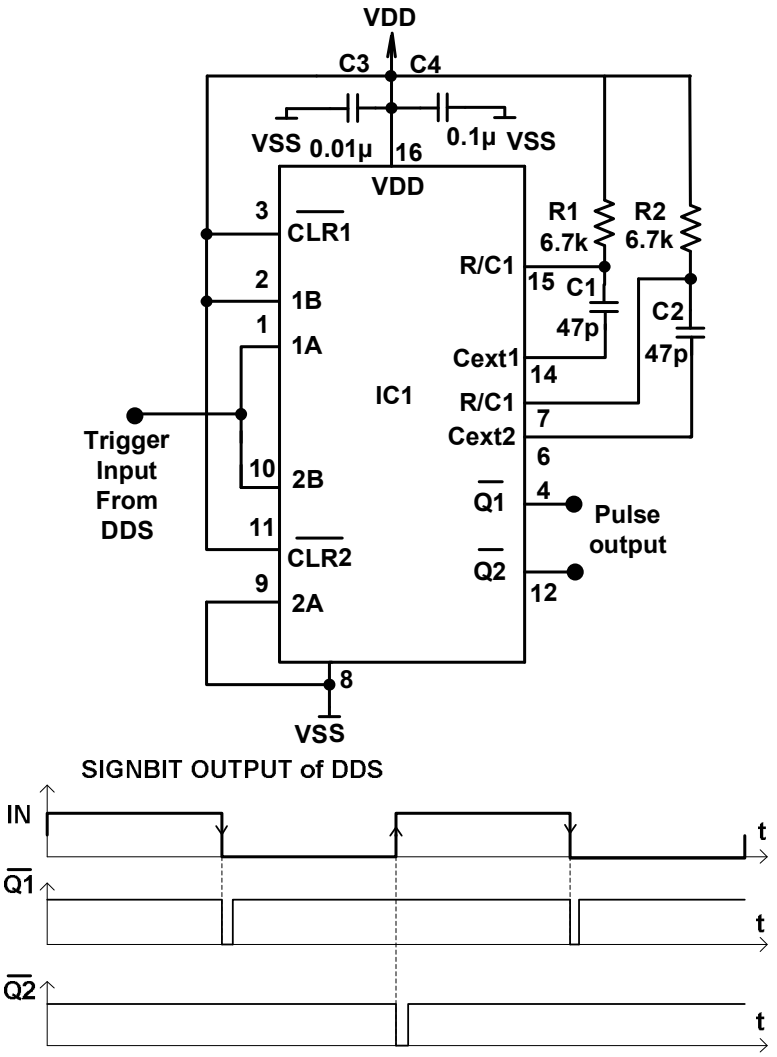

Fig. 4.16 Monostable multivibrator using IC1: SN74221 [38]

connected to one of the trigger inputs of the multivibrators as shown in Fig. 4.16. The other input is connected either to the ground or to the VDD according to Table 4.1 Thus pulses are generated with reference to the rising and the falling edges of the "signbit" output from DDS. The pulse width for each multivibrator is set by selecting timing components R1, R2, C1, and C2

4.6 Two channel slicing and sampling

It is found that the alternating peaks of the output of the slicing amplifier are generally of unequal amplitudes. Sampling and holding the unequal peaks introduces ripple in the output.

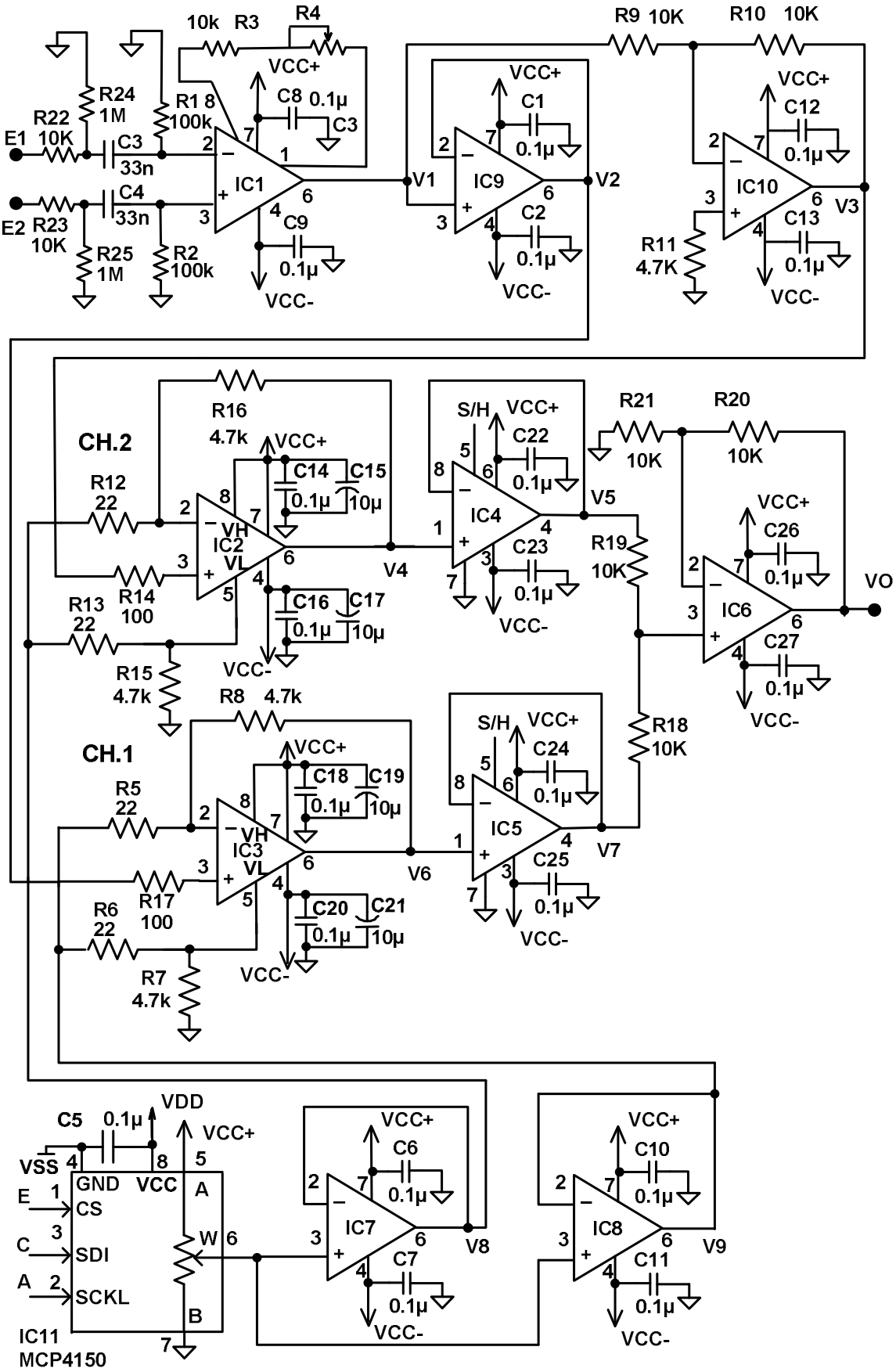

Fig. 4.17 Two-channel slicing and sampling
(IC1: INA128, IC2 - IC3:AD8037, IC4 - IC5:HA5351, IC6-IC9:LF356)

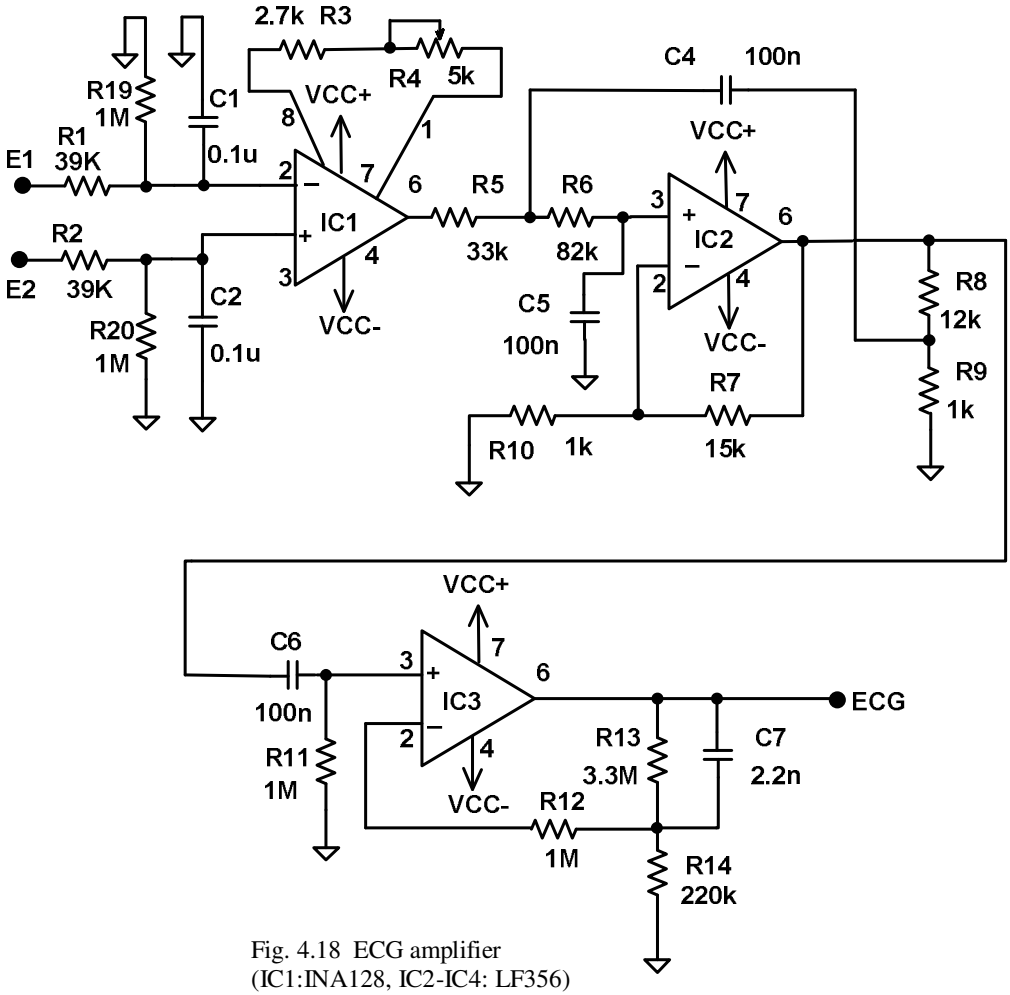

Fig. 4.18 ECG amplifier
(IC1:INA128, IC2-IC4: LF356)

To avoid the error, two channels of the slicing and the sample-and-hold circuit are implemented as shown in Fig. 4.17. The output of the difference amplifier is connected to the Channel-1. It is also connected to Channel-2 after inversion. Each channel consists of the slicing amplifier and the sample-and-hold circuit. The positive peak of the amplitude modulated carrier is sliced and amplified by the slicing amplifier of Channel-1 and the negative peak is sliced, inverted, and amplified by the slicing amplifier of Channel-2. The sample-and-hold circuit in each channel samples the output in a small duration near the peak and holds it. The outputs are added together. Thus any low frequency offset in the input gets cancelled and the demodulated output represents the impedance variation.

4.7 ECG amplifier

The R peak of the ECG signal is used as a reference signal in impedance cardiography. The ECG amplifier was adapted from earlier designs [14], [16]. The voltage sensing electrodes in the impedance cardiograph picks up the ECG signal along with the amplitude modulated

carrier signal. As shown in Fig. 4.18, the lowpass filter rejects the high frequency amplitude modulated carrier. The difference amplifier amplifies the low frequency ECG signal and cancels the common mode pickup. The output is given to the filter section. It has a lowpass filter with cut-off frequency of 20 Hz and highpass filter with the cut off frequency of 1.6 Hz to eliminate offset and low frequency drift and to accentuate the R-peaks. The total gain is in the range of 170 to 440. It may be noted that the ECG signal is taken from ICG electrodes and is severely highpass filtered. The output should be used only for getting the R peaks and not for other features of the ECG waveform.

4.8 Baseline restoration circuit

A bioimpedance signal generally consists of a large baseline drift over small signal excursion [7], [22], [23]. The drift varies with the electrodes placement and a motion artifact. Highpass filtering result in loss of signal components. The signal may be digitally processed to remove the large drift after digitization of the signal. However, to make an effective use of the input range of the analog-to-digital converter, the drift must be removed at least partially before signal acquisition.

The baseline restoration circuit reported by Pandey *et. al.* [22], [23] is used for our circuit. As shown in Fig. 4.19, the output signal of the amplifier is compared with two threshold voltages [V_{t1}, V_{t2}].The threshold voltages are set corresponding to the input range of the signal acquisition. When output crosses the threshold range in either direction, the up-down counter is updated and the new estimation of the drift voltage (output of the digital-to-analog converter (D/A)) gets subtracted from the input signal. One quantization step of D/A converter after amplification corresponds to half of the threshold voltage range. Thus after threshold range crossing of the output, the signal is brought back in to the middle of the range. The output voltage V_o for the circuit shown in Fig. 4.20 is given as,

$$V_O = A_s V_{in} - A_x \left(V_x - \frac{A_r V_r}{A_x} \right) \tag{4.19}$$

where,

$$A_s = \left(\frac{R_2 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3} \right) \left(1 + \frac{R_5}{R_4} \right)$$

$$A_r = \left(\frac{R_1 R_2}{R_1 R_2 + R_1 R_3 + R_2 R_3} \right) \left(1 + \frac{R_5}{R_4} \right)$$

$$A_x = \frac{R_5}{R_4}$$

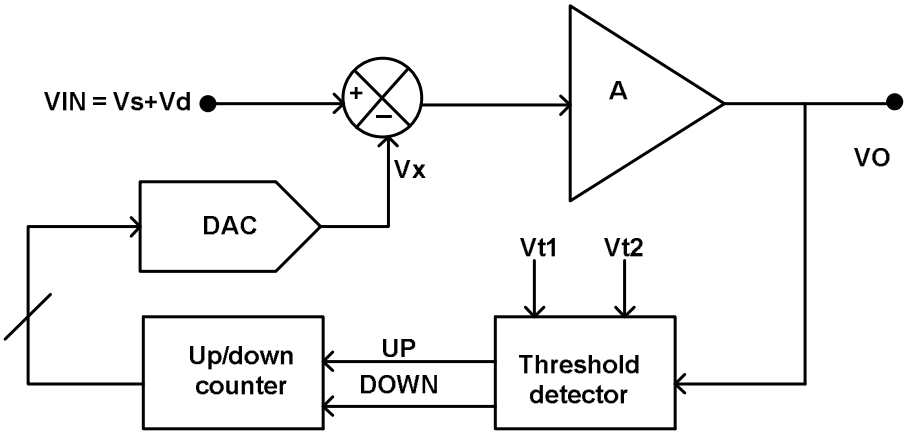

Fig. 4.19 Block diagram of tracking based baseline restoration circuit [22], [23]

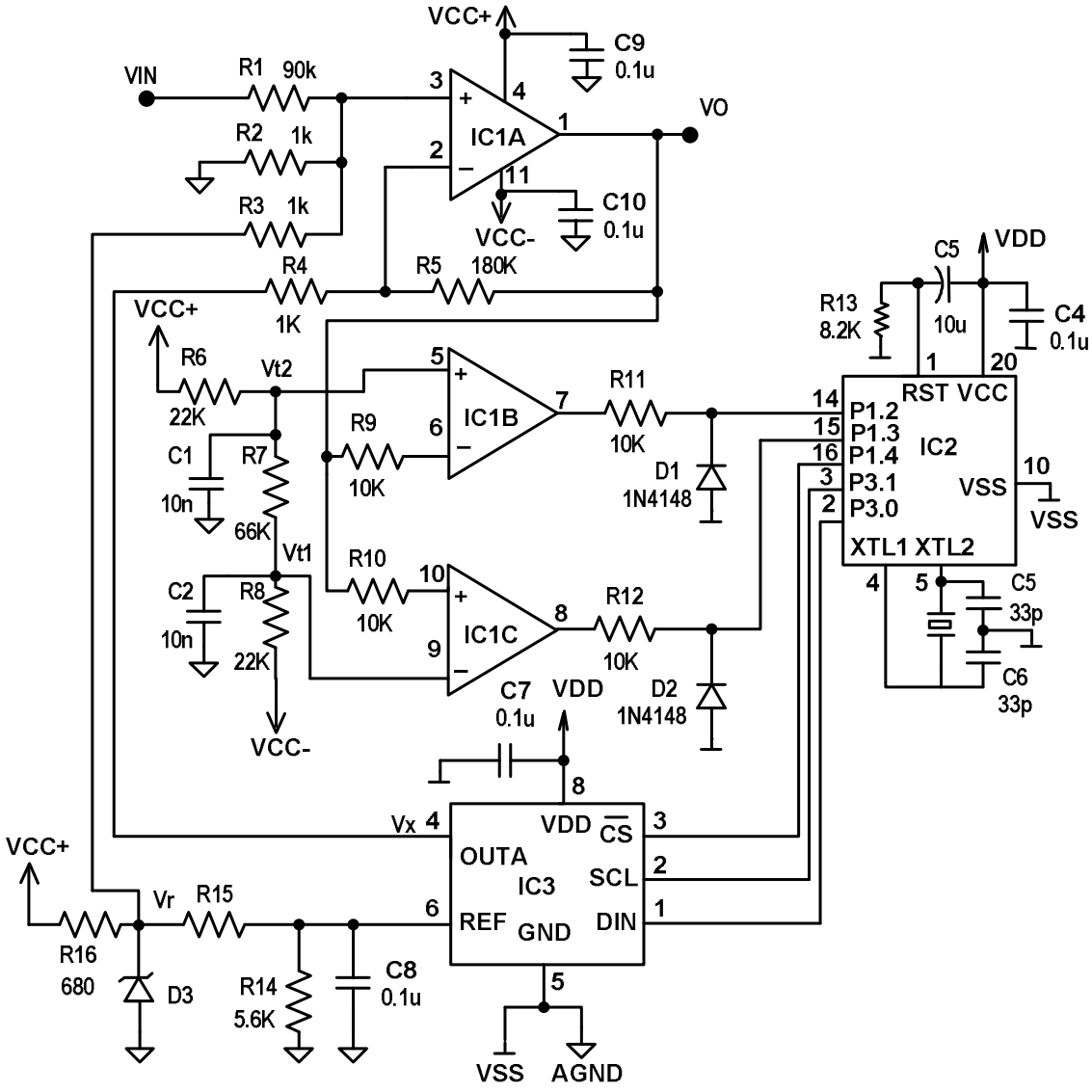

Fig. 4.20 Baseline restoration circuit [22], [23] (IC1: LM324, IC2: AT89C2051, IC3:TLV5618)

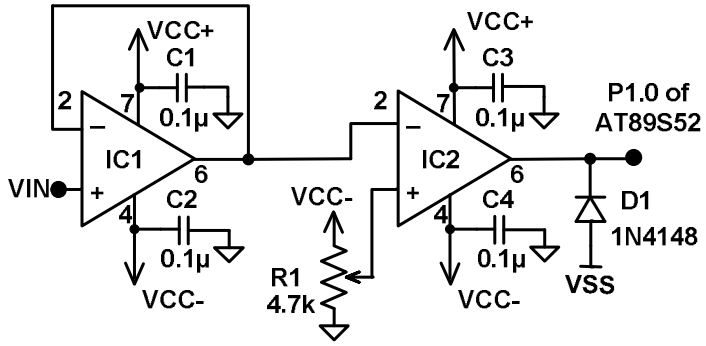

Fig. 4.21 High contact impedance indicator [16].

The input signal is the signal of interest V_s superimposed on the baseline drift voltage V_d. The signal gain A_s is given as,

$$A_s = \frac{V_{t2} - V_{t1}}{V_{s\,max} - V_{s\,min}} \tag{4.20}$$

For the step voltage of ΔV_x of D/A converter, the gain A_r is given as,

$$A_r = 0.5\left(\frac{V_{t2} - V_{t1}}{\Delta Vx}\right) \tag{4.21}$$

Thus amplified quantization step is half of the threshold voltage range. With reference voltage of 4.2 V, 256 steps of D/A converter, ΔV_x is about 16 mV. The component values in Fig 4.20 are selected for A_s = 1, A_r = 90, A_x = 180, threshold voltages of ± 3 V, and V_r = 4.2 V. Compared to the signal gain of around 45 in [22], we have a smaller gain in the baseline restoration circuit, because the slicing amplifier provides a gain of around 200.

4.9 Contact impedance indicator

A contact impedance indicator is required to ensure proper contact between the skin and a surface electrode. For this purpose output of the demodulator can be compared with the known voltage corresponding to a nominal value of a basal resistance as shown in Fig. 4.21. The output of the comparator is connected to the port pin of a microcontroller. When the demodulated output exceeds the set reference voltage level, an indication is given on the LCD. The reference value for the high impedance can be set by using the potentiometer R1.

4.10 The controller circuit

The controller circuit is shown in Fig. 4.22. A microcontroller IC1 AT 89S52 is used as controller of the hardware. The two digital potentiometers and the two DDS are controlled

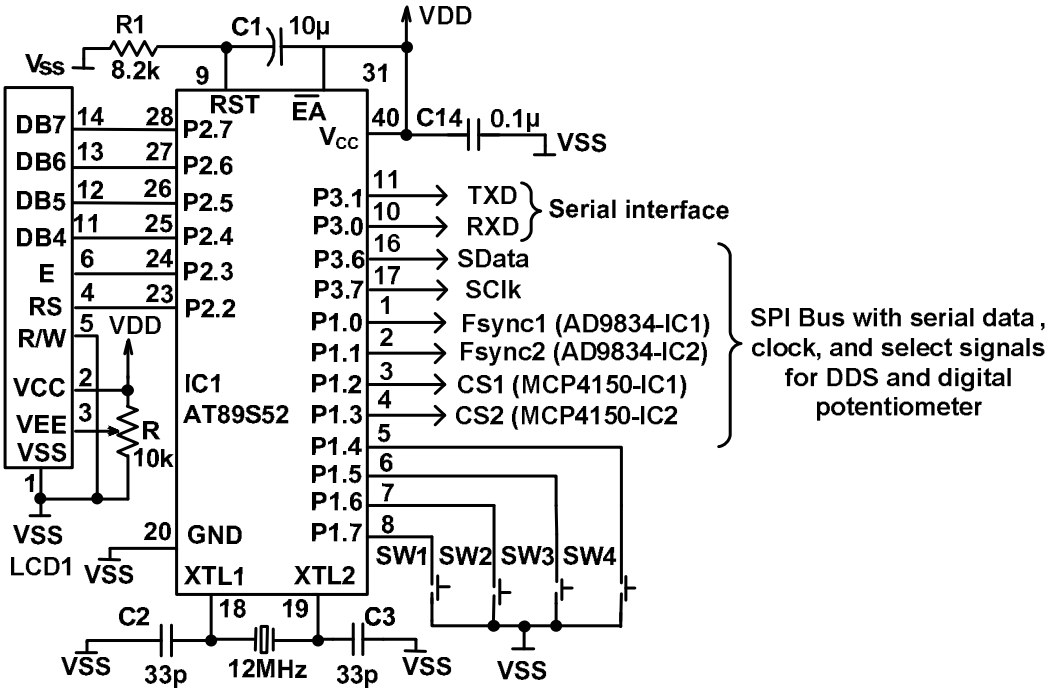

Fig. 4.22 Controller circuit

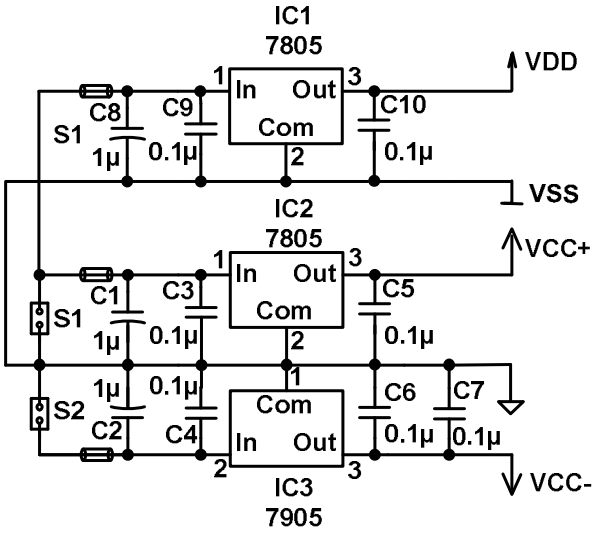

Fig. 4.23 Power supply circuit

via SPI bus. The two potentiometers are used for setting the current level and to set slicing reference voltage level. The two DDS chips are used in the oscillator circuit. An LCD (LCD1) and four soft keys (SW1, SW2, SW3, and SW4) provide user interface. The soft

keys are directly connected to the pins of Port-1 and no pull-up resistors are needed. The LCD is interfaced using 4-pin parallel interface to the pins of Port2

4.11 Power supply

The circuit is powered by ±9 V dc. Two voltage regulators, (IC2 and IC3) are used to supply the analog sections of the hardware with regulated +5 V and −5 V as shown in Fig. 4.23. The digital section is powered by regulated +5 V from a separate voltage regulator IC1.

Chapter 5
TEST AND RESULTS

5.1 Output of the diode based slicing amplifier

Input voltage to the slicing amplifier is of 2.28 V (p-p) with a frequency approximately 50 kHz. The reference voltage is set around 840 mV. The 300 mV difference is amplified with gain of around 30. For the frequencies greater than 50 kHz, the delay is observed between input and output signals. The output waveform is shown in Fig. 5.1.

5.2 Output of the slicing amplifier and sample-and-hold circuit using voltage clamp amplifier IC AD8037

The waveforms are shown in Fig. 5.2. Vin represents input to the slicing amplifier, V_{slice} represents output of the slicing amplifier, and V_{sample} represents the output of the sample-and-hold circuit. The outputs of two channels of slicing and sampling circuit are shown in Fig. 5.3.

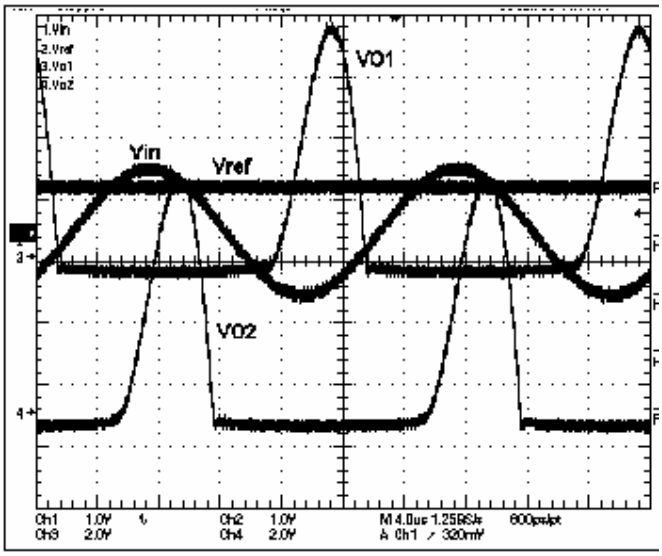

Fig. 5.1 Output waveforms of diode based slicing amplifier for f = 50 kHz

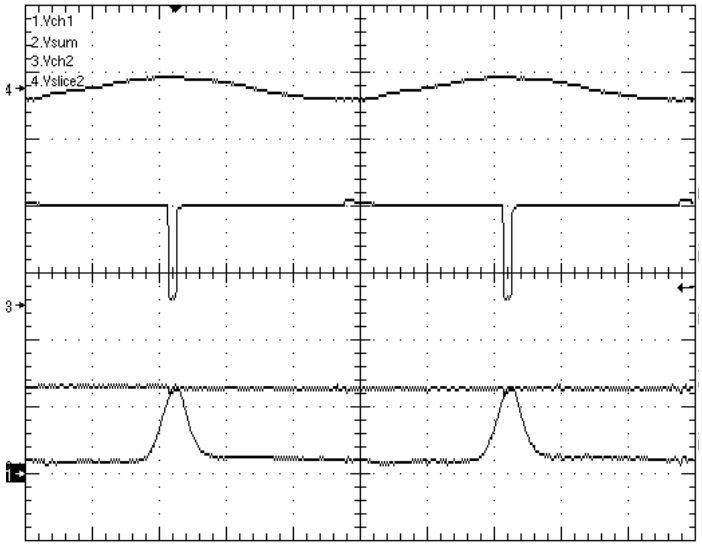

Fig. 5.2 Output waveforms of slicing amplifier using voltage clamp amplifier IC AD8037 for f = 100 kHz

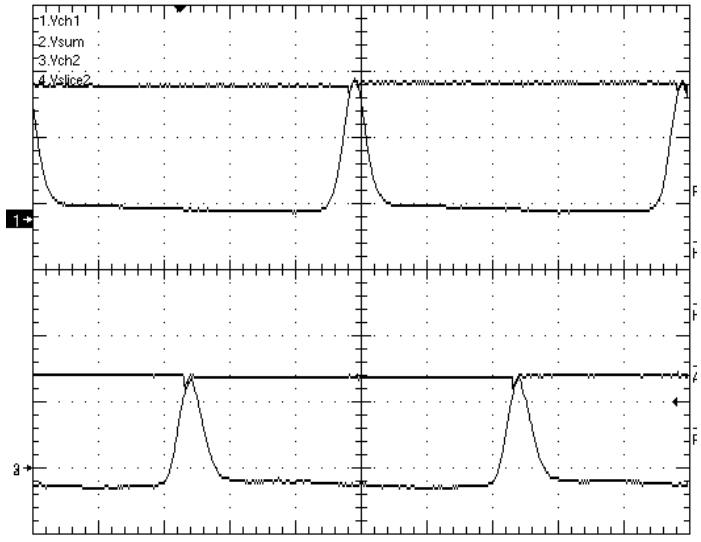

Fig. 5.3 Output waveforms of two channels of slicing and sampling for f = 100 kHz

5.3 Validation of the hardware using thorax simulator

The thorax simulator is used to test the hardware developed for the impedance cardiography. The current source output is connected to the current terminals of the simulator. The voltage sensing terminals are connected to the input terminals of the difference amplifier of the impedance detector. The excitation current is of approximately 1 mA. The basal impedance is set as 196 Ω. The demodulated outputs of each channel and the summing amplifier are observed on the CRO for various simulator settings. It is observed that, the demodulated

output signal is contaminated with 50 Hz noise of about 1V. When internal common of the simulator circuit is connected to the circuit ground, the interference noise is reduced to 80 mV. An example of the output signal of Channel-2 is shown in Fig. 5.4 for the two cases.

Output waveforms were observed for different values of ΔR and for carrier frequencies of 50 kHz and 100 kHz. The peak-to peak values of the demodulator outputs are shown in Table 5.1 for the simulator setting of R = 196 Ω, Freq. = 1 Hz, Type of resistance variation: sinusoidal. From these results, the impedance detector was found to successfully demodulate the signal with modulation as low as 0.2%.

Table 5.1 Demodulator output voltages of Channel-1 and Channel-2

Sr. No.	$\Delta R/R$ (%)	f = 50 kHz		f = 100 kHz	
		Ch.-1 output (p-p mV)	Ch.-2 output (p-p mV)	Ch.-1 output (p-p mV)	Ch.-2 output (p-p mV)
1	1.2	830	530	560	360
2	1.0	630	400	390	300
3	0.8	480	310	330	320
4	0.6	400	260	290	260
5	0.4	240	200	170	150
6	0.2	170	150	100	80
7	0	0	0	0	0

5.4 Output waveforms of each channel and summing amplifier

The output waveforms of Channel-1, Channel-2, and summing amplifier are shown in Fig. 5.5 – Fig. 5.10 for the different settings of the thorax simulator as given in Table 5.2.

Table 5.2 Settings of the thorax simulator for the outputs shown in Fig. 5.5 – Fig. 5.10

Figure	f (Hz)	R (Ω)	$\Delta R/R$ (%)	Variation
Fig. 5.5	1	196	1.2	Sinusoidal
Fig. 5.6	1	196	1.2	Square
Fig. 5.7	1	196	0.6	Sinusoidal
Fig. 5.8	1	196	0.6	Square
Fig. 5.9	32	196	1.2	Sinusoidal
Fig. 5.10	1	196	0	Sinusoidal

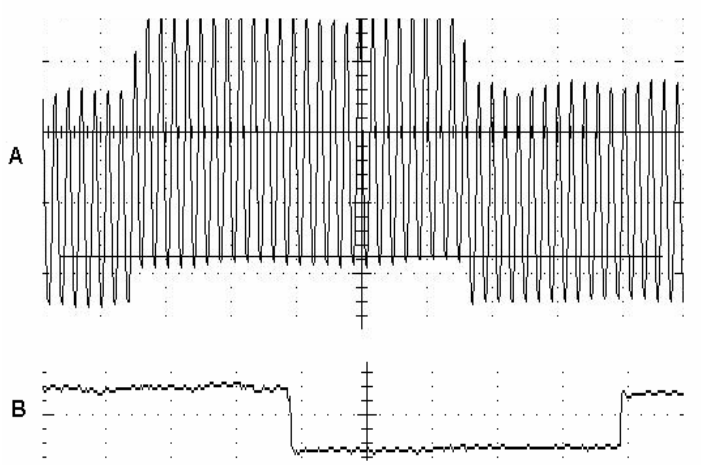

Fig. 5.4 Demodulated output waveforms of Channel-2
A. When simulator int. com. is not connected with circuit ground
B. When simulator int. com. is connected with circuit ground

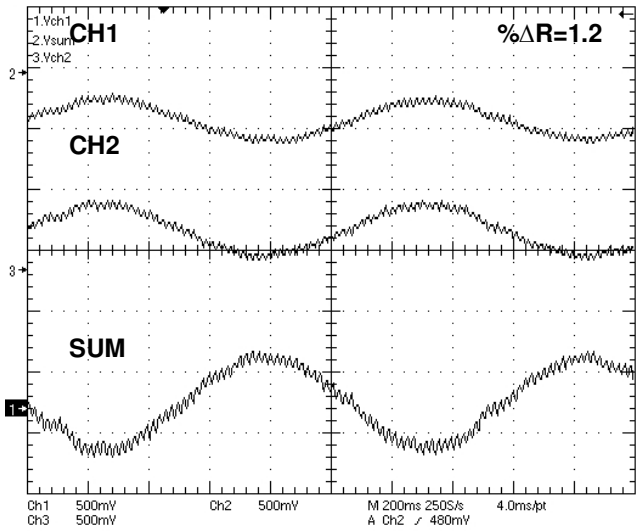

Fig. 5.5 Output waveforms of Channel-1, Channel-2, and summing amplifier for exc. freq = 100 kHz; R = 196 Ω, f = 1 Hz, $\Delta R/R$ =1.2%, variation = sinusoidal

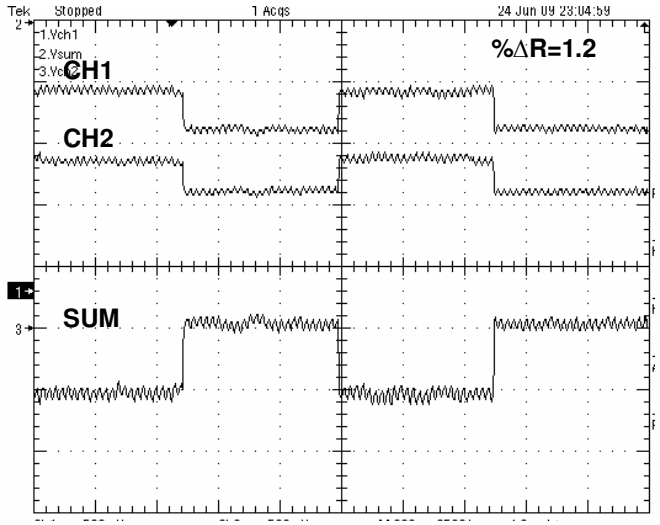

Fig. 5.6 Output waveforms of Channel-1, Channel-2, and summing amplifier for exc. freq = 100 kHz; R = 196 Ω, f = 1 Hz, $\Delta R/R$ =1.2%, variation = square.

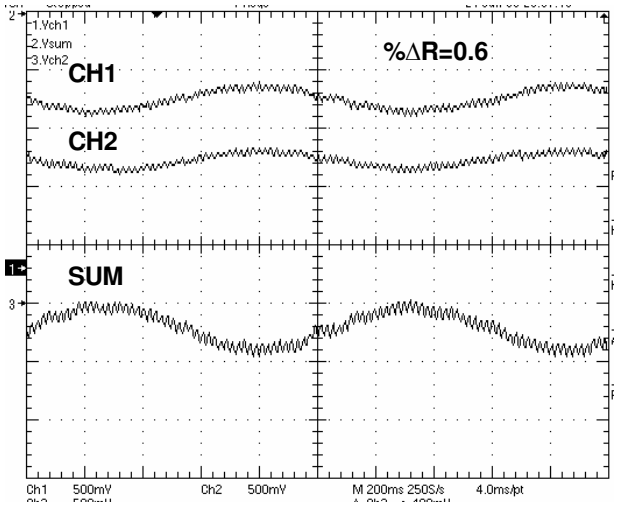

Fig. 5.7 Output waveforms of Channel-1, Channel-2, and summing amplifier for exc. freq = 100 kHz; R = 196 Ω, f = 1 Hz, $\Delta R/R$ =0.6 %, variation = sinusoidal

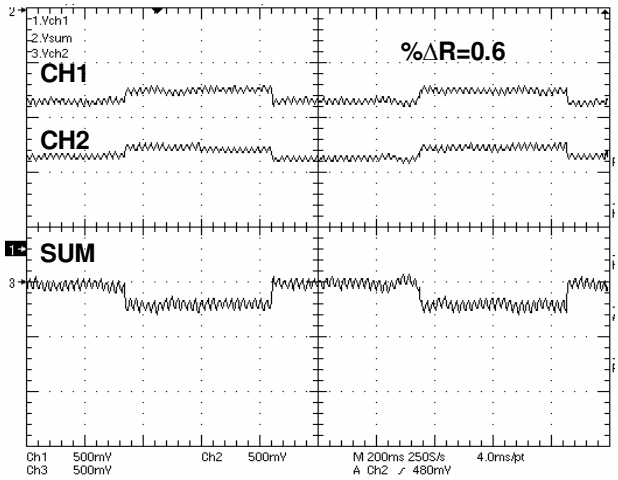

Fig. 5.8 Output waveforms of Channel-1, Channel-2, and summing amplifier for exc. freq = 100 kHz; R = 196 Ω, f = 1 Hz, $\Delta R/R$ = 0.6%, variation = square

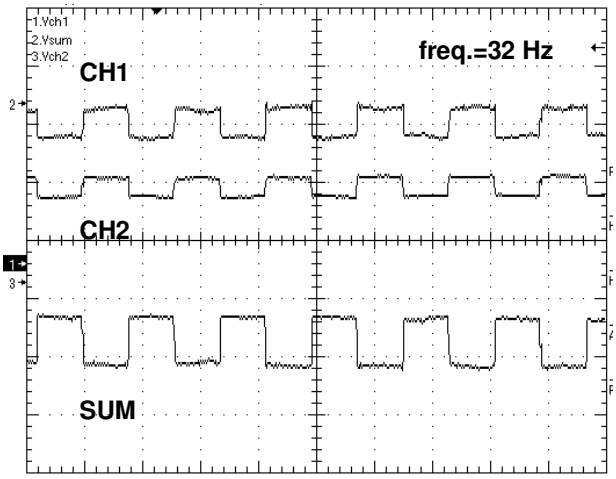

Fig. 5.9 Output waveforms of Channel-1, Channel-2, and summing amplifier, for exc. freq = 50 kHz; R = 196 Ω, f = 32 Hz, $\Delta R/R$ =1.2%, variation = square.

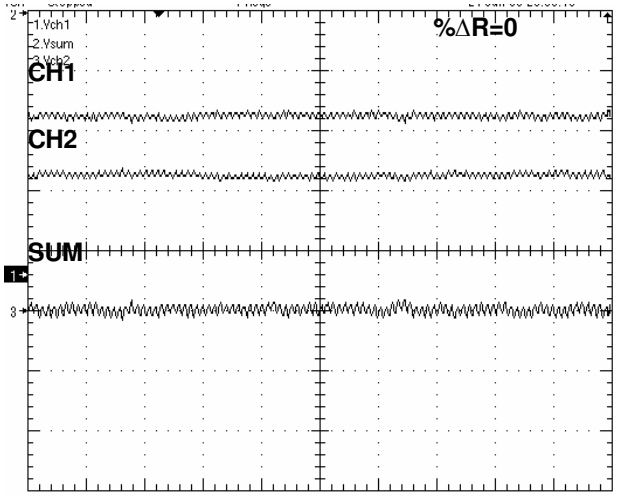

Fig. 5.10 Output waveforms of Channel-1, Channel-2, and summing amplifier for exc. freq = 50 kHz; R = 196 Ω, f = 1 Hz, $\Delta R/R$ = 0 %, variation = sinusoidal

Chapter 6
SUMMARY AND CONCLUSION

The project objective was to develop instrumentation for impedance cardiography, based on earlier reported circuits as well as by investigating new circuits for improving the performance.

As the first stage in the development of the instrumentation, a thorax simulator using a microcontroller and digital potentiometers has been developed and prototyped for testing and calibration of ICG and ECG hardware. Development involved upgrading features of the earlier designs of bioimpedance thorax simulator [14]-[16], [19], by using digital potentiometers for simulation of various shapes for ECG and ICG signals. The circuit permits simultaneous simulation of these two waveforms. The various wave shapes like sinusoidal and square for testing of the ECG circuit have been realized, by using different lookup tables in the microcontroller's memory. The frequency range of the ICG signal is extended up to 250 Hz. Thus the circuit can be used for calibration of some of the other bioimpedance measuring instruments, like glottograph.

After studying the various circuit blocks of the ICG hardware, a new instrument is designed, involving new approaches to the excitation source as well as the demodulator for sensing the small variation in thoracic impedance, with high sensitivity, low signal distortion, and low noise. Modified Howland current source is used for the voltage-to-current conversion. This reduces instability problem due to stray capacitances at the op amp input terminals as faced in the earlier circuits. An innovative demodulator is developed. It is based on a slicing amplifier for increasing the sensitivity, and synchronous sample-and-hold for eliminating the carrier ripple and reducing the noise. A programmable waveform generator based on a DDS AD9834 is used to generate sinusoidal signal of the frequency in range of 50 kHz to 500 kHz. Two DDS chips are synchronized by operating on the same master clock and synchronized software controls. One DDS provide sinusoidal input to the voltage-to-current converter while the square wave output of the other DDS is used as reference signal for the sampling pulse generation circuit. The microcontroller controlled circuit provides flexibility in selection of the frequency as well as phase shift. The excitation current is set by a digital potentiometer. All the parameters can be set using the 4-soft keys and the LCD or by serial interface to the microcontroller. Another digital potentiometer is

used to set the reference level for the slicing amplifier of the demodulator, which corresponds to subtraction of a specific value of the base impedance.

The impedance cardiograph is tested using the thorax simulator. The test is carried out by changing various parameters of the simulator. Circuit was tested and found to work satisfactory for modulation index in the range from 0.1 to 1.2 for the modulating frequencies from 1 Hz to 250 Hz.

The thorax simulator circuit has been assembled on a 2-layer PCB with PTH and fully tested and boxed. The schematic and the PCB layouts for the simulator are given in Appendix B and C respectively. For the impedance cardiography hardware, a 2-layer PCB layout has been prepared. The schematic and the layouts for the impedance cardiography hardware are given in Appendix D and E respectively. The circuit needs to be assembled on the PCB, boxed, and tested.

Appendix A
VOLTAGE CLAMP AMPLIFIER IC AD 8037

Figure A.1 is an idealized block diagram of voltage clamp amplifier AD8036 connected as a unity gain voltage follower. The primary signal path comprises A1 (a 1200 V/μs, 240 MHz high voltage gain, differential to single-ended amplifier) and A2 (a G = +1 high current gain output buffer). The AD8037 differs from the AD8036 only in that A1 is optimized for closed-loop gains of two or greater. The CLAMPIN section is comprised of comparators CH and CL, which drive switch S1 through a decoder. The unity-gain buffers in series with +VIN, VH, and VL inputs isolate the input pins from the comparators and S1 without reducing bandwidth or precision. The two comparators have about the same bandwidth as A1 (240 MHz), so they can keep up with signals within the useful bandwidth of the AD8036.

To illustrate the operation of the CLAMPIN circuit, consider the case where VH is referenced to 1 V, VL is open, and the AD8036 is set for a gain of +1, by connecting its output back to its inverting input through the recommended 140 Ω feedback resistor. Note that the main signal path always operates closed loop, since the CLAMPIN circuit only affects A1's noninverting input. If a 0 V to 2 V voltage ramp is applied to the AD8036's +VIN for the connection just described, VOUT should track +VIN perfectly up to 1 V, then should limit at exactly 1 V as +VIN continues to 2 V. In practice, the AD8036 comes close to this ideal behavior. As the +VIN input voltage ramps from zero to 1 V, the output of the high limit comparator CH starts in the off state, as does the output of CL. When +VIN just exceeds VIN (ideally, by say 1 μV, practically by about 18 mV), CH changes state, switching S1 from "A" to "B" reference level. Since the + input of A1 is now connected to VH, further increases in +VIN have no effect on the AD8036's output voltage. In short, the AD8036 is now operating as a unity-gain buffer for the VH input, as any variation in VH, for VH > 1 V, will be faithfully reproduced at VOUT.

Operation of the AD8036 for negative input voltages and negative clamp levels on VL is similar, with comparator CL controlling S1. Since the comparators see the voltage on the +VIN pin as their common reference level, then the voltage VH and VL are defined as "High" or "Low" with respect to +VIN. For example, if VIN is set to zero volts, VH is open, and VL is +1 V, comparator CL will switch S1 to "C," so the AD8036 will buffer the

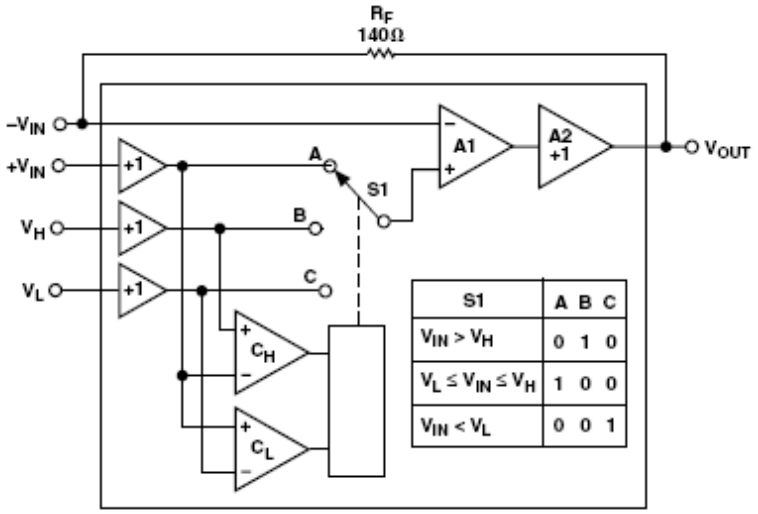

Fig. A.1 Internal block diagram of AD 8037

voltage on VL and ignore +VIN. The performance of the AD8036 and AD8037 closely matches the ideal just described. The comparator's threshold extends from 60 mV inside the clamp window defined by the voltages on VL and VH to 60 mV beyond the window's edge. Switch S1 is implemented with current steering, so that A1's +input makes a continuous transition from say, VIN to VH as the input voltage traverses the comparator's input threshold from 0.9 V to 1.0 V for VH = 1.0 V. The practical effect of these nonidealities is to soften the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the CLAMPIN circuit. The AD8036's and AD8037's CLAMPIN input clamp architecture works only for noninverting or follower applications and, since it operates on the input, the clamp voltage levels VH and VL, and input error limits will be multiplied by the amplifier's closed-loop gain at the output. For instance, to set an output limit of ±1 V for an AD8037 operating at a gain of 3.0, VH and VL would need to be set to +0.333 V and –0.333 V, respectively. The only restriction on using the AD8036's and AD8037's +VIN, VL, VH pins as inputs is that the maximum voltage difference between +VIN and VH or VL should not exceed 6.3 V, and all three voltages be within the supply voltage range. For example, if VL is set at –3 V, then VIN should not exceed +3.3 V

Appendix B

SCHEMATIC DIAGRAM OF THE THORAX SIMULATOR

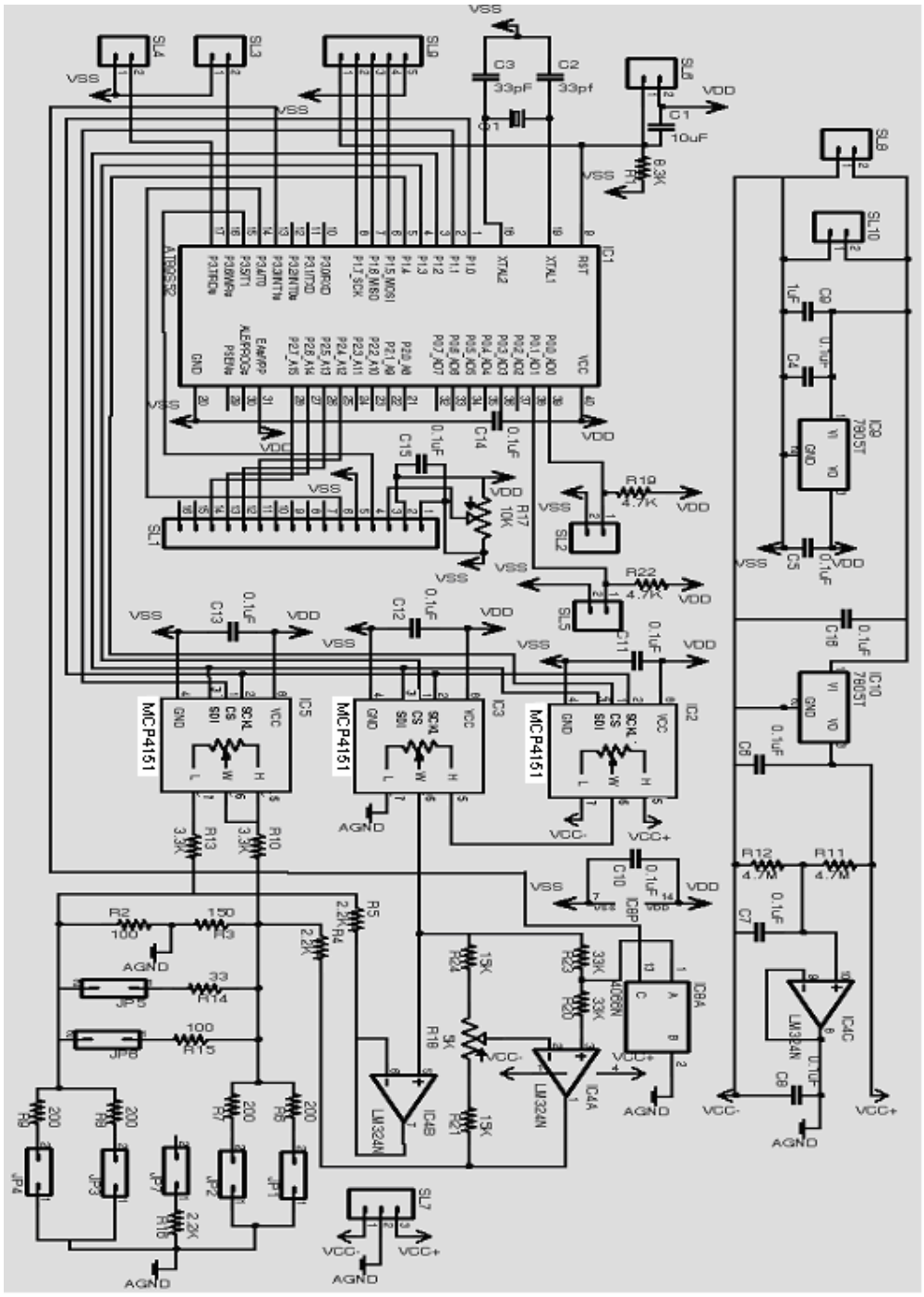

Fig. B.1 Schematic diagram of the thorax simulator

Appendix C

PCB LAYOUT OF THORAX SIMULATOR

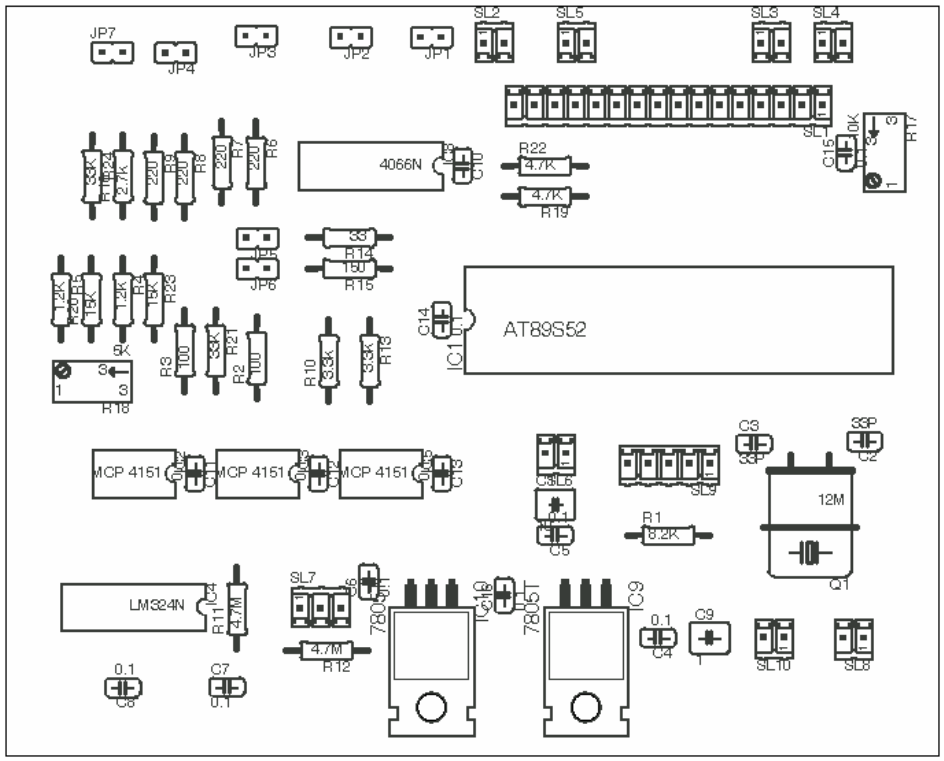

Fig. C.1 Component placement layout of thorax simulator PCB (12.5 cm× 9.5 cm)

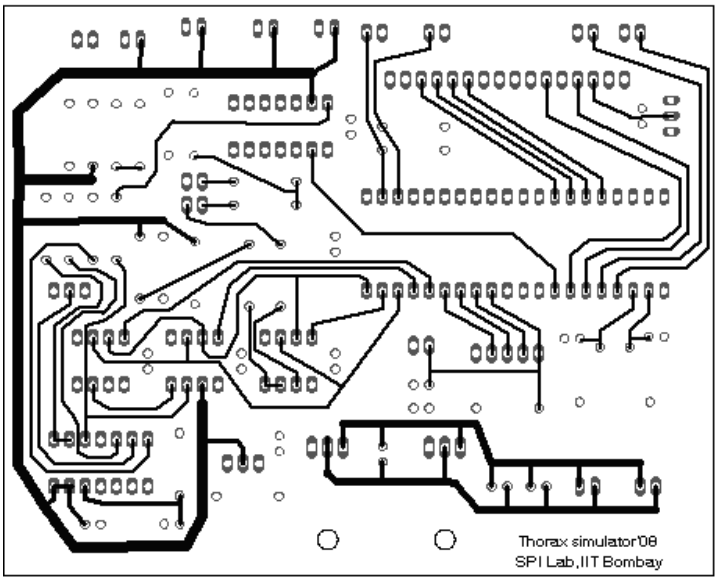

Fig. C.2 Component side of thorax simulator PCB (12.5 cm × 9.5 cm)

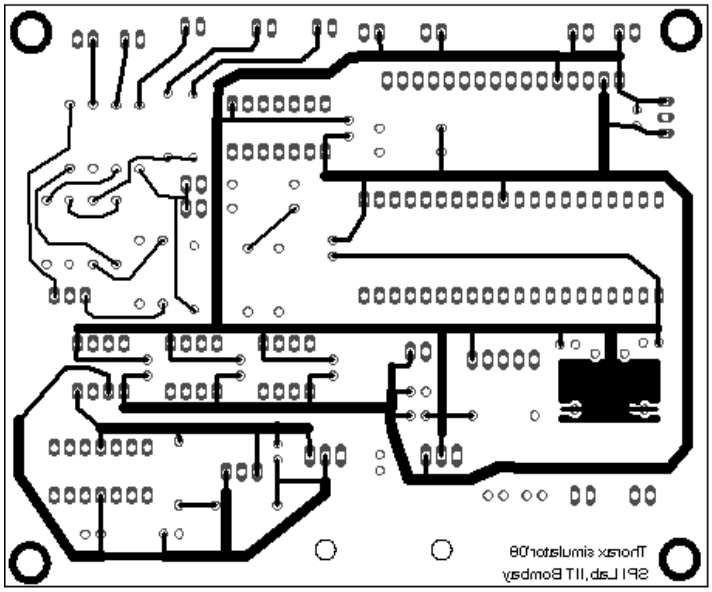

Fig. C.3 Solder side of thorax simulator PCB (12.5 cm × 9.5 cm)

Appendix D

SCHEMATIC DIAGRAM OF THE IMPEDANCE CARDIOGRAPHY HARDWARE

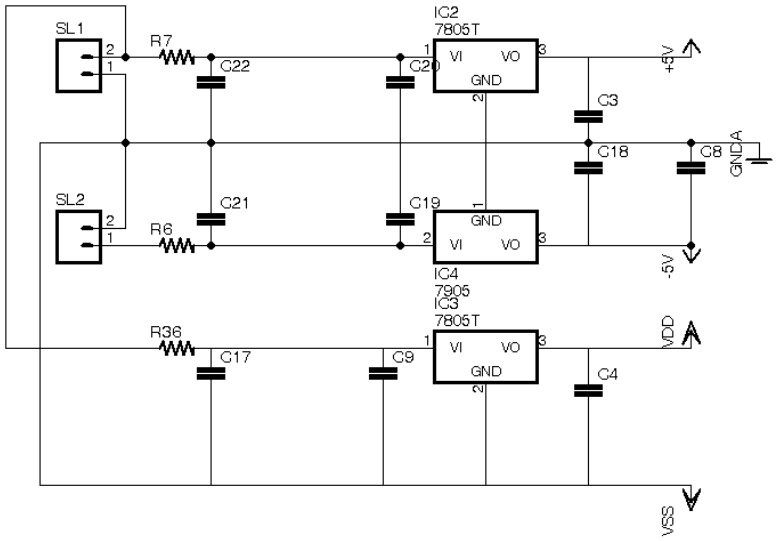

Fig. D.1 Schematic diagram of the power supply as the part of the impedance cardiography hardware

Appendix E

PCB LAYOUT OF IMPEDANCE CARDIOGRAPHY HARDWARE

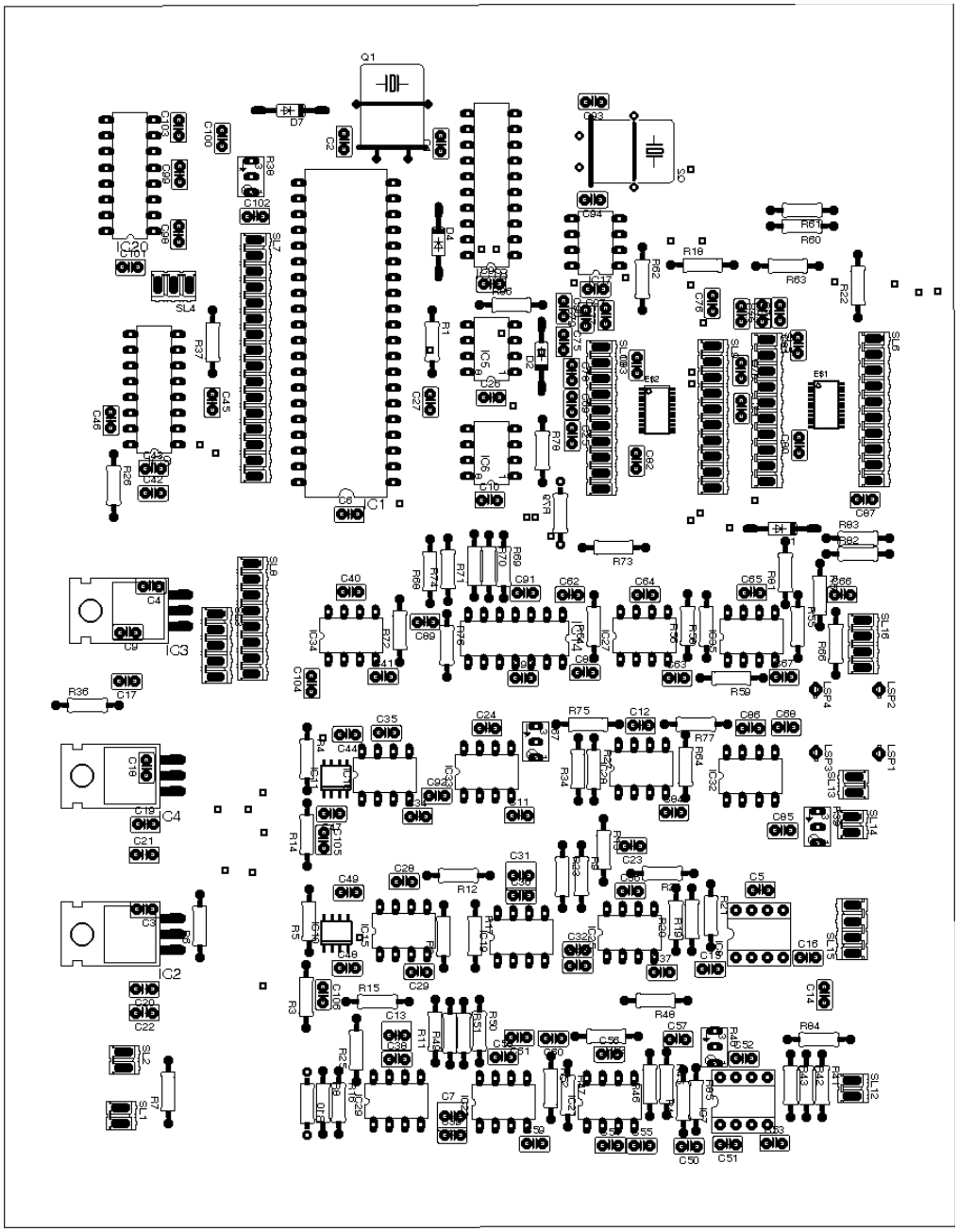

Fig. E.1 Components placement of impedance cardiograph PCB (20 cm × 15 cm)

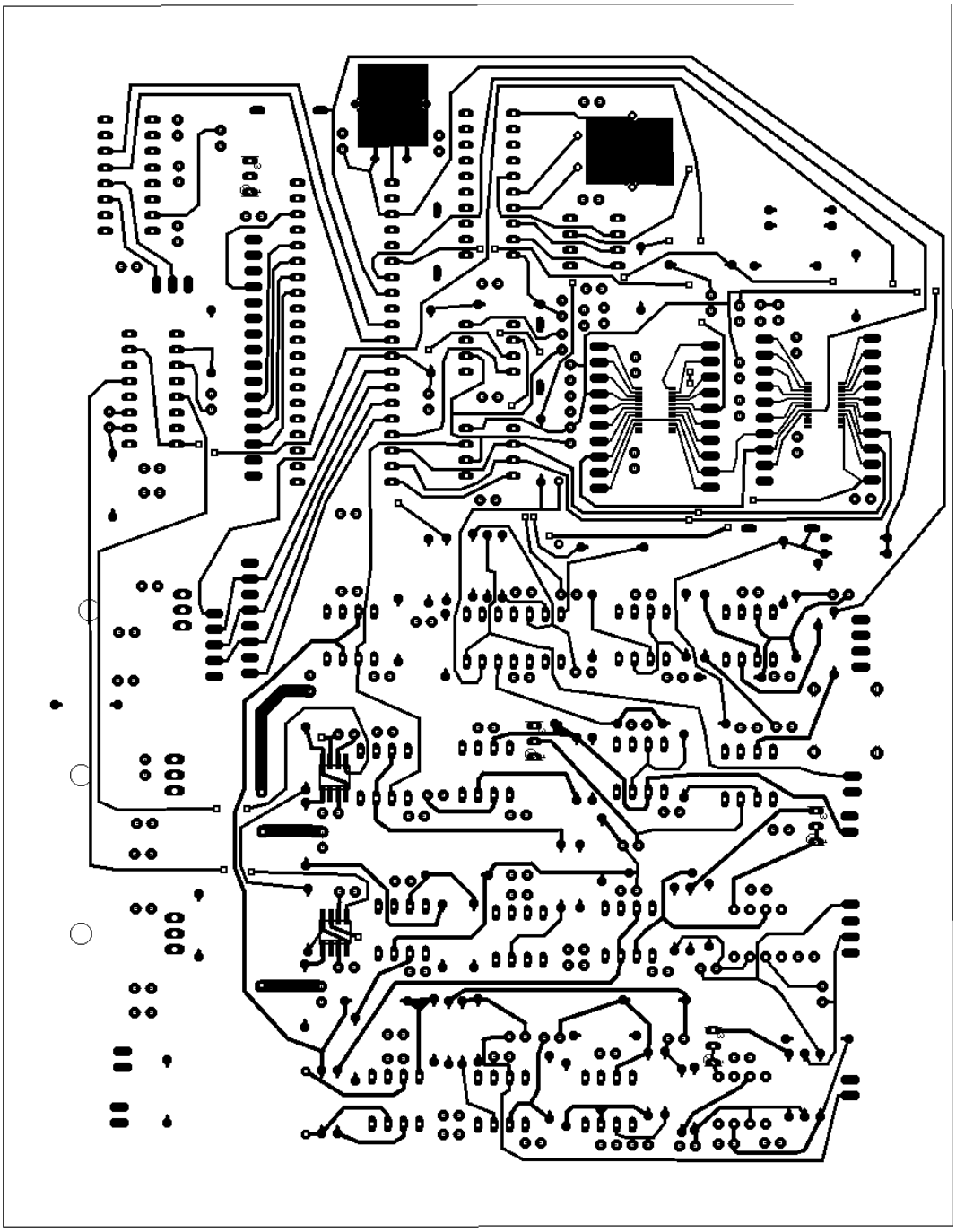

Fig. E.2 Component side of impedance cardiograph PCB (20 cm × 15 cm)

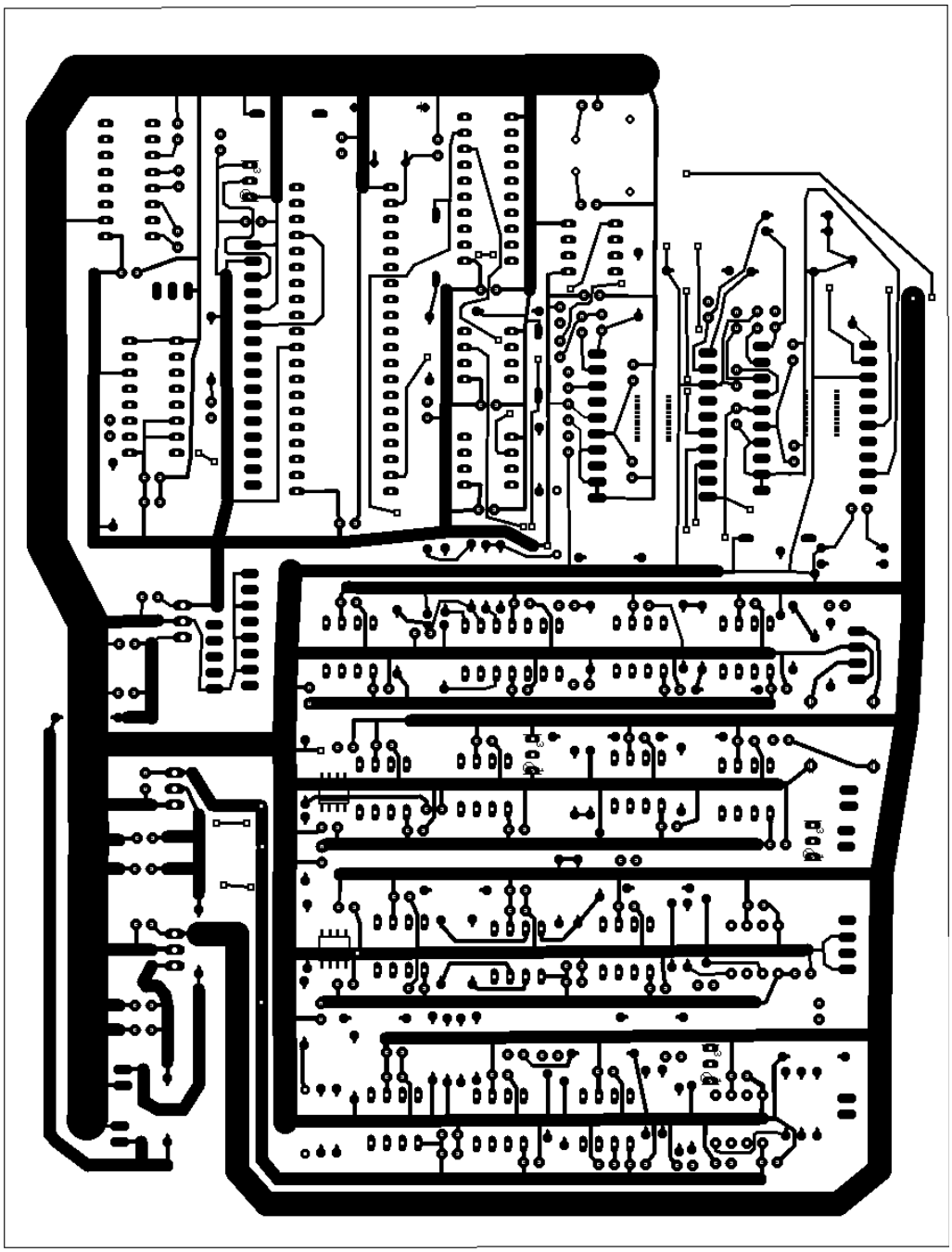

Fig. E.3 Solder side of impedance cardiograph PCB (20 cm × 15 cm)

REFERENCES

[1] J. Nyboer, *Electrical Impedance Plethysmography,* 2nd ed., Charles C. Thomas, Springfield, Massachusetts, 1970.

[2] L. Cromwell, F. J. Weibell, and E. A. Pfeiffer, *Biomedical Instrumentation and Measurements*, 2nd ed., Prentice Hall, New Delhi, 1990.

[3] M. Min, T. Parve, A. Ronk, P. Annus, and T. Paavle, "Synchronous sampling and demodulation in an instrument for multifrequency bioimpedance measurement", *IEEE Trans. Inst. Meas*, vol. 56, pp. 1365 - 1372, 2007

[4] W. G. Kubicek, F. J. Kottke, and M. U. Ramos, "The Minnesota impedance cardiograph – theory and applications", *Biomed. Eng*., vol. 9, pp. 410 - 416, 1974

[5] L. E. Baker, "Principles of impedance technique", *IEEE Eng. Med. Biol. Mag.,* vol. 8, pp. 11 - 15, 1989.

[6] R. P. Patterson, "Fundamentals of impedance cardiography", *IEEE Eng. Med. Biol. Mag.,* vol. 8, pp. 35 - 38, 1989.

[7] M. Qu, Y. Zhang, J. G. Webster, and W. J. Tompkins, "Motion artifact from spot and band electrodes during impedance cardiography", *IEEE Trans. Biomed. Eng.,* vol. 33, pp. 1029 - 1036, 1986.

[8] J. Wtorek and A. Polinski, "Multifrequency impedance plethysmograph", in *Proc. IEEE Inst. Meas. Tech. Conf.*, Brussels, Belgium, 1996, pp. 1452 - 1455.

[9] J. Fortin, W. Habenbacher, and A. Heller, "Non-invasive beat-to-beat cardiac output monitoring by an improved method of transthoracic bioimpedance measurement", *Comp. Bio. Med.,* vol. 36, pp. 1185 - 1203, 2006.

[10] F. Mora, G. Villegas, A. Hernandez, W. Coronado, R. Justiniano, and G. Passariello, "Design of an instrumentation system for a neurocardiology laboratory", in *Proc. 2nd Int. Conf. IEEE Dev., Cir. and Sys.*, Carcas, Venezuela, 1998, pp. 272 - 277.

[11] V. Vondra, J. Halamek, I. Viscor, and P. Jurak, "Two channel bioimpedance monitor for impedance cardiography", in *Proc. 28th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.,* 2006, pp. 6061 - 6063.

[12] G. Panfili, L. Piccini, L. Maggi, S. Parini, and G. Andreoni, "A wearable device for continuous monitoring of heart mechanical function based on Impedance Cardiography", in *Proc. 28th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, 2006, pp. 5968 - 5971.

[13] B. P. Kuriakose / P. C. Pandey (Supervisor), "An impedance cardiograph", *M.Tech. Dissertation*, Biomedical Engineering Group, School of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2000.

[14] N. S. Manigandan / P. C. Pandey (Supervisor), "Development of hardware for impedance cardiography", *M.Tech. Dissertation*, Biomedical Engineering Group, School of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2004.

[15] N. K. S. Naidu / P. C. Pandey (Supervisor), "Hardware for impedance cardiography", *M.Tech. Dissertation*, Biomedical Engineering Group, School of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2005.

[16] L. Venkatachalam / P. C. Pandey (Supervisor), "Development of hardware for impeda nce cardiography", *M.Tech. Dissertation*, Biomedical Engineering Group, School of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2006.

[17] J. N. Sarvaiya / P. C. Pandey (Supervisor), "Development of an impedance glottograph, *M.Tech. Dissertation*, Biomedical Engineering Group, School of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2006.
[18] A. C. Guyton, *Textbook of Medical Physiology*, 7th ed., Saunders, Philadelphia, 1986.
[19] V. K. Pandey, P. C. Pandey, and J. N. Sarvaiya, "Impedance simulator for testing of instruments for bioimpedance sensing", *IETE J. Research*, vol. 54, no. 3, pp. 203 - 207, 2008.
[20] G. D. Jindal and J. P. Babu, "Calibration of dz/dt in impedance plethysmography", *Med. Biol. Eng. Comp*., vol. 23, pp. 279 - 280, 1985.
[21] B. M. Oliver, Square-wave and pulse testing of linear systems, in B. M. Oliver and J. M. Cage (Eds.), *Electronic Measurements and Instrumentation*, McGraw Hill, Singapore 1975.
[22] V. K. Pandey and P. C. Pandey, "Tracking based baseline restoration circuit for acquisition of bio signals", *Electron. Letters,* vol.43, pp. 13 - 14, 2007.
[23] V. K. Pandey, N. K. S. Naidu, and P. C. Pandey, "Tracking based baseline restoration for acquisition of impedance cardiogram and other biosignals", in *Proc. 27th Annu. Int. Conf. IEEE Eng. Med. Biol.*, 2005, pp. 3486- 3489.
[24] H. Goovaerts, T. Faes, E. Raajimakers, and R. Heethaar, "An electrically isolated balanced wideband current source: basic considerations and design", *Med. Biol. Eng. Comp*., vol. 36, pp. 598 - 603, 1998.
[25] D. Tsunami, J. McNames, A. Colbert, S. Pearson, and R. Hammerschlag, "Variable frequency bioimpedance instrumentation", in *Proc. 26th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.,* 2004, pp. 2386 - 2389.
[26] K. Cheng, C. Chen, M. Huang, and C. Chen "A multi-frequency current source for bioimpedance application", in *ITAB*, Ioannina, Greece, 2006.
[27] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd ed, McGraw-Hill, New Delhi, 2002.
[28] A. J. Fourcin, "Laryngographic examination of vocal fold vibration", *Ventilatory and Phonatory Control Systems,* Oxford University Press, London, 1974, pp. 313 - 315.
[29] A. Ronk, P. Annus, and T. Paavle "Synchronous sampling and demodulation in an instrument for multifrequency bioimpedance measurement", *IEEE Trans. Inst. Meas.*, vol. 56, no. 4, pp. 1365 - 1372, 2007.
[30] R. Pallas-Areny and J. Webster, "Bio-electric impedance measurements using synchronous sampling", *IEEE Trans. Biomed. Eng.*, vol 40, no. 8, pp. 824 - 828, 1993.
[31] Microchip Technology, "7/8-bit single/dual SPI digital POT with volatile memory", Available online, ww1.microchip.com/downloads/en/DeviceDoc/22060a.pdf, downloaded on 27th Dec. 2007.
[32] Atmel Corporation, "8-bit microcontroller with 8K bytes in-system programmable flash AT89S52", Available online, www.atmel.com/dyn/resource/prod_documents/doc1919.pdf, downloaded on 27th Dec. 2007.
[33] Analog Devices, "Low distortion, wide bandwidth voltage feedback clamp amps AD8036/AD8037", Available online, www.analog.com/static/importedfiles/data_sheets/AD8036_8037.pdf, downloaded on 19th Nov. 2008.
[34] Analog Devices, "Low power 20 mW 2.3 V to 5.5 V programmable waveform generator AD9833" Available online, www.analog.com/static/importedfiles/Data_Sheets/AD9833.pdf, downloaded on 17th Nov. 2008.
[35] Analog Devices, "20mW power, 2.3 V to 5.5 V, 75 MHz complete DDS AD9834", Available online, www.analog.com/static/importedfiles/Data_Sheets/AD9834.pdf, downloaded on 20th May 2009.
[36] Texas Instruments, "Precision, low power instrumentation amplifier", Available online, focus.ti.com/lit/ds/symlink/ina128.pdf, downloaded on 25th Nov. 2008.
[37] Intersil, "64ns sample and hold amplifier", Available online, www.intersil.com/data/fn/fn3690., downloaded on 5th May 2009.

[38] Texas Instruments, "Dual monostable multivibrator with Schmitt-trigger inputs", Available online, focus.ti.com/lit/ds/symlink/sn74221.pdf, downloaded on 3rd June 2009

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Bhupesh B. Patil

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