A MICROCONTROLLER-BASED

INTEGRAL CYCLE POWER CONTROLLER

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Master of Technology

by

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Dissertation Approval

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ABSTRACT

In ac power control, phase angle switching permits fine control but it introduces higher order harmonics and electromagnetic interference. Use of integral cycle switching reduces electromagnetic interference but it gives relatively discrete control steps and results in sub-synchronous and super-synchronous harmonics in the power supply line and it may cause dc current in inductive loads. In this project, a microcontroller-based integral cycle controller is developed for providing fine control steps and for suppressing the sub-synchronous and super-synchronous harmonics by using a switching strategy based on a pseudo-random sequence. An IIR filter simulating the load inertia is used for controlling the cycles to keep the duty cycle within a specified tolerance about the desired value. The pseudo-random selection of on-cycles distributes the switching noise over a broad-band, without any dominant sub-synchronous and super-synchronous harmonics. The pseudo-random sequence generator and the IIR filter are implemented in software on the microcontroller. A triac is used as the power switch and a zero-crossing detector is used to generate the firing pulses in synchronism to the ac supply zero crossings. The firing angle can be adjusted to reduce the dc current component in inductive loads.

CONTENTS

LIST OF FIGURES

LIST OF ABBREVIATIONS

RFI	radio frequency interference
ICC	integral cycle control
EMI	electro-magnetic interference
PFC	power factor correction
RMS	root mean square
PF	power factor
THD	total harmonic distortion
BRM	binary rate multiplier
ZCD	zero crossing detector
PPI	programmable peripheral interface
PIPO	parallel-in/parallel-out
IIR	infinite impulse response
RAM	random access memory
LED	light emitting diode
DIP	dual in-line package
PCB	printed circuit board

LIST OF SYMBOLS

α	triac firing angle
ϕ	load power factor angle
$v(t)$	ac supply input voltage
$v_L(t)$	load voltage
$i_L(t)$	load current
i_h	harmonic component of current
ψ	phase angle between supply voltage and harmonic
V_{RMS}	root mean square value of voltage
I_{RMS}	root mean square value of current
T_0	ac cycle time period
f_0	ac supply frequency
n_{on}	number of on cycles
n_{off}	number of off cycles
t_{on}	period of on cycles
t_{off}	period of off cycles
N	number of cycles in the total control period
D	duty cycle of integral cycle controller
T	total control period of on and off cycles
L	number of switching patterns in ICC

Chapter 1
INTRODUCTION

1.1 Background

Low cost controllers for controlling ac power delivered to the load generally use a triac and phase angle switching or integral cycle switching [1]. Phase angle switching refers to a technique that provides a means of varying power to a load by altering the firing angle of the triac. This technique produces higher order harmonics and high inrush current while switching on. It also generates radio frequency interference (RFI). In integral cycle control (ICC), power is applied for an integer number of cycles of the power frequency f_0 and then removed for an integer number of cycles. It is suitable for loads with inertia - like motors and heaters. As the switch is closed at the zero crossing of the supply voltage, there will be low inrush current, but it introduces low frequency (sub-synchronous) and high frequency (super-synchronous) components affecting the distribution power supply line. These two problems can be reduced by using proper switching strategy.

For inductive loads, if the conduction is not initiated at the correct point in the voltage wave, there will be a large dc offset in the load current which could be as high as double the normal current and it may cause magnetic saturation effects in the inductive load. The current in an inductive load subjected to sinusoidal supply voltage is given by

$$i = \frac{V_m}{Z}\left[\sin(wt-\phi) - \sin(\alpha-\phi)e^{\frac{R}{\omega L}(\alpha-wt)}\right] \tag{1.1}$$

where $V_m \sin\omega t$ is the supply voltage, $Z\angle\phi$ is the load impedance, and α is the triac firing angle with respect to the voltage zero crossing. The second term in above expression represents the transient dc offset. This term could add or subtract from the first peak of the first term depending upon the value of α chosen. This dc current offset component can be reduced by adjusting the triac firing angle α closer to the load power factor angle ϕ [2] [3].

The source impedance causes drop in the supply voltage due to current flow. This impedance is inductive and increases with frequency. The higher the frequency component of current, greater is the distortion in voltage waveform. On the other hand, capacitive impedance reduces with frequency [4]. The combined effects may be listed as the following.

(i) At low frequencies, impedance of the ac power source is determined by the low impedance of transformers and transmission lines.

(ii) At high frequencies, the source impedance is determined by the low capacitive impedance of power factor correction capacitors (PFC).

(iii) For intermediate range frequencies, both the capacitive and inductive effects are present and may result in very high impedance. A small harmonic current within this frequency range can give a very high and undesirable harmonic voltage due to resonance.

Harmonic distortion in power supply affects the electrical equipment differently depending on their method of operation. Domestic lights and heaters are not affected by harmonics whereas induction motor windings are overheated by harmonics leading to insulation degradation and loss of service life. Also some of the equipment may need accurate voltage waveshape and they malfunction if harmonics are present. In power supply systems, substation transformers and power factor capacitors are most affected by harmonics. Distorted current waveforms in transformers can cause extra heating that reduces its service life. Capacitors may get damaged due to excessive heating of dielectric caused by harmonics in the voltage supply.

The sub-synchronous components add to the rms current, but do not improve average power that results in degraded power factor [5]. They cause a voltage drop in the source impedance resulting in low-frequency supply side voltage components, and introducing flicker on the supply bus. The super-synchronous components cause excess core loss in the supply transformer and may cause communications interference. Hence an ac power controller is needed which reduces the sub-synchronous and super-synchronous components while delivering power to the load.

1.2 Project Objective

The objective of this project is to develop a microcontroller-based controller for controlling the ac power delivered to load in fine control steps, using integral cycle

control by employing a switching strategy to reduce the sub-synchronous and super-synchronous components so that the supply voltage does not get distorted. The prototype developed has to be tested for operation under the condition of wide variation in the power supply voltage, frequency, and waveshape.

1.3 Report Outline

Chapter 2 provides a review of some of the earlier reported switching techniques for ac power control with detailed analysis of integral cycle control method. Chapter 3 covers the design of the controller circuit for integral cycle control. Chapter 4 describes the experimental set-up and test results. Summary of work done and conclusion is presented in the last chapter.

Chapter 2
POWER CONTROL TECHNIQUES

The power delivered to a single-phase ac load can be smoothly controlled by using a bidirectional switch such as triac. The controllers are generally based on phase controlled switching or integral cycle switching.

2.1 Phase Control Switching

This is a widely used method to control the average power delivered to the load through triac. In this method, the triac conducts for a fraction of each half cycle depending on the firing angle [1]. Fig. 2.1 shows the circuit diagram used to control ac power delivered to the load. Here the triac is triggered at some non-zero point in both positive and negative ac half cycles. Assuming the input voltage to be

$$v(t) = V_{\mathrm{m}} \sin(\omega t) \tag{2.1}$$

For resistive load, with input supply voltage $v(t)$ and triac firing angle α, the load voltage can be expressed as a Fourier series

$$V_{\mathrm{L}}(t) = a_0 + \sum a_n \cos n\omega_0 t + \sum b_n \sin n\omega_0 t \tag{2.2}$$

The output voltage contains only odd harmonics of the fundamental and the Fourier coefficients [1] are given as

$$a_0 = 0 \tag{2.3}$$

$$a_1 = \frac{V_{\mathrm{m}}}{2\pi}(\cos 2\alpha - 1)$$

$$b_1 = \frac{V_{\mathrm{m}}}{2\pi}\left[\sin 2\pi + 2(\pi - \alpha)\right]$$

and n^{th} harmonic components are given as

$$a_{n=3,5,7....} = \frac{V_{\mathrm{m}}}{2\pi}\left[\frac{2}{n+1}\{\cos(n+1)\alpha - 1\} - \frac{2}{n-1}\{\cos(n-1)\alpha - 1\}\right] \tag{2.4}$$

$$b_{n=3,5,7...} = \frac{V_{\mathrm{m}}}{2\pi}\left[\frac{2}{n+1}\sin(n+1)\alpha - \frac{2}{n-1}\sin(n-1)\alpha\right] \tag{2.5}$$

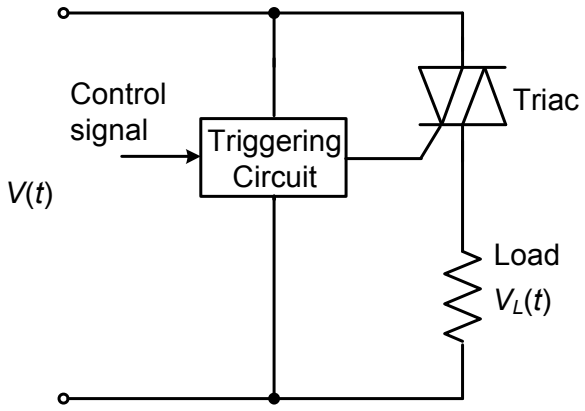


Fig. 2.1 Ac power control using triac [1].

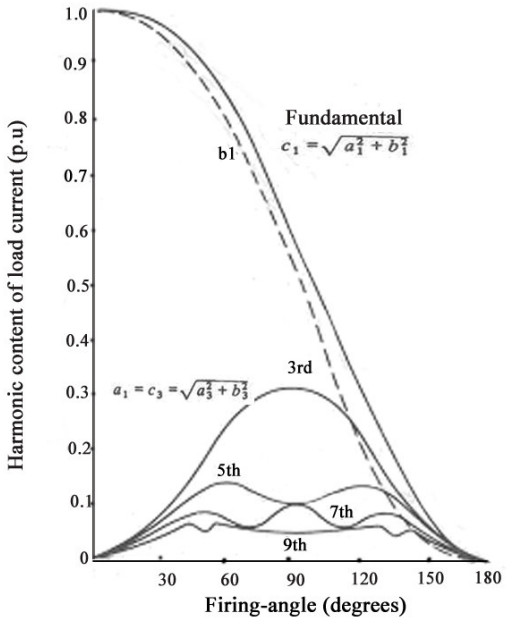


Fig. 2.2 Harmonic content of load current vs. firing angle from [1].

For resistive load, wave-shape of the load current is same as that of the load voltage. Fig. 2.2 shows the plot of the harmonic content of the load current as a function of α. At smaller firing angles the contribution of higher harmonics is negligible. At $\alpha = 0^0$, the load voltage is sinusoidal and therefore contains no higher harmonic components. However, at $\alpha = 90^0$, the third harmonic component is about half the fundamental component and the fifth and seventh harmonics also become significant.

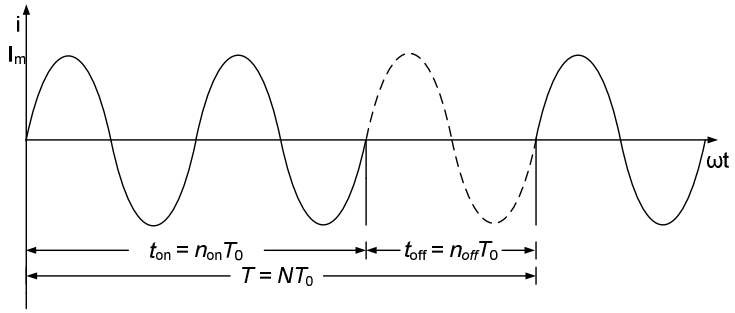


Fig. 2.3 Integral cycle waveform showing on/off cycles.

The main disadvantage of using phase control in triac applications is the generation of electromagnetic interference (EMI). Each time the triac is fired, the load current rises from zero to the load–limited current value in a very short time. The resulting di/dt generates a wide spectrum of noise which may interfere with the operation of nearby electronic equipment unless proper filtering is used.

2.2 Integral Cycle Control Switching

In this technique, a triac is triggered at the zero crossing instant of the sinusoidal voltage. This reduces the turn-on transients and EMI. The power control is achieved by passing and blocking the cycles applied to the load through triac. A typical waveform for integral cycle control is shown in Fig. 2.3. For a sinusoidal input supply voltage,

$$v(t) = V_m \sin \omega t \tag{2.6}$$

with time period $T_0 = 2\pi/\omega$. If the input is connected for n_{on} cycles and disconnected for n_{off} cycles, then the controller on-time $t_{on} = n_{on}T_0$, and controller off-time $t_{off} = n_{off}T_0$. The time period of the controlled output voltage $T = t_{on} + t_{off} = (n_{on} + n_{off})\, T_0$.

The rms value of the input voltage $V_{RMS} = V_m / \sqrt{2}$. The rms value of the output voltage is given as

$$V_{L(RMS)} = \left[\frac{1}{T}\int_0^T [v_0(t)]^2\, dt\right]^{0.5}$$

$$= \left[\frac{V_m^2}{\omega T}\int_0^{\omega t_{on}} \sin^2 \omega t\; d(\omega t)\right]^{0.5}$$

$$= \left[\frac{V_m^2}{\omega T}\int_0^{\omega t_{on}}\left[\frac{1-\cos 2\omega t}{2}\right]d(\omega t)\right]^{0.5}$$

$$= \left[\frac{V_m^2}{2\omega T}\left[(\omega t_{on})-\frac{\sin 2\omega t_{on}}{2}\right]\right]^{0.5} \quad (2.7)$$

Since $\omega t_{on}= 2\pi, 4\pi, 6\pi, 8\pi, 10\pi,\ldots..,$ sin $(2\omega t_{on}) = 0$. Hence the output is given as

$$V_{L(RMS)} = \frac{V_m}{\sqrt{2}}\sqrt{\frac{t_{on}}{T}}$$

which can be written as

$$V_{L(RMS)} = V_{RMS}\sqrt{D} \quad (2.8)$$

where $D = n_{on} / (n_{on} + n_{off})$ is the duty cycle of the integral cycle control. Power factor is given as

PF = (output load power) / (input volt – ampere)

$$= \frac{I_{L(RMS)}^2 R_L}{V_{RMS} I_{RMS}} \quad (2.9)$$

The input supply current is the same as the load current, hence $I_{(RMS)} = I_{L(RMS)}$. Thus the power factor is given as

$$PF = \frac{V_{L(RMS)}}{V_{RMS}} = \sqrt{D} \quad (2.10)$$

The repetition period of the load waveform is N cycles ($N = n_{on} + n_{off} = T / T_0$) and the instantaneous load voltage $v_L(\omega t)$ in terms of ωt is given as

$$\begin{aligned} v_L(\omega t) &= V_m \sin \omega t, && 0 \le \omega t \le 2\pi n_{on} \\ &= 0 && 2\pi n_{on} \le \omega t \le 2\pi N \end{aligned} \quad (2.11)$$

Fourier coefficients a, b for integral cycle load voltage of n_{on} conducting cycles followed by an n_{off} off cycles are given by [1]

$$a_0 = \frac{1}{\pi}\int_0^{2\pi n_{on}} v_L(\omega t)\, d(\omega t)$$

$$= 0 \quad (2.12)$$

$$a_n = \frac{1}{\pi}\int_0^{2\pi n_{on}} v_L(\omega t)\cos n\omega t\, d(\omega t)$$

$$= \frac{V_m N}{\pi(N^2 - n^2)}[1-\cos(2\pi n_{on})] \quad (2.13)$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi n_{on}} v_L(\omega t)\sin n\omega t\, d(\omega t)$$

$$= \frac{V_m N}{\pi(N^2 - n^2)}[-\sin(2\pi n_{on})] \tag{2.14}$$

The amplitude c_n of the n^{th} harmonic component, for $n \neq N$, is found to be

$$c_n = \sqrt{a_n^{\,2} + b_n^{\,2}}$$

$$= \frac{2V_m N}{\pi(N^2 - n^2)}[\sin(\pi n_{on})] \tag{2.15}$$

The above equation shows that an integral cycle waveform contains even order harmonics as well as odd order harmonics, depending on the values of n_{on} and N. The phase angle between the supply voltage and the n^{th} current harmonic is given by

$$\psi_n = \tan^{-1}\frac{a_n}{b_n}$$

$$= \tan^{-1}\left[\frac{1-\cos(2\pi n_{on})}{-\sin(2\pi n_{on})}\right]$$

$$= \tan^{-1}\left[\frac{\sin(\pi n_{on})}{-\cos(\pi n_{on})}\right]$$

which after simplification gives

$$\psi_n = \pi - \frac{\pi n_{on}}{N}\ , \qquad n < N$$

$$= \frac{\pi n_{on}}{N} - \pi\ , \qquad n > N \tag{2.16}$$

Thus, integral cycle waveforms contain super-synchronous harmonic components of the supply frequency (when $n > N$) as well as sub-synchronous harmonic components also (when $n < N$). The subsynchronous frequency components have a serious disadvantage in most of the applications since it may exceed the value of the supply frequency component [1]. To avoid setting up sub-harmonic resonances in power supply system or to avoid natural frequencies of motor loads, proper choice of control period N is necessary.

2.3 Analysis of integral cycle control

Chang et al. [5] have reported the impact of switching strategies on power quality. They treated the ICC as the modulator where ac sinusoidal supply is modulated by square wave type signal. The load current $i_L(t)$ is the product of sine wave $i(t)$ and the modulating square signal $m(t)$ which can be treated as additions of a series of

phase shifted square function $s(t)$ with duty cycle $D = n_{\text{on}} / (n_{on} + n_{off})$ and period $T = (n_{on} + n_{off})\ T_0$ where T_0 is the period of supply cycle. To find the signal $m(t)$, consider that the single cycle is 'on' out of $(n_{on} + n_{off})$ cycles.

Let $\omega_{\text{d}} = 2\pi / T$ and $p = 1 / (n_{on} + n_{off})$. Fourier series expression for the single on cycle is given as

$$s(t) = \sum_{k=-\infty}^{\infty} A_k e^{jk\omega_{\text{d}}t} \tag{2.17}$$

where

$$A_k = \frac{1}{T}\int_0^{pT} s(t)e^{-jk\omega_{\text{d}}t} \quad = \frac{1}{T}\left[\frac{e^{-jk\omega_{\text{d}}t}}{-jk\omega_{\text{d}}}\right]_0^{pT} = \frac{1}{k\pi}e^{-jkp\pi}\sin(kp\pi) \tag{2.18}$$

$$A_0 = \lim_{k\to 0}\frac{\sin(kp\pi)}{k\pi} = p \tag{2.19}$$

Therefore the single on-cycle waveform can be written as

$$s(t) = p + \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} \frac{e^{-jpk\pi}}{k\pi}\sin(pk\pi)e^{jk\omega_{\text{d}}t} \tag{2.20}$$

After adding all the phase shifted functions for the n_{on} cycles, we get

$$m(t) = \frac{n_{\text{on}}}{n_{\text{on}} + n_{\text{off}}} + \sum_{l=1}^{n_{\text{on}}} e^{-j(2\pi/\omega_0)P_l t} \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} A_k e^{jk\omega_{\text{d}}t} \tag{2.21}$$

The coefficient A_{k} can be zero or nonzero depending on the selected switching strategy. The load current $i_{\text{L}}(t)$ can be expressed as

$$i_{\text{L}}(t) = m(t)i(t)$$

where $i(t)$ is the load current with the resistive load directly connected to the supply, and is given as

$$i(t) = I_{\text{m}} \sin \omega t = I_{\text{m}}\left(\frac{e^{j\omega t} - e^{-j\omega t}}{2j}\right) \tag{2.22}$$

Hence the load current is given as

$$i_L(t) = \left[\frac{jn_{\text{on}}}{2(n_{\text{on}} + n_{\text{off}})}(e^{-j\omega_0 t} - e^{j\omega_0 t}) + \sum_{k=-\infty}^{+\infty} \frac{A_k}{j2}(e^{j(k\omega_{\text{d}} - \omega_0)t} - e^{j(k\omega_{\text{d}} + \omega_0)t})\right] I_{\text{m}} \tag{2.23}$$

Thus, the load current $i_{\text{L}}(t)$ contains $\omega_0 \pm k\omega_{\text{d}}$ frequency components. Some frequency components can be deleted or their amplitude can be attenuated by using proper switching strategy. From the above equation we can conclude that

- The minimum frequency of harmonic is f_0 / (n_{on} + n_{off}) and components occur at integer multiples of this frequency.
- There are no integer harmonics above f_0 component.
- The amplitude of fundamental component (f_0) remains constant at I_m n_{on} / (n_{on} + n_{off}), independent of the switching strategy and the component has no phase shift.
- The amplitude of all the frequency components other than f_0 depends on switching strategy.

Sub-synchronous harmonics are the frequency components of the voltages and currents below fundamental component f_0. They are present at integer multiple of minimum frequency f_0 / (n_{on} + n_{off}). These components get added to rms current but not added to average power and thus degrade the power factor. They also cause a voltage drop in the supply impedance resulting in low frequency supply-side voltage components and the flicker on the supply side bus. Super-synchronous harmonics are the frequency components that occur above f_0 and at integer multiples of f_0 / (n_{on} + n_{off}). These components are also referred as interharmonics as they may occur at frequencies between f_0, $2f_0$, $3f_0$,….These high frequency components cause excess core loss in the supply transformer.

As the supply voltage is maximum at the fundamental frequency component (f_0), only the load current component at f_0 will give the average power. Choosing the different patterns of 1's and 0's, where 0 means the power cycle is blocked and 1 means the power cycle is passed on to the load gives the switching strategy for ICC. Thus for a given duty cycle D, there will be L different switching patterns given as

$$L = C_{n_{on}}^{n_{on}+n_{off}} = \frac{(n_{on}+n_{off})!}{n_{on}!\,n_{off}!} \tag{2.24}$$

The load current will have an impact on the electric power quality of the supply in the form of total harmonic distortion and the losses in the supply transformer due to I^2R and core losses. The core losses will be due to high frequency components of load current. In addition to this, it will have an impact on the supply side also in the form of flicker caused by voltage fluctuations.

The total harmonic distortion (THD) of the load current is given as $\mathrm{THD} = \sqrt{\sum_h I_h^{\,2}} \;/\; I_0$ where I_h refers to load current component at all harmonics except

f_0 component and I_0 is the power frequency component. The THD is the function of the duty cycle D and can be expressed as

$$\text{THD} = \frac{I_{\text{h(RMS)}}}{I_0} = \frac{\sqrt{D - D^2}}{D} = \sqrt{\frac{1 - D}{D}} \tag{2.25}$$

2.4 Different switching strategies

McCarthy and Danesh [6] reported a circuit based on binary rate multiplier (BRM). A BRM has two inputs: a pulse train of frequency f acting as a clock and parallel binary number C that controls the number of output pulses. The output is another pulse train whose average frequency is given by

$$f_{\text{a}} = \frac{f}{2^p} \sum_{r=0}^{p-1} C_r 2^r \tag{2.26}$$

where $C = (C_{\text{p-1}} C_{\text{p-2}} \ldots .. C_1 C_0)$, p = number of bits in C, and $C_{\text{r}} = 0$ or 1. Pulses generated at the zero crossings of the supply voltage waveform serve as the clock input to BRM. The BRM output is also a train of pulses coincident with supply zero crossings having average frequency proportional to digital control signal C. These pulses are amplified to trigger the triac at the beginning of the appropriate half cycles. The mean load current is thus proportional to C. Fig. 2.4 shows a schematic of the circuit. The zero crossing pulses from squaring circuit are given to Schmitt inverter to condition the edges of the waveform. Another six inverters in cascade gives out two square waves with two different and small delays. These waveforms are used in the monostable to produce pulses corresponding to positive going and negative going zero crossings. The output pulse width is determined by externally connected capacitor. The monostable triggers on the positive edge of B if either A1 or A2 is high, and on negative edge of A1 if A2 and B are high. The waveforms at different points are also shown in the figure. The negative going pulse output from the monostable is used as clock input to BRM. BRM output pulses are used to drive the triac gate.

Nieznadski [7] used an accumulator for distributing on and off cycles optimally for minimizing the low frequency ripple in the output power. If the number of on cycles n_{on} divides the total cycle period T, the output pulse train will be regular with equal spacing of T / n_{on} clock periods and each pulse occur at $\theta_{\text{i}} = i (T / n_{\text{on}})$. However usually n_{on} does not divide T and the output pulse train may be

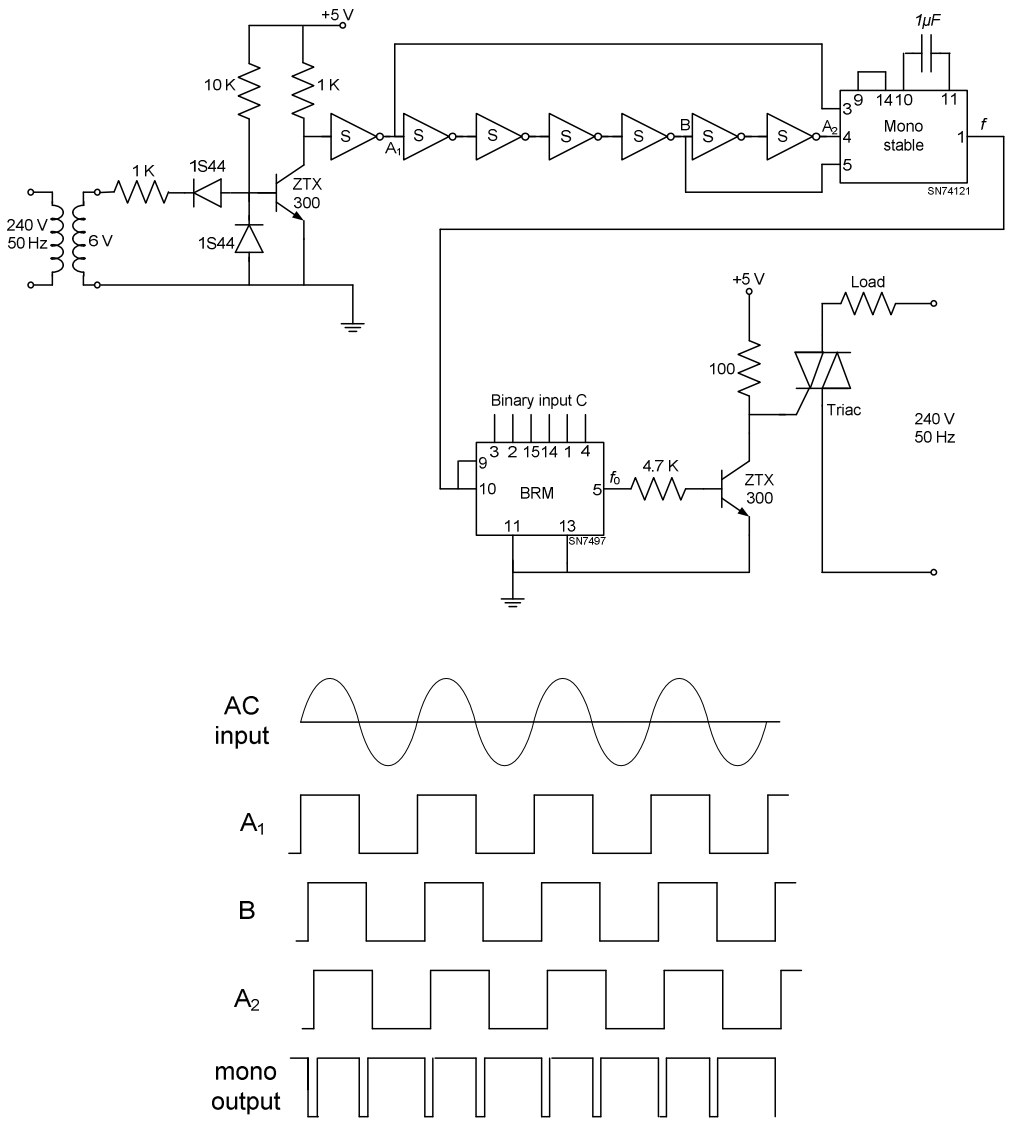


Fig. 2.4 Binary rate multiplier based circuit for ICC in [4] and associated waveforms.

obtained by rounding the integer values of pulse instant as θ_i = rnd (i (T / n_{on})). The accumulator as shown in Fig. 2.5 consists of a parallel adder (74LS283) and a parallel-in / parallel-out (PIPO) register (74LS195). Two-input AND gate transforms the non-return-to-zero carry pulse train into the return-to-zero output pulse train and a flip-flop is used for glitch-free operation. The repetition frequency of the carry pulses is $\upsilon = n_{on}$ / T. In 74LS195, when PE is low, the shift register appears as four

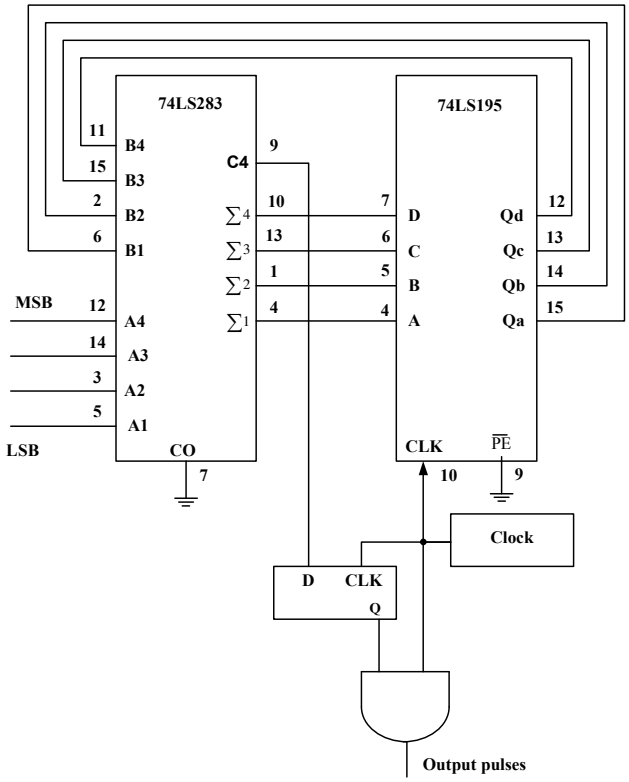


Fig. 2.5 Accumulator using adder and shift register for uniform distribution of pulses as given in [5].

common clocked D flip-flops. The data on parallel inputs A, B, C, D is transferred to respective Q_a, Q_b, Q_c, Q_d outputs following the low-to-high clock transition.

In the circuit of [5], the accumulator performs, at each discrete time instant k, modulo-M addition of the input number n_{on} and the previous result of addition, that is

$$a_k = a_{k-1} \underset{M}{+} n_{on} \tag{2.27}$$

where, M is the capacity of the accumulator ($M = 2^m$: m is the bit size of register and adder). The above equation can be rewritten as

$$a_k = a_{k-1} + n_{on} \qquad \text{for } a_{k\text{-}1} + n_{on} < M \tag{2.28}$$

$$a_{k-1} + n_{on} - M \qquad \text{for } a_{k\text{-}1} + n_{on} \geq M$$

$$a_k = a_0 + kn_{on} - iM \tag{2.29}$$

where i is the number of carries (i.e., output pulses) counted from 0^{th} time instant to k^{th} time instant. The output pulse number i occurs at time $k = \theta_i$ if and only if $a_{k\text{-}1}$ +

$n_{on} \geq M$. Hence $a_k \leq n_{on} - 1$ *for* $k = \theta_i$. Considering that all states are nonnegative, we get $0 \leq a_0 + \theta_i \times n_{on} - iM \leq n_{on} - 1$, which can be rearranged as

$$\frac{iM - a_0}{n_{on}} \leq \theta_i \leq \frac{iM - a_0 - 1}{n_{on}} + 1 \tag{2.30}$$

Since θ_i is an integer and difference between left and right side estimates of θ_i is less than unity, the above equation uniquely determines θ_i for given n_{on} and a_0 where a_0 is the initial state (i.e. the number loaded to the register by the $k = 0$ pulse).Thus the accumulator generates optimum pulse trains for the whole range of input numbers n_{on}.

Glaser et al. [8] reported a cycle skipping or integral cycle control circuit using pseudo-random generator with digital comparator as shown in Fig. 2.6. This produces the random binary bit stream which has data rate equal to ac power line frequency and is used to turn on / turn off the switch that controls the power applied to load. The data stream is generated such that the probability of any bit being equal to one is equal to the desired fraction of full power. They tested the scheme for electrical loads such as kitchen range with electrical resistance burners wherein thermal time constant is much longer than the period of ac line. They reported that the fine power control resolution is achieved without requiring long control period and the visible flicker due to pulsating ac line current is reduced. At the beginning of each line cycle in this circuit, zero crossing detector sends signal to random number generator which generates random data stream with a uniform distribution. The output of random number generator is compared with the desired fraction *D*. If random number is less than *D*, the output of comparator is one and the switch turns on at the beginning of line cycle and will remain on for one full cycle. Thus switch will be on during a fraction *D* of the time giving the number of cycles needed to apply the desired power to load. Due to randomness, very high resolution in power control can be achieved. Another advantage is that perceptible flicker due to pulsating ac line current is reduced, both in visibly radiant loads and in electric illumination devices in close proximity to the load.

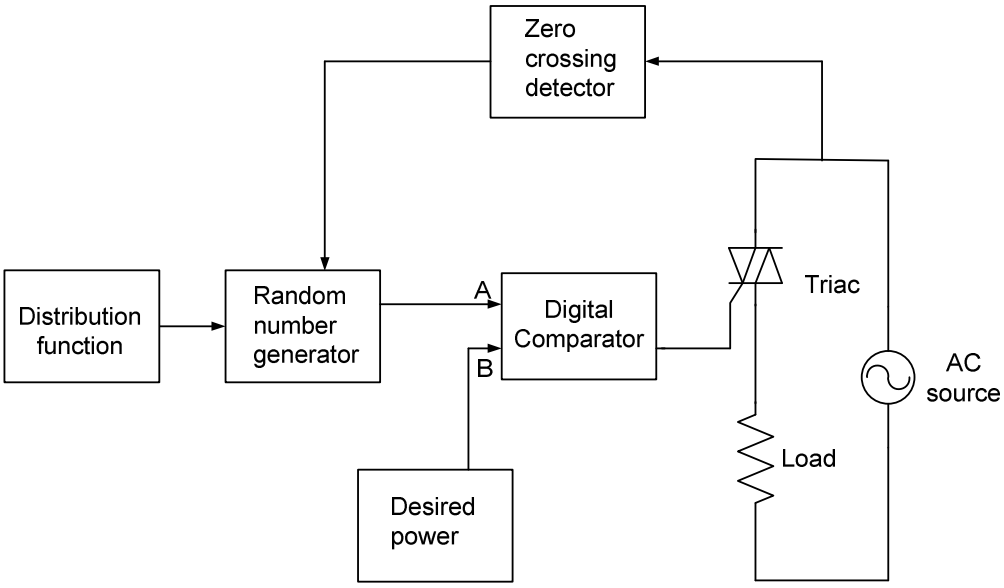


Fig. 2.6 ICC with uniform on/off cycle distribution [6].

2.5 Integral cycle controller for inductive loads

Rahman et al. [2] reported a circuit for controlling power in inductive loads using integral cycle method which automatically adjusts the firing angle of triac to eliminate undesirable dc component in current of inductive loads. This dc offset in load current could be as large as double the normal current and likely to cause magnetic saturation effects in the inductive load. The initial conduction started with firing angle α = 90° and subsequently it is made equal to power factor angle ϕ thereby firing triac when current is zero in each burst of on cycles.

El-Bolek and Abd-El-Hamid [3] reported a microprocessor-based system shown in Fig. 2.7 for controlling the power applied to inductive loads through integral cycle switching. After choosing the initial triac firing angle (α), microprocessor adjusts the firing angle (α) depending on the load power factor angle ϕ at every burst of conduction cycles. This helps in removing the dc current offset component that will appear in load current depending on the triac firing angle. The inductive load is connected to ac supply via triac. The firing pulses for triac are produced and controlled by microprocessor (8086). Zero-crossing detectors ZCD1 gives square pulses synchronous to ac supply zero crossings and ZCD2 produces square pulses corresponding to load current taken through 1 Ω resistor connected in series with inductive load. These signals are fed to microprocessor through 8255

PPI. The triac firing pulses produced by microprocessor are given to triac driver through 8255. A driver is used to amplify the power level of the triggering pulses to ensure triggering of any triac. The voltage and current waveforms are also shown in

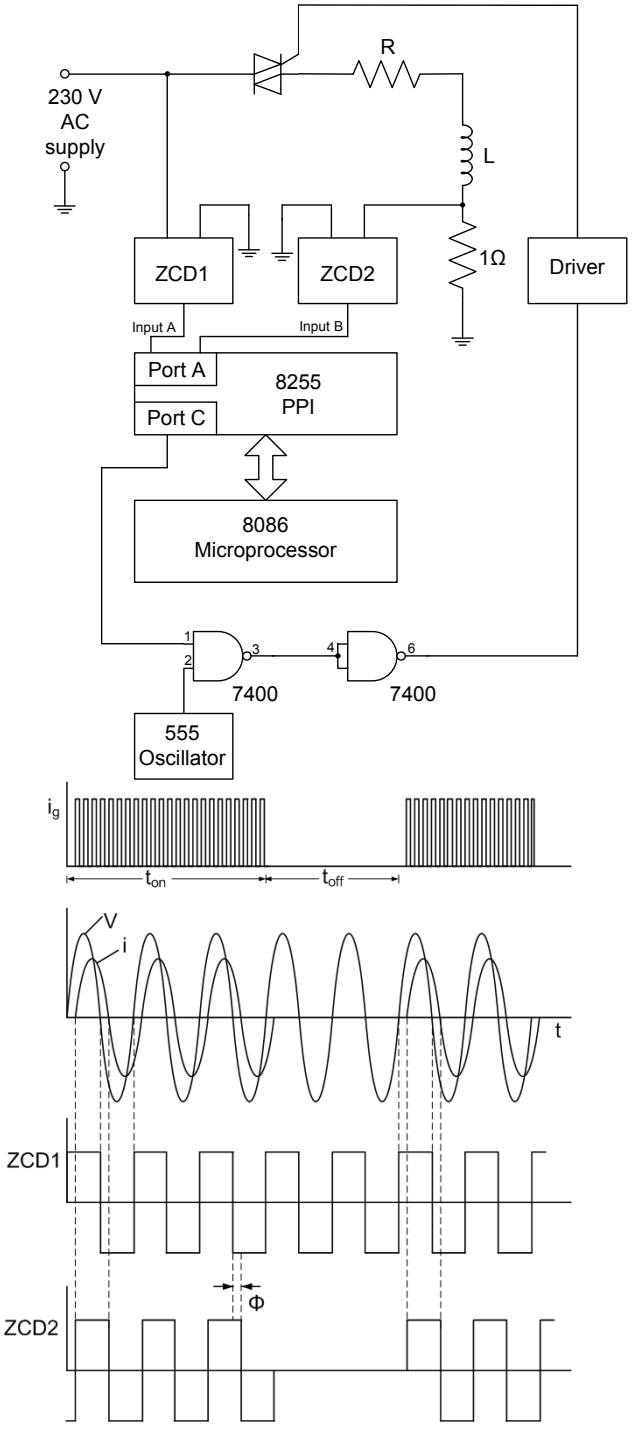


Fig. 2.7 Microprocessor based self adjusting system of [8] and the voltage and current waveforms.

Fig. 2.7. The size of the pulse transformer used in triac driver to isolate power circuit from microprocessor circuit is reduced by using high frequency carrier gating. This is done by changing long triggering pulses into series of short pulses using AND gate and 20 kHz oscillator.

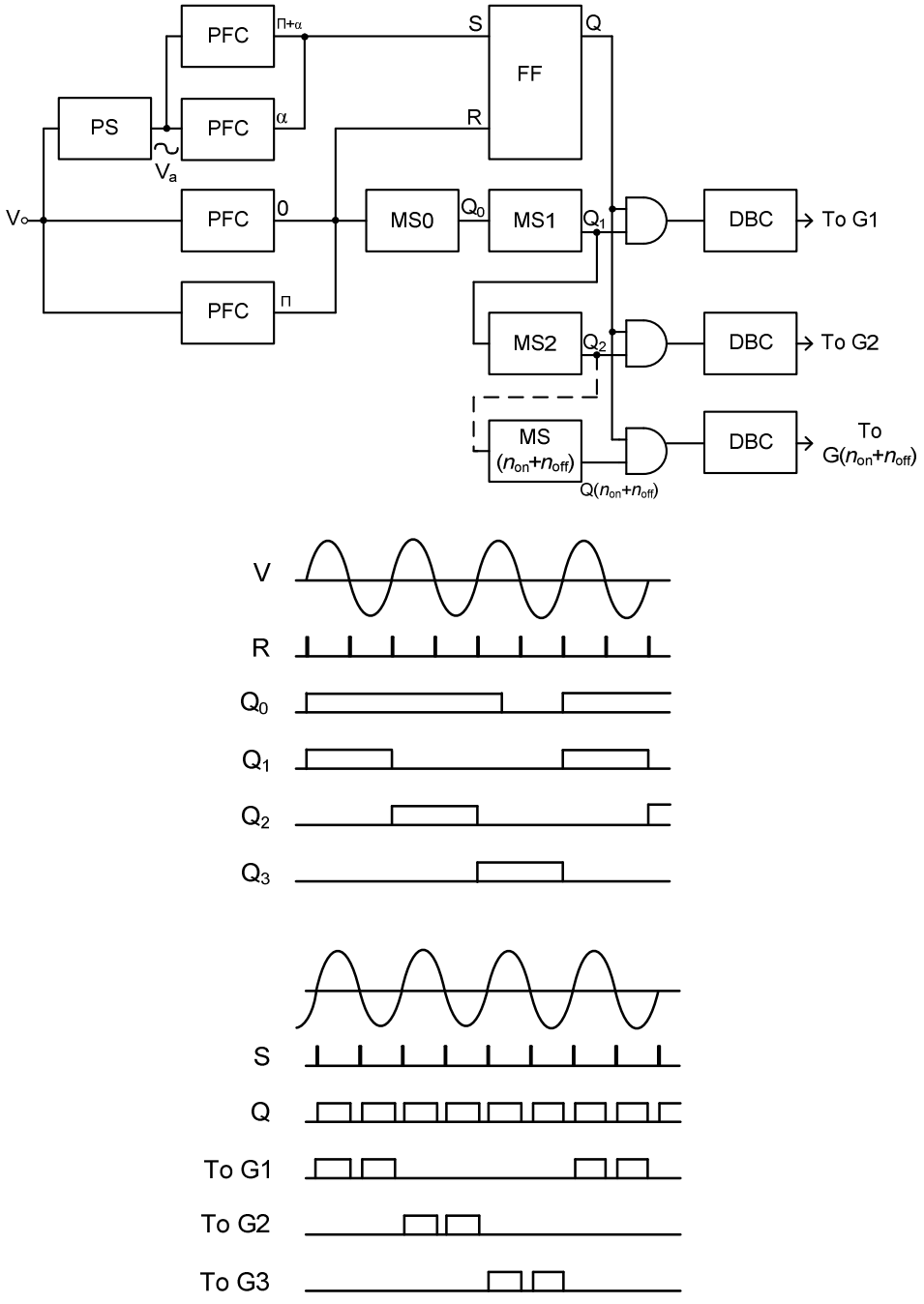


Fig. 2.8 Controller using phase shift network of [9] and associated waveforms.

Asghar [9] reported the discontinuous phase controlled switching which is the combination of phase controlled switching and integral cycle switching, that reduces higher order harmonics and high inrush currents, eliminates radio frequency interference. This technique can be used for controlling power delivered to electric heater which is the resistive load, made of several parallel resistors as shown in Fig. 2.8. This controller circuit uses RC phase-shifter (PS) circuit that generates a phase-shifted ac signal (V_α). This signal is then fed to a pulse forming circuit (PFC) which gives a sharp positive pulse at positive and negative zero-crossing instants. Output Q of flip-flop remains high between α to β and ($\alpha + \beta$) to 2π. A non-retriggerable monostable MS0 sets total or ($n_{on} + n_{off}$) period, while retriggerable monostables (MS1, MS2,…MS($n_{on} + n_{off}$)) enable the trigger pulses to reach the gates of triac for n_{on} cycles sequentially. The waveforms at different points are also shown in Fig. 2.8. The load resistance R is arranged as ($n_{on} + n_{off}$) number of parallel resistances R_1 such that $R_1 = (n_{on} + n_{off})\ R$ where n_{on} and n_{off} represents number of on and off cycles. The maximum power P_{max} can be obtained by switching all resistances R_1 continuously at $\alpha = 0$. For the minimum output power, only one R_1 is switched at a time sequentially for one cycle.

For fan-type loads such as single phase induction motors (SPIM), performance of the proposed controller improves when technique is applied to control main winding voltage only [10]. Speed control by a regulator based on ac phase controlled switching (using resistance or inductor in series) causes significant power wastage and lowers power factor (PF). It also causes problems such as double-supply-frequency pulsation of torque, series of odd-order voltage harmonics and pulsations at even multiples of supply frequency. High order harmonics cause more iron losses, noise from the core and reduced overall efficiency.

2.6 ICC using random sequence generator and IIR filter

A microcontroller-based power control board that allows both phase angle switching and integral cycle switching [11] was developed at IIT Bombay. Low pass IIR filter with pseudo-random number generator was used to add the randomness while outputting the on cycles with the objective of distributing the sub-synchronous components approximately uniformly over f_0 / L to $0.4\ f_0$ where L is the sequence length of the pseudo-random sequence generator. An IIR filter was used to keep

track of the effective duty cycle, and the sequence was modified to 0 or 1 in order to keep the duty cycle in a specified tolerance about the desired value. Control of triac firing angle to limit the high inrush current in inductive loads was tried out in another project as reported in [12]. Here on cycles are outputted in a burst followed by off cycle period.

2.7 Project objectives

Based on the review of the work reported earlier, it may be concluded that a proper switching strategy in ICC helps in controlling and limiting the undesired sub-synchronous and super-synchronous current components. Further control of the firing angle is desirable in case of inductive load, to limit short-time dc components. Hence, the objective of the current project is to develop a controller combining both these features, and using a microcontroller in order to reduce the total number of components and to reduce the cost. As a specific application, it was decided to use it as a fan regulator.

Chapter 3
CONTROLLER DESIGN

3.1 Proposed technique

The project objective is to design an integral cycle controller for ac power which can be used as a fan regulator or controller of other single-phase ac loads with considerable internal inertia to mask the ripples in the power due to missing cycles. The controller circuit should have the means for inputting the duty cycle and the triac firing angle in initial cycle of burst to remove or reduce the transient dc offset. As the application does not require large memory, microcontroller AT89C2051 from Atmel [13] was selected to serve as the core of the controller circuit. This 20 pin IC has on-chip flash RAM of 2 KB, 2 ports (port 1: general purpose input / output pins; port2: multifunction pins), 2 timers, and can communicate over serial port.

Fan speed is controlled by varying the voltage applied to the fan motor using integral cycle switching. Triac [14] firing is synchronized with the zero crossings of ac supply voltage, by using a zero-crossing detector. The low-voltage microcontroller circuit is isolated from high-voltage triac circuit using an IC MOS3020 [15], a random-phase optoisolator with triac driver output.

The controller can be used with either of the two control schemes. In Scheme-1, all the on cycles are outputted in a single burst followed by off cycles. In Scheme-2, the conducting cycles are distributed over a control period. The uniform distribution of conducting cycles with control of the average duty cycle is to be achieved using a pseudo-random number generator and a digital low pass IIR filter, both realized on the microcontroller itself. The desired speed can be achieved by passing the cycles so that average of the cycles passed lies close to the duty cycle required for the desired speed.

To calculate the running average of the duty cycle, a low-pass IIR filter is implemented.

$$y(n) = (1-\beta)x(n) + \beta y(n-1) \tag{3.1}$$

where, $y(n)$ is running average after n^{th} cycle and $x(n)$ is the input to filter and represents the control for passing the n^{th} cycle. On and off cycles are represented as 1 and 0 as the values of the input $x(n)$ to the filter. The input to the filter, control $x(n)$, is decided by whether the previous average $y(n\text{-}1)$ is within the acceptable range of the running average. If previous average is below the range, input to the control is set to '1' and if it is above the range, control is set '0'. In case the average lies within the range, the control is decided by the random sequence $r(n)$. Hence the conditions on input $x(n)$ are given as

$$x(n) = \begin{cases} 0 & \text{if } y(n\text{-}1) > \text{desired output} + \text{tolerance} \\ 1 & \text{if } y(n\text{-}1) < \text{desired output} - \text{tolerance} \\ r(n) & \text{otherwise} \end{cases} \quad (3.2)$$

The pseudo-random binary sequence $r(n)$ has an average of 50 % 1's. This sequence is generated in the microcontroller by using feedback shift-register technique [16]. The 16-bit register is used with four taps at bits 4, 13, 15, and 16 for feedback. Bits at these feedback taps are exclusive-ORed and the resultant bit is shifted to LSB of the shift register. This gives a pseudo-random sequence of 0's and 1's with sequence length of 65535. The IIR filter is also implemented on the same microcontroller using 16-bit integer arithmetic.

3.2 Controller hardware

The controller circuit is shown in Fig. 3.1. The zero-crossing detector is designed to get the sync pulses required for triac triggering in phase angle switching as well as integral cycle switching. In the test model of the circuit, speed setting is done through 8 switches which inputs the duty cycle of ICC. The firing angle of the triac in fractional cycle control is set using another set of 4 switches. Firing of the triac is delayed in the first cycle of every sequence of on cycles using fractional cycle control and the remaining cycles are passed at the zero crossing instant. The power circuit consisting of the triac and load is isolated from the controller circuit by optoisolator. Each of the blocks is described in the following subsections.

3.2.1 Voltage supply and zero crossing detection

Two circuits were tested for obtaining the regulated +5 V dc for the circuit operation along with zero-crossing detector as shown in Fig. 3.2 and Fig. 3.3. Ac input supply

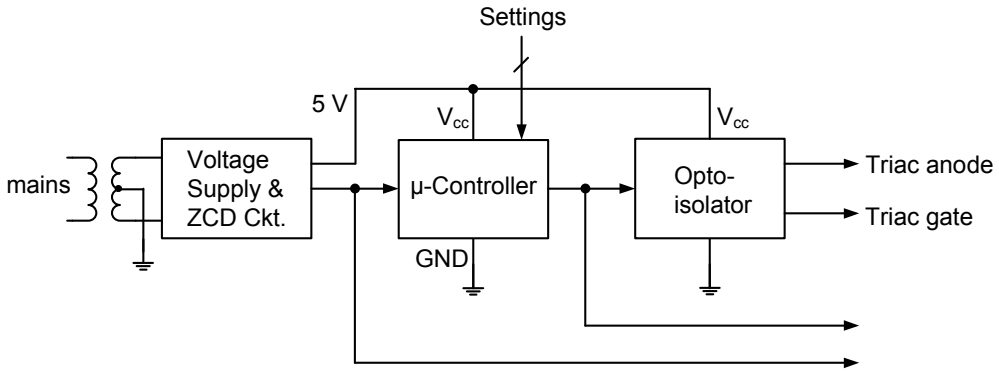


Fig. 3.1 A schematic of the controller circuit.

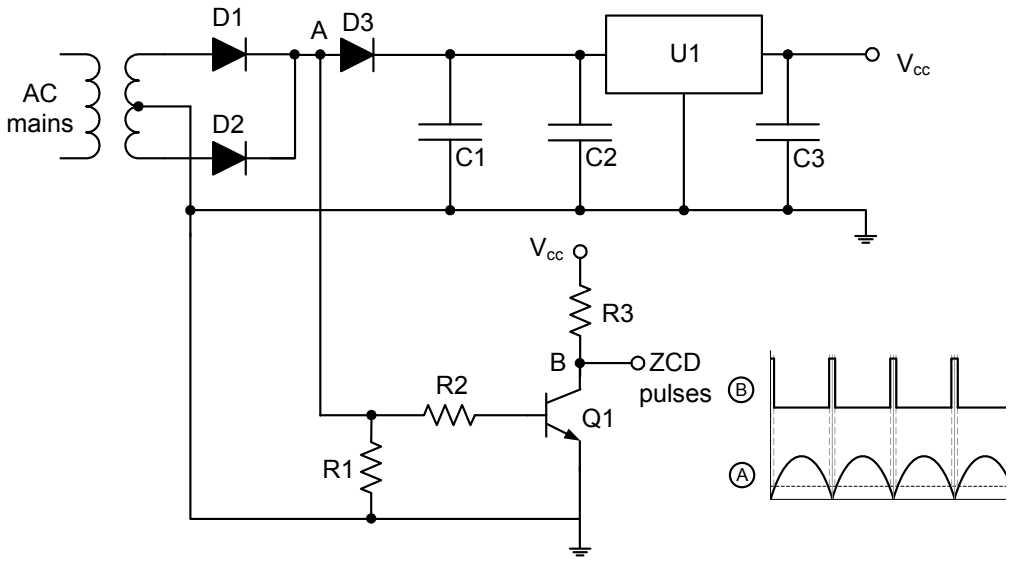


Fig. 3.2 Voltage supply and ZCD circuit (VS-ZCD-1).

voltage is stepped down to 12 V by transformer and applied to the full-wave rectifier formed by diodes D1and D2. The pulsating output voltage is filtered by capacitor C1 and fed to voltage regulator U1 which provides the 5 V regulated supply for the microcontroller. Capacitors C2 and C3 are used as decoupling capacitors at input and output of the voltage regulator respectively. Diode D3 is used to isolate the full-wave rectified waveform from the filtered dc. Full-wave rectified pulsating voltage is applied to base of the transistor. When the input voltage at base is more than the cut-in voltage of base-emitter junction of transistor, it starts conducting and goes into saturation by giving zero output. When input voltage is less than cut-in voltage, Q1 remain cut off and give high output. Thus Q1 conducts for most part of the ac

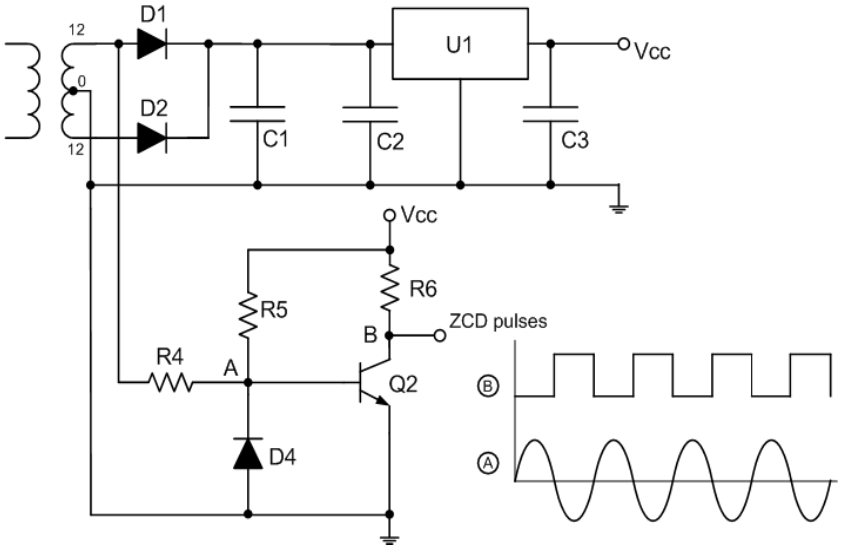


Fig. 3.3 Voltage supply and ZCD circuit (VS-ZCD-2).

cycle and remain off for very short duration giving a narrow pulse at each zero crossing of the input AC voltage.

In integral cycle control, a full ac cycle is turned on and off and hence we need only one of the two zero crossings. Hence, we used another circuit as shown in Fig. 3.3. This is basically a squarer circuit. In the positive half cycle, transistor Q2 conduct giving zero output and in negative half cycle Q2 remain cut off giving voltage nearly equal to V_{CC}. The rising edge of these pulses is used for controlling the triac. This circuit does not need the series diode D3 of Fig. 3.2.

3.2.2 Microcontroller circuit

As the integral cycle controller does not require a large amount of memory; the controller can be designed using the 20-pin microcontroller AT89C2051 which has on-chip programmable flash of 2 KB [13]. The microcontroller circuit with its associated components is shown in Fig. 3.4. In the experimental setup, the number of on/off cycles and triac firing angle may be set through DIP switches SW1 and SW2 interfaced to the microcontroller ports. The port pins P1.0 and P1.1 do not have internal pull-up and hence external pull-up is provided through resistors R11 and R12 respectively. The resistor R10 and capacitor C5 form the power-on reset for the microcontroller. The crystal XTAL with capacitors C6 and C7 is used for generating the clock by the on-chip oscillator. The microcontroller receives the sync pulses corresponding to the time instant of zero crossings on pin P3.5 and determines

whether the ac cycle is to be passed on to the load or not, by outputting pulses on pin P3.7.

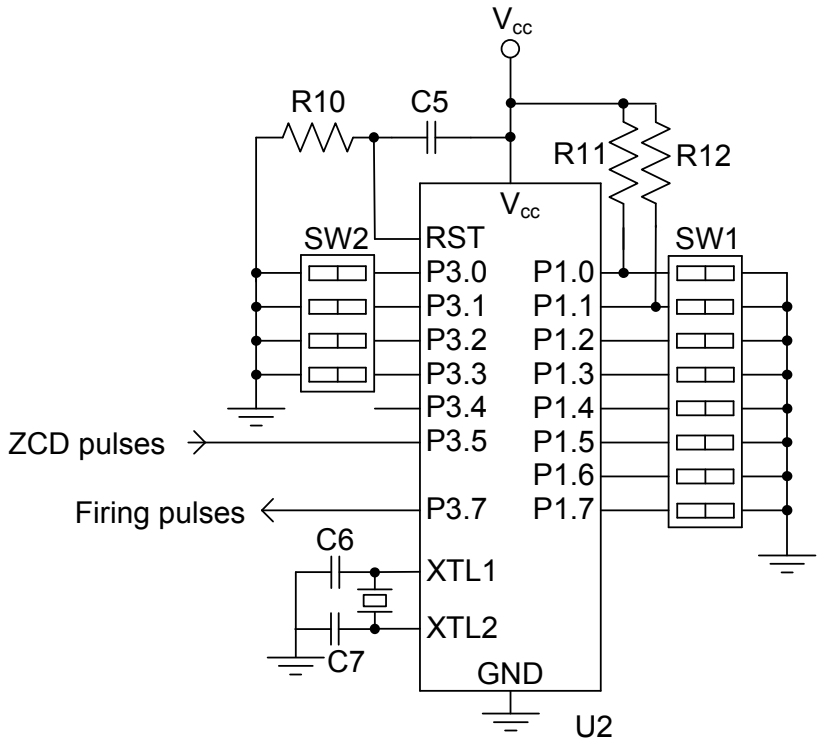


Fig. 3.4 Microcontroller with control inputs (SW1 and SW2).

For distributing the on cycles randomly over a control period, the digital low pass IIR filter and the pseudo-random sequence generator as discussed earlier are implemented in software.

3.2.3 Triac control with optical isolation

Triac is equivalent to two silicon controlled rectifiers connected in opposite directions with their gates shorted and it can conduct in the either directions, when a

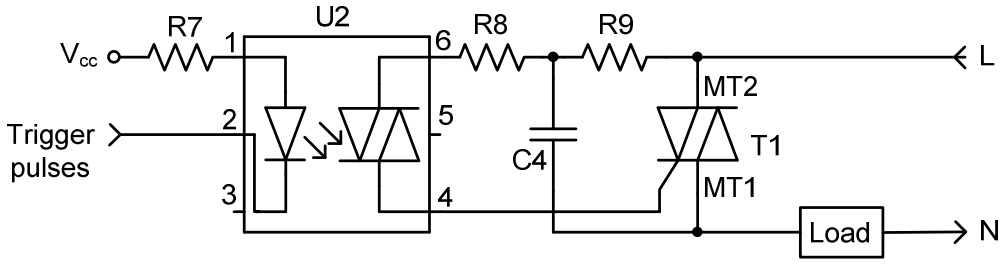


Fig. 3.5 Triac control with optical isolation.

pulse is given to its gate. The triac controller circuit is shown in Fig. 3.5. A low pulse from the microcontroller U3 (P3.7) switches on the LED inside triac driver U2 [14], which in turn trigger the triac on. Where inductive loads have to be controlled, a single short pulse at the zero crossing may be unsatisfactory as the current may not have risen to its sustaining value.

To ensure that the triac gets triggered in every ac cycle, the length of the pulse can be increased or a burst of high frequency pulse train may be used [1]. These pulses from the microcontroller are applied to the pin 2 (cathode of the LED) of the optoisolator and pin 1 (anode of LED) is connected to V_{cc} through resistor R7 which limit the current through the LED. The optoisolator having triac driver output drives the gate of the triac T1 and provide isolation between triac load circuit and controller circuit. Resistor R8 and capacitor C4 are used to protect the diac in the triac driver from the voltage transients across the triac. The line wire of the power supply is fed to the triac and the load is connected in series with triac and the neutral. Minimum holding current must be maintained in order to keep the triac on.

3.2.4 Controller system

The schematic of the overall system is shown in Fig. 3.6 and the list of components used is given in Table 1. The circuit is breadboarded using above described blocks. The software is described in next section

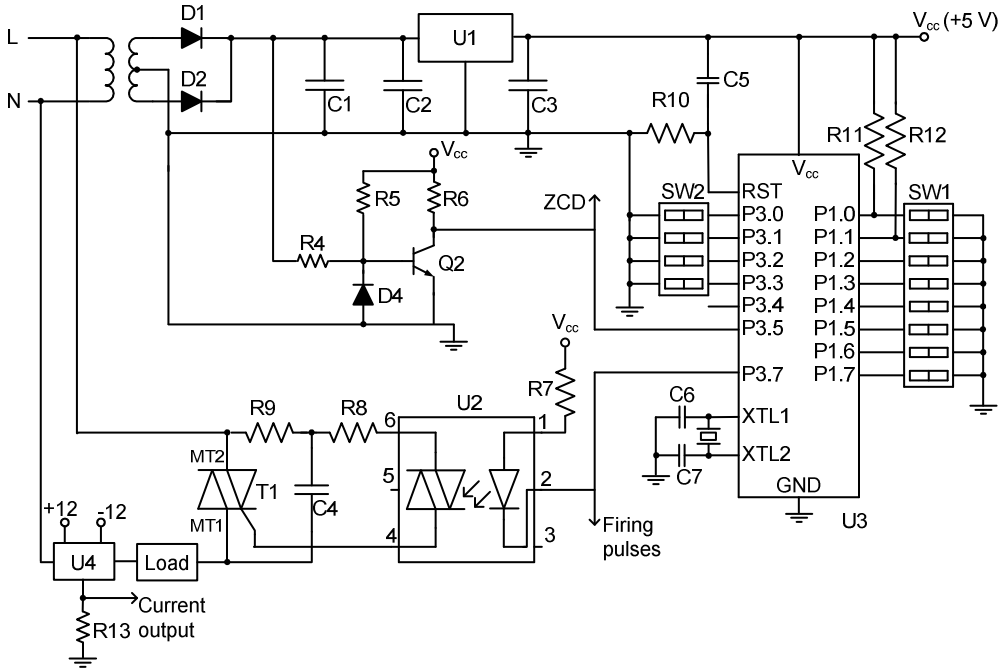


Fig. 3.6 Schematic of the ICC system.

Table 1: List of components

Component	Designator	Specifications
Resistor	R1, R3, R9	1 kΩ / 0.25 W
Resistor	R2, R4, R11, R12	10 kΩ / 0.25 W
Resistor	R5, R6	100 kΩ / 0.25 W
Resistor	R7	150 Ω / 0.25 W
Resistor	R8	220 Ω / 0.25 W
Resistor	R10	8.2 kΩ / 0.25 W
Resistor	R13	82 Ω / 0.25 W
Capacitor	C1	1000 µF / 50 V
Capacitor	C2, C3,	1 µF / 25 V
Capacitor	C5	10 µF / 25 V
Capacitor	C4	0.22 µF / 400 V
Capacitor	C6, C7	33 nF
Diode	D1, D2, D3, D4	1N4007
Triac	T1	BTA 06A
Voltage Regulator	U1	LM 7805
Optoisolator	U2	MOC 3020
Microcontroller	U3	AT89C2051
Hall sensor	U4	LA 55 - P
Crystal	XTAL	12 MHz
Switches	SW1, SW2	DIP switch
Transformer		12 - 0 - 12 V

3.3 Controller software

The microcontroller is programmed to perform following tasks.

1. Receive the desired duty cycle through switches, interfaced on port 1.

2. Generate the triac firing pulses according to ZCD pulses.

3. Calculate the running average of duty cycle in each cycle.

4. Generate the pseudo-random sequence

An IIR filter is implemented in software to calculate the running average and control the input to the filter. If the average lies within the range, input to the filter is decided by pseudo-random sequence. To implement IIR low pass filter, using integer arithmetic, equation (3.1) is modified to

$$y(n) = \left(Ax(n) + By(n-1) \right) / C \qquad (3.3)$$

where $(1 - \beta) = A / C$, $\beta = B / C$, and β is the load inertia constant in (3.1).

$$\beta^n = 0.01$$

If we consider the control period of 20 cycles,

$\beta = (0.01)^{1/20} = 0.7936 \approx 0.8$ and $(1 - \beta) = 0.2$

For simplicity of programming, the filter was implemented using 8-bit coefficients and 16-bit accumulator for intermediate results. Hence the coefficients in (3.3) were scaled to have integers. Using $C = 64$, we get $A = 13$ and $B = 51$.

The software on the microcontroller is written in assembly language. The main program initializes the ports, timers and different assigned variables. Timer 0 is used to generate firing pulse for triac and timer 1 is used to generate the pseudo-random sequence. The algorithm of main program and different subroutines is as below.

Main program

Initializations

Port 1: input port, port 3: P3.0 – P3.5 as input, P3.7 as output, timer 0 and timer 1 in mode 1, timer overflow interrupts, cycle_count (cycle), seed value for pseudo-random sequence generator, filter input, previous average, on_cycle_count (cpulse)

Start:

Initializations.

rep:

Read switch settings on port P1 to get the number of on cycles.

Get the values of duty cycle and tolerance from look-up table to determine the effective duty cycle based on above switch settings.

pol:

Poll for pin P3.5 to check if ZCD pulse available?.If no, go to pol.

Decrement and check cycle_count. If non-zero, go to cal.

Re-initialize cycle_count, on_cycle_count, and go to rep.

cal:

Get the input value, $x(n)$, for filter, multiply it with filter-coefficient A and store the result in R2R1.

Get the previous average output $y(n\text{-}1)$, multiply it with filter-coefficient B and store the result in R4R3.

Add the present input and previous average value, divide the result by 64 to get the present average value and store it in R4R3.

Store the same for later use, as a previous average $y(n\text{-}1)$ in next cycle.

Check if average duty cycle is greater than the desired value? If no, go to neg_tol.

out0:

Set the filter input to 0.

Set bit 05h to indicate it has serviced off cycle and go to pol.

neg_tol:

Check if average duty cycle is less than the desired value? If no, go to random.

out1:

Set filter input to 1 and call pulse subroutine and go to pol.

random:

Check the pseudo-random number? If it is 1, go to in_one.

Set filter input to 0.

Set bit (05h), to indicate that it has serviced off cycle and go to pol.

in_one:

Set the filter input to 1 and call pulse subroutine and go to pol.

pulse:

Set the flag_bit.

Check the bit (05h) for whether the firing angle is required? If yes, go to fract.

Load registers R0 and R1 with small delay for firing triac at zero crossing and go to load.

fract:

Read port 3 to get the firing angle setting for triac.

Get the desired value from firing angle look-up table into R1 & R0 registers.

load:

Load this value in timer 0 registers (TL0 & TH1) appropriately and start the timer.

Check triac firing pulse finished? If no, keep checking flag_bit.

Clear bit (05h) to indicate it has come after servicing on cycle.

Return from subroutine.

Timer0 (T0) Service Routine

Stop the timer.

Increment pulse_counter.

Check whether total number of pulses over? If not, go to pulse_out.

Set bit (04h) to indicate that control period is over and go to no_action.

pulse_out:

Output the triac firing pulse.

no_action:

Clear flag_bit to indicate that pulse output is over.

Return from the interrupt.

Timer1 (T1) Service Routine (for pseudo-random sequence generator)

Bring high-byte of seed value in accumulator

Rotate accumulator left to get bit 15 of seed in MSB and store it in 42h

Rotate accumulator left again for 2 times to get bit 13 of seed in MSB and store it in 43h

Bring low-byte of seed in accumulator, swap it to get bit 4 in MSB and store in 44h

Logically XOR the bits 16, 15, 13 and 4 of seed and save the result in carry bit

Rotate 16-bit value of seed to left through carry. Bit coming out of MSB of high-byte of seed value is the pseudo-random number

Return from the interrupt.

Chapter 4
TEST AND RESULTS

The microcontroller-based integral cycle controller as described in the previous chapter was assembled on breadboard and its performance was tested for

1) Operation under variations in supply voltage and frequency and for different wave-shapes.
2) Different switching strategies with resistive and inductive loads.
3) Effect of phase delay on removal of short-time transient in inductive loads.

4.1 Experimental set-up

The experimental set-up for testing the controller circuit is shown in Fig. 4.1. The ac power delivered to the load is controlled by the designed integral cycle controller. A Hall-effect sensor, powered by the external ± 12 V dc supply, is used for distortion-less monitoring of the phase relationship between the supply voltage and the load current. The set-up gives 3 outputs for monitoring: the ZCD output as detected by the controller circuit, pulses in-synchronous with the triac firing pulses and the load current as sensed by the Hall-effect sensor. The supply voltage and load voltage are monitored using differential probes. In this set-up, the supply voltage may be given from a high power ac amplifier for studying the circuit performance for variations in supply voltage and frequency and for different wave-shapes.

4.2 Controller operation with variations in supply voltage and frequency and for different wave-shapes

The controller is tested with static resistive load (R = 55 Ω) using burst (or on/off) switching strategy for operation under variations in supply voltage, frequency and different wave-shapes. The supply voltage for this purposes is provided by amplifying the output of a function generator (“Aplab 2019”) by a power amplifier “RMX 4050HD” (QSC Audio Inc., Costa Mesa, Cal.) with lower and upper 3-dB cutoff frequencies of 5 Hz and 50 kHz, respectively.

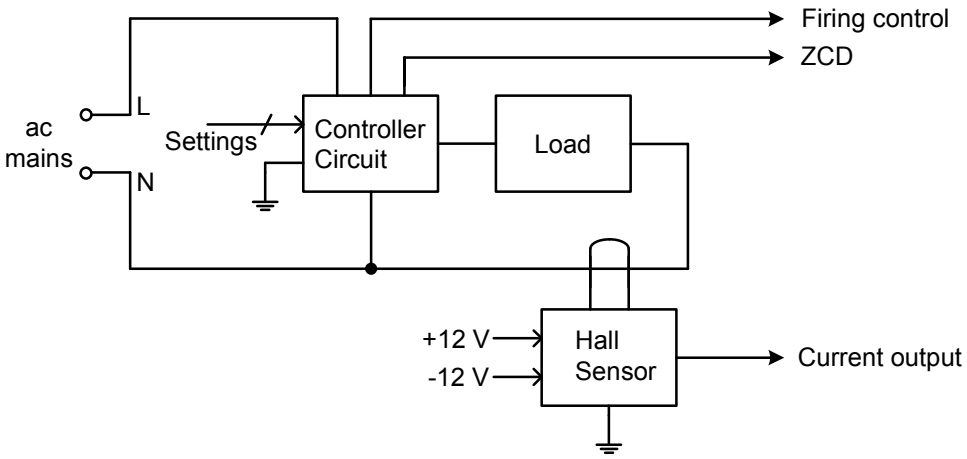


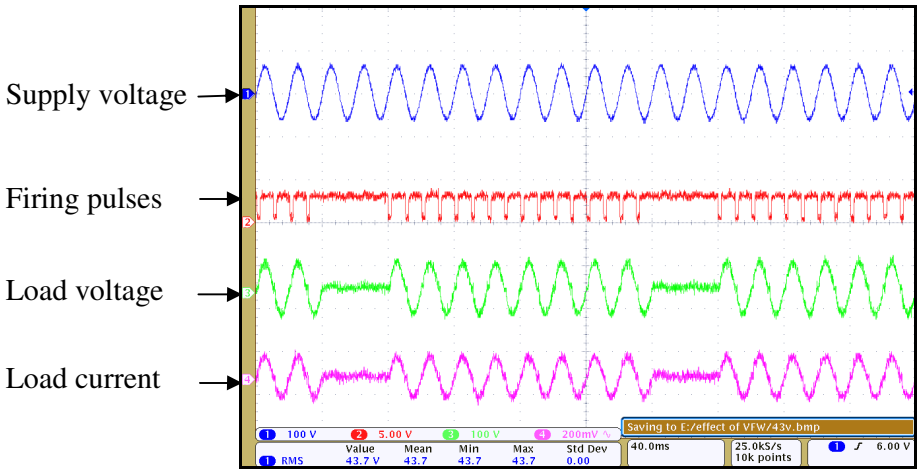
Fig. 4.1 Experimental set-up for testing the microcontroller based ICC circuit.

In the burst mode, the controller periodically passes all on-cycles in a burst and then blocks all off-cycles. Fig. 4.2 shows the controller operation with sinusoidal supply of 50 Hz and variation in supply voltage. The controller operation was satisfactory for supply RMS voltage down to 43 V.

Fig. 4.3 shows the controller operation with sinusoidal supply with RMS voltage 57 V and different frequencies. The controller worked satisfactorily in the frequency range 42 - 82 Hz.

A signal generator and power amplifier combination was used for testing the circuit operation with different wave shapes. Fig. 4.4 shows the supply voltage as output by the amplifier for triangular and square wave inputs of 50 Hz to the power amplifier. The supply voltage was distorted due to high-pass filtering by the power amplifier. Even with the distorted supply waveforms, the controller operated satisfactorily.

(A)



(B)

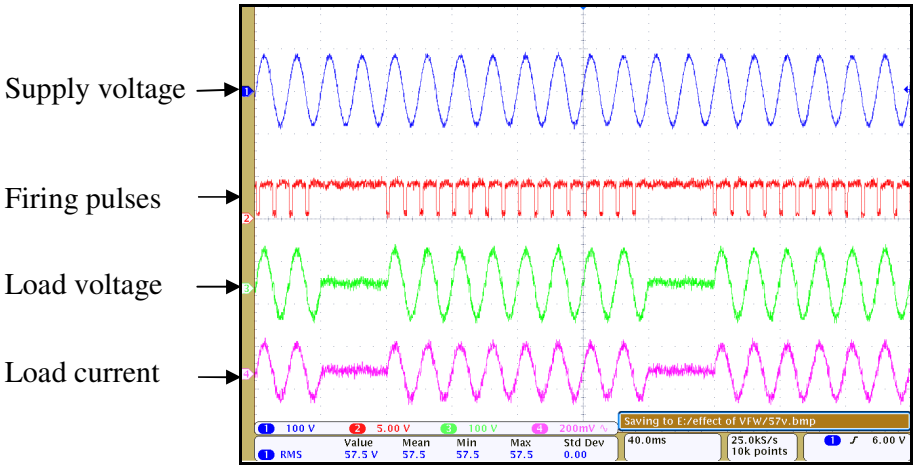
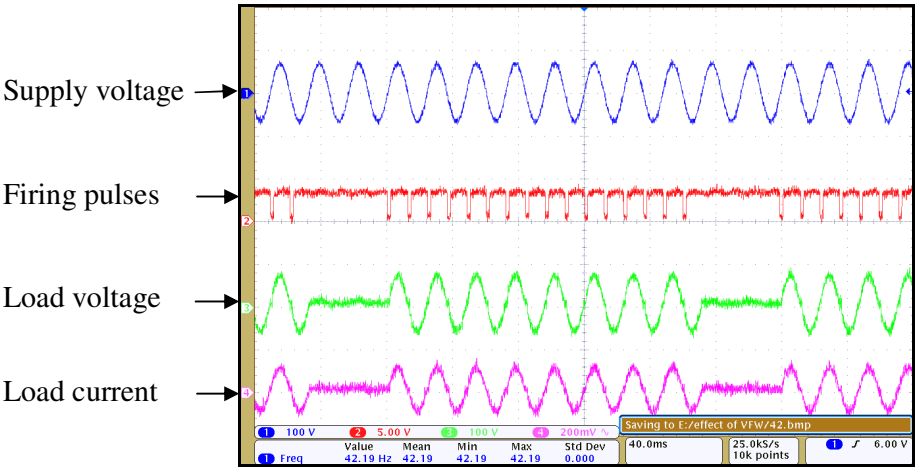
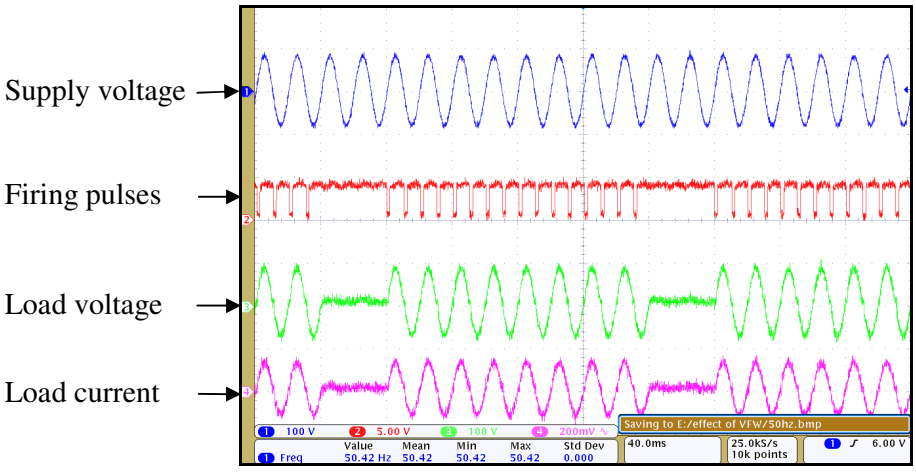


Fig. 4.2 Controller operation in burst mode, for sinusoidal supply with frequency of 50 Hz and RMS voltages of (A) 43 V, and (B) 57 V.

(A)



(B)



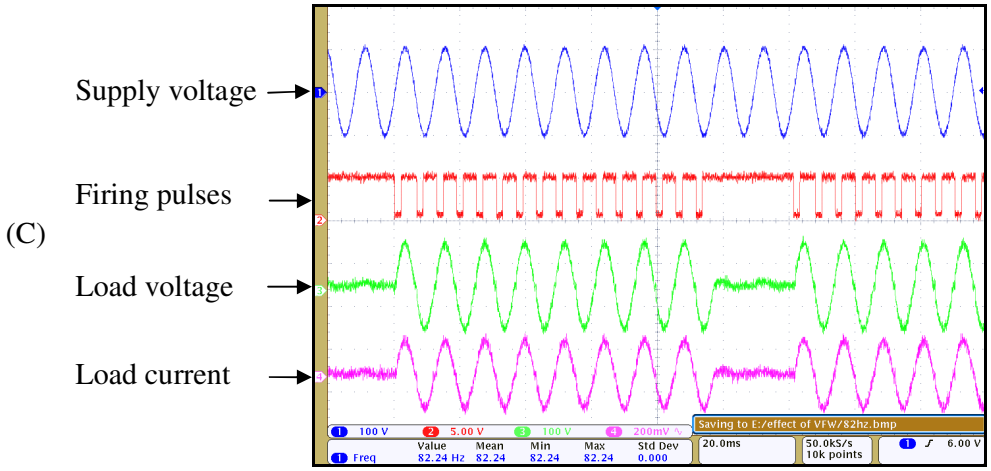
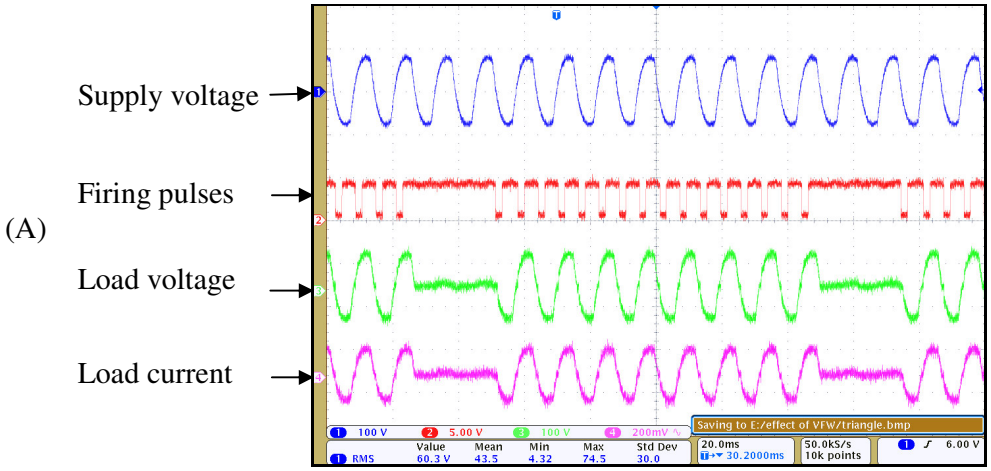


Fig. 4.3 Controller operation in burst mode for sinusoidal supply with RMS voltage of 57 V and frequencies of (A) 42 Hz, (B) 50 Hz, and (C) 82 Hz.



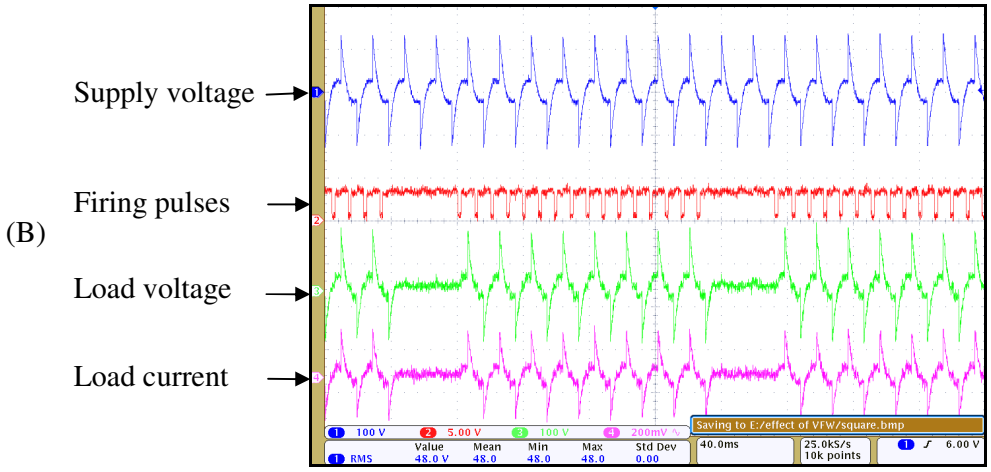
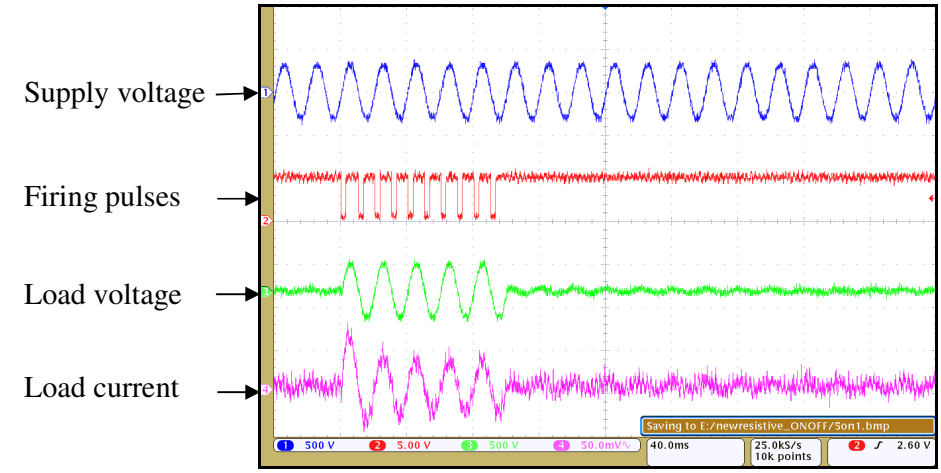


Fig. 4.4 Controller operation in burst mode with supply voltage obtained from power amplifier for inputs of (A) triangular wave, and (B) square wave.

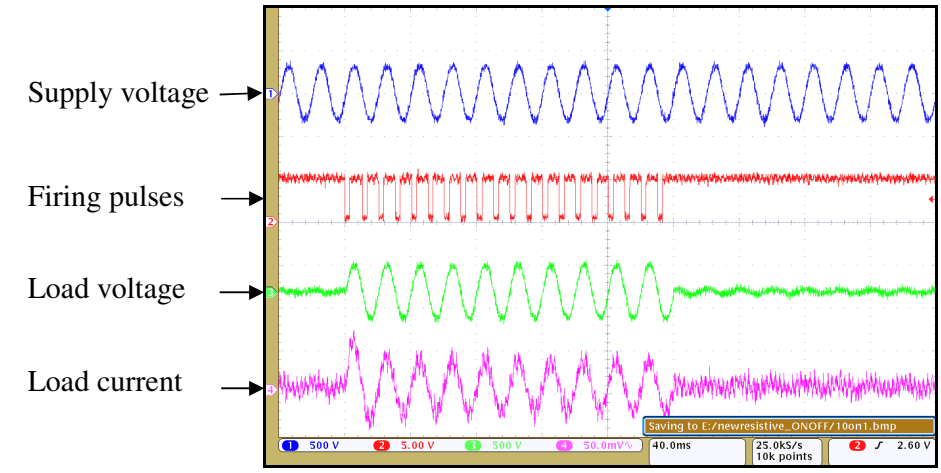
4.3 Controller operation using burst switching strategy, resistive load, and different duty cycles

A 40 W incandescent lamp was used as a resistive load for testing the controller. The lamp had a resistance 70 Ω in the cold state. The load voltage and load current were observed for control period set as 20 cycles and 5, 10 and 15 on-cycles. An inrush current was observed during the initial cycle due to low turn-on resistance as shown in Fig. 4.5.

(A)



(B)



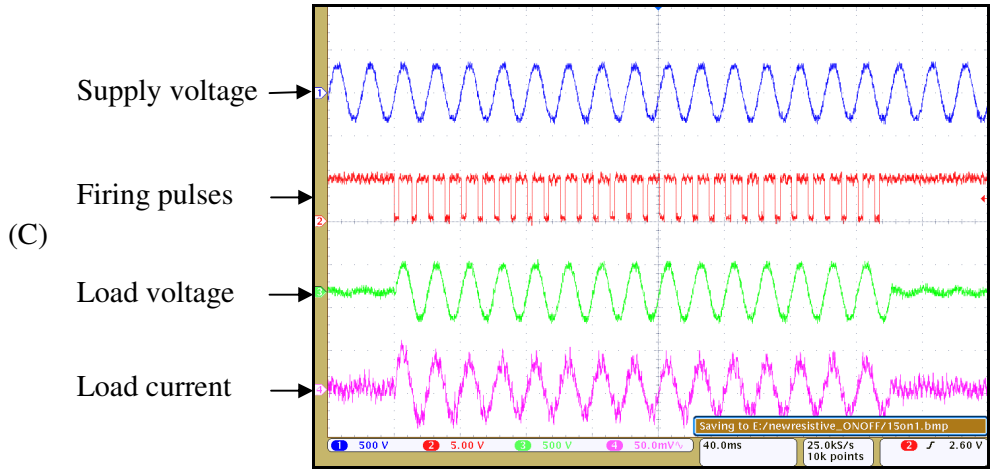
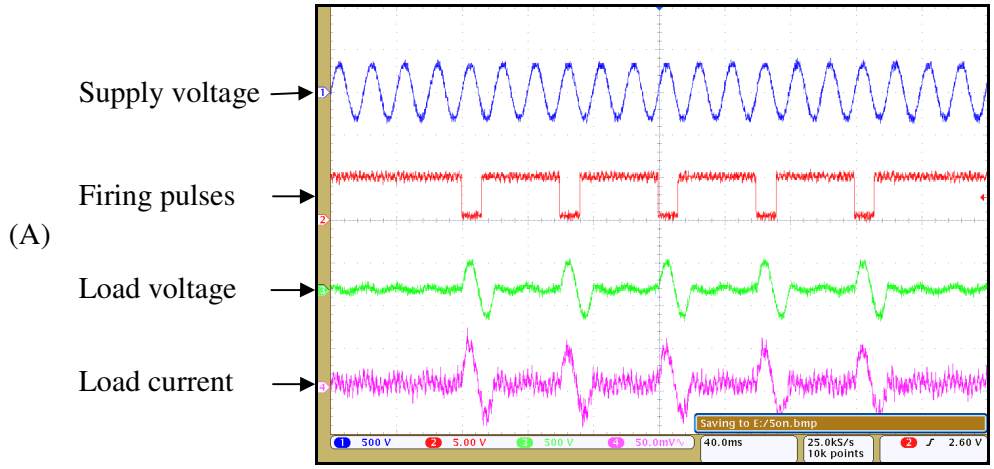


Fig. 4.5 Controller operation using burst switching strategy, supply from mains voltage, and resistive load for duty cycles of (A) 5/20, (B) 10/20, and (C) 15/20.

4.4 Controller operation using random switching strategy, resistive load, and different duty cycles

The same 40 W lamp as used in the previous section was used for testing the controller using switching strategy determined by pseudo-random sequence and low-pass IIR filter. The controller was tested for duty cycles of 5/20, 10/20, and 15/20 passing, with on-cycles randomly distributed by pseudo-random sequence and the duty cycle tracked by the low pass IIR filter. The controller operated satisfactorily. Inrush current was observed after large number of cycles. The waveforms observed are shown in Fig. 4.6.



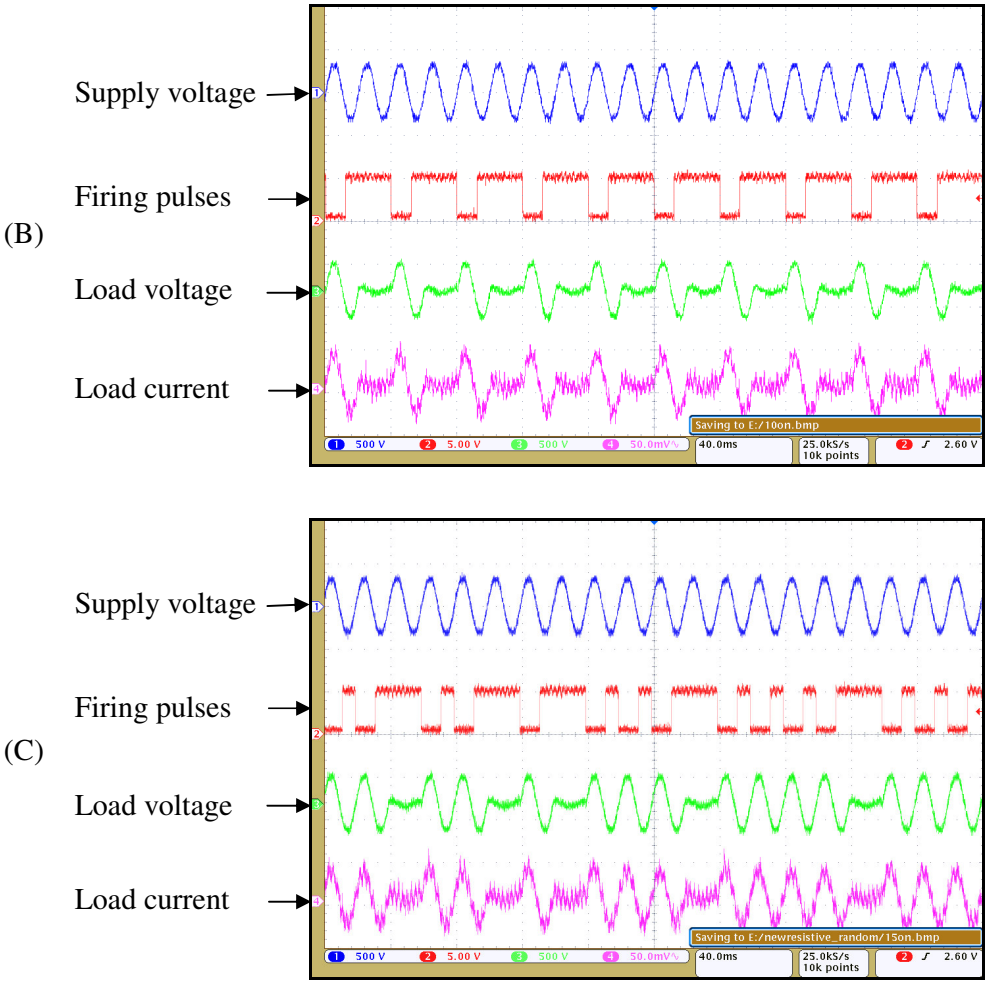


Fig. 4.6 Controller operation using random switching strategy, supply from mains voltage, and resistive load for duty cycles of (A) 5/20, (B) 10/20, and (C) 15/20.

4.5 Controller operation using burst switching strategy, inductive loads and different duty cycles

A table fan with a resistive speed regulator was used as an inductive load for testing the controller. The fan was tested with the fan speed set to (i) highest speed and the (ii) lowest speed setting, giving two inductive loads ZL1 and ZL2. The measured impedances in the unpowered state were (i) ZL1: dc resistance = 708 Ω, 50-Hz impedance = 378 Ω and (ii) ZL2: dc-resistance = 971 Ω, 50-Hz impedance = 373 Ω. The two loads were used for testing the controller operation using burst switching strategy and to observe the load current. The load voltage and load current were observed for mains voltage as the supply voltage, and duty cycles of 5/20, 10/20 and

15/20. The waveforms are shown in Fig. 4.7 and Fig.4.8. The load current waveforms exhibit transient dc components due to inductive component of the load.

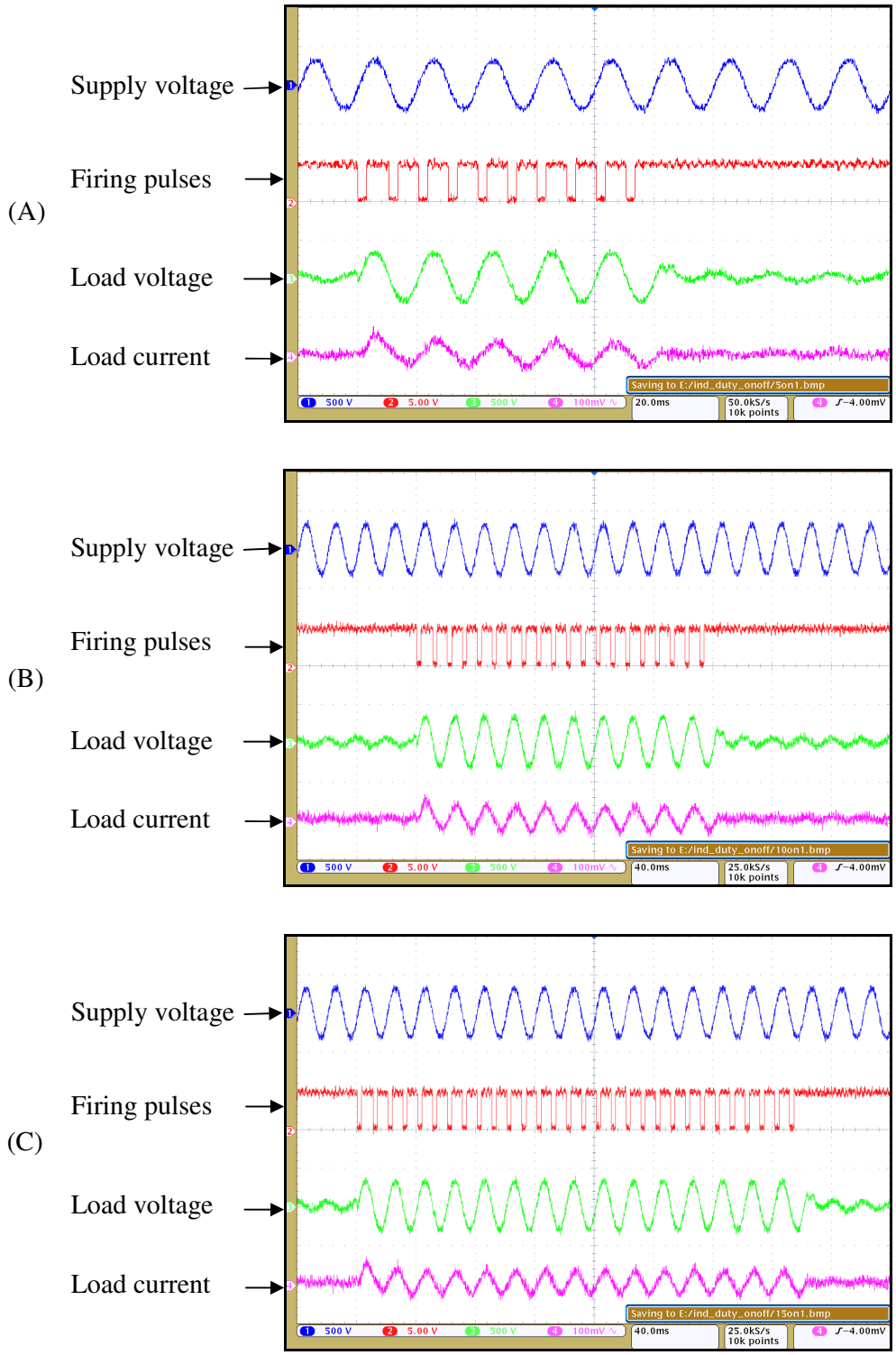


Fig. 4.7 Controller operation using burst switching strategy, mains voltage, and inductive load ZL1, for duty cycles of (A) 5/20, (B) 10/20, and (C) 15/20.

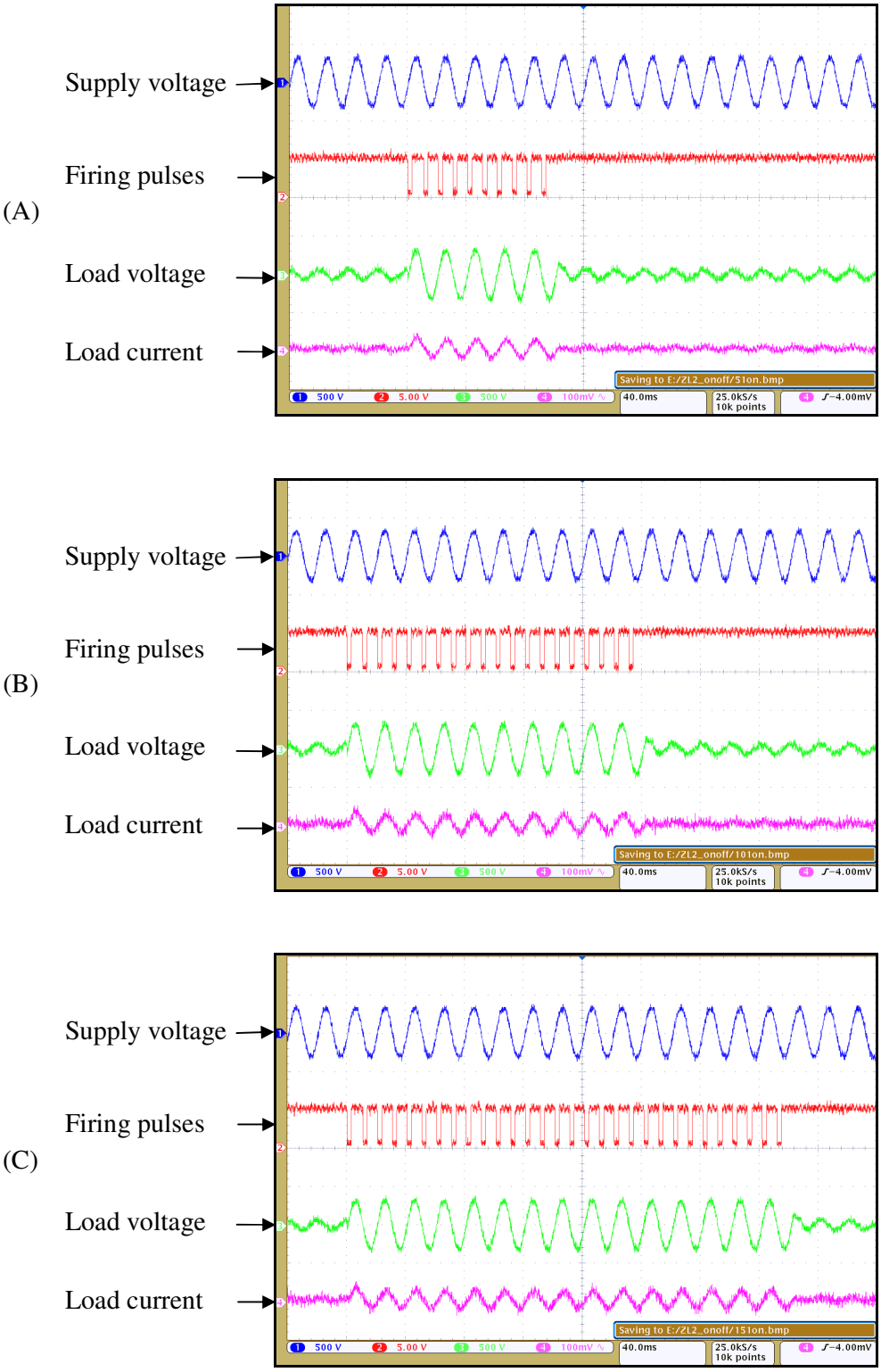
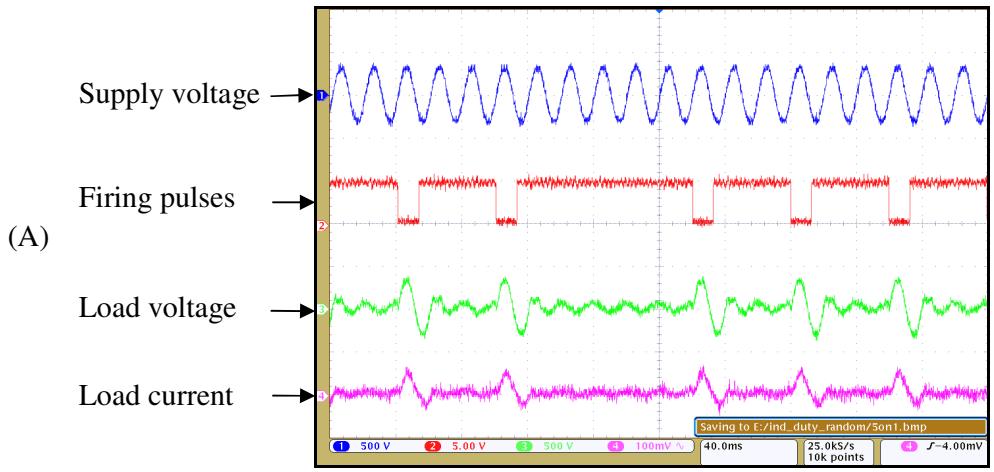
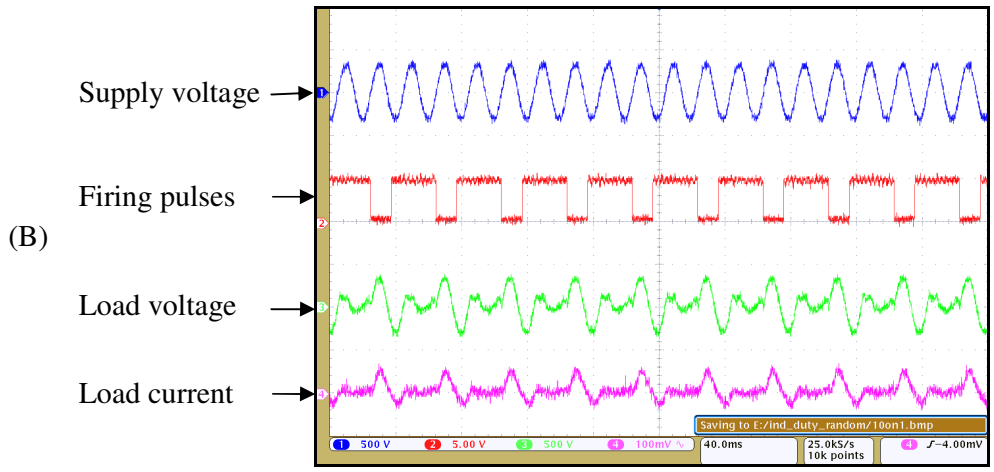


Fig. 4.8 Controller operation using burst switching strategy, mains voltage, and inductive load ZL2, for duty cycles of (A) 5/20, (B) 10/20, and (C) 15/20.

4.6 Controller operation using random switching strategy, inductive loads and different duty cycles

The fan used in the tests reported in the previous section was used for testing the controller using switching strategy determined by pseudo-random sequence and low pass IIR filter. Here also controller is tested using mains voltage as the supply voltage and for duty cycles of 5/20, 10/20, and 15/20. The waveforms for ZL1 and ZL2 are shown in Fig. 4.9 and Fig. 4.10 respectively and the load currents exhibit short-time dc transients.





(C)

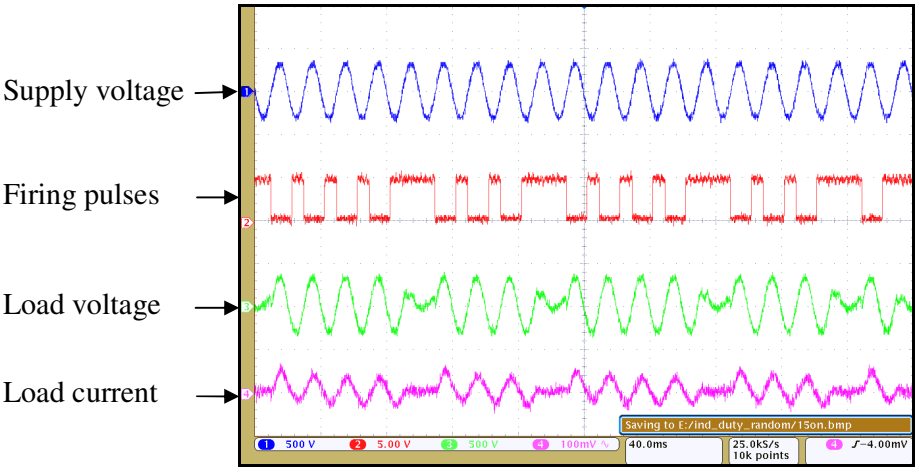
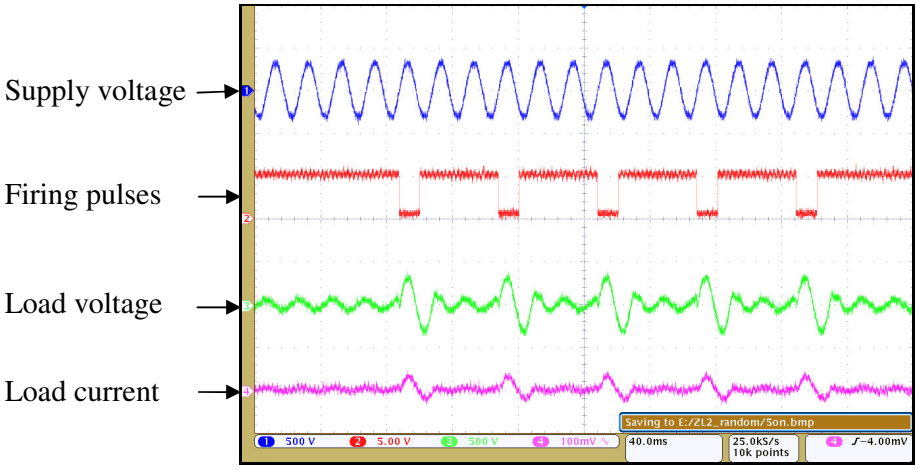
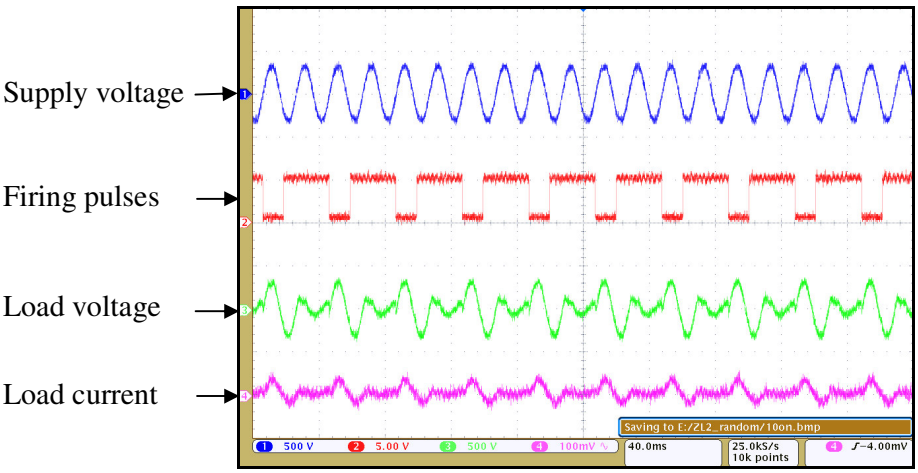


Fig. 4.9 Controller operation using random switching strategy, mains voltage, and inductive load ZL1 and duty cycles of (A) 5/20, (B) 10/20, and (C) 15/20.

(A)



(B)



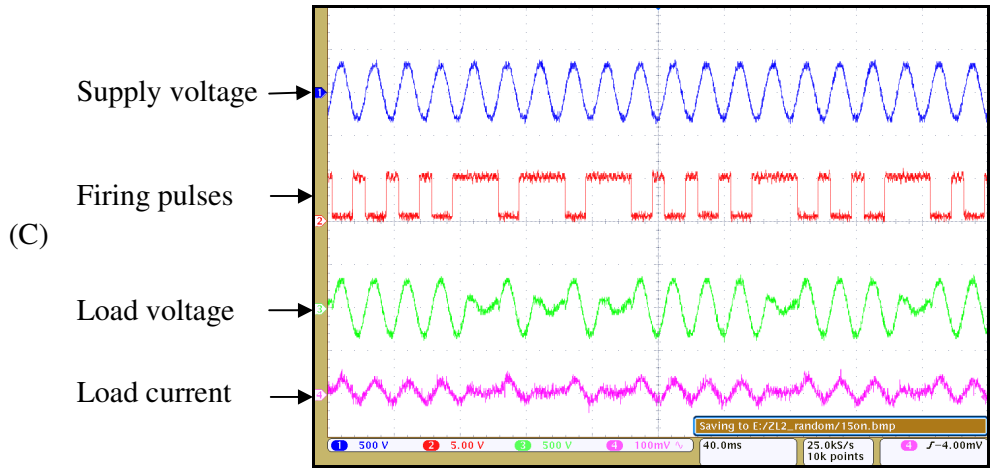
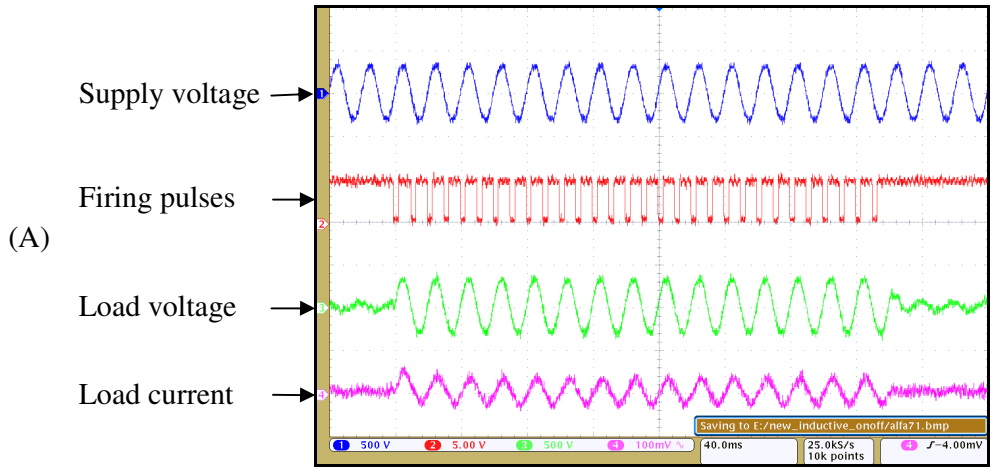


Fig. 4.10 Controller operation using random switching strategy, mains voltage, and inductive load ZL2 and duty cycles of (A) 5/20, (B) 10/20, and (C) 15/20.

4.7 Effect of phase delay for removing short-time dc transient in inductive loads with burst switching

The table fan used for tests in the previous two sections was used for examining the effect of changing the phase delay on the transients. The waveforms for ZL1 and ZL2 are shown in Fig. 4.11 and Fig. 4.12 respectively. It is seen that the short-time transient component present in load current of inductive load was reduced by adjusting the triac firing angle in the first cycle of a burst.



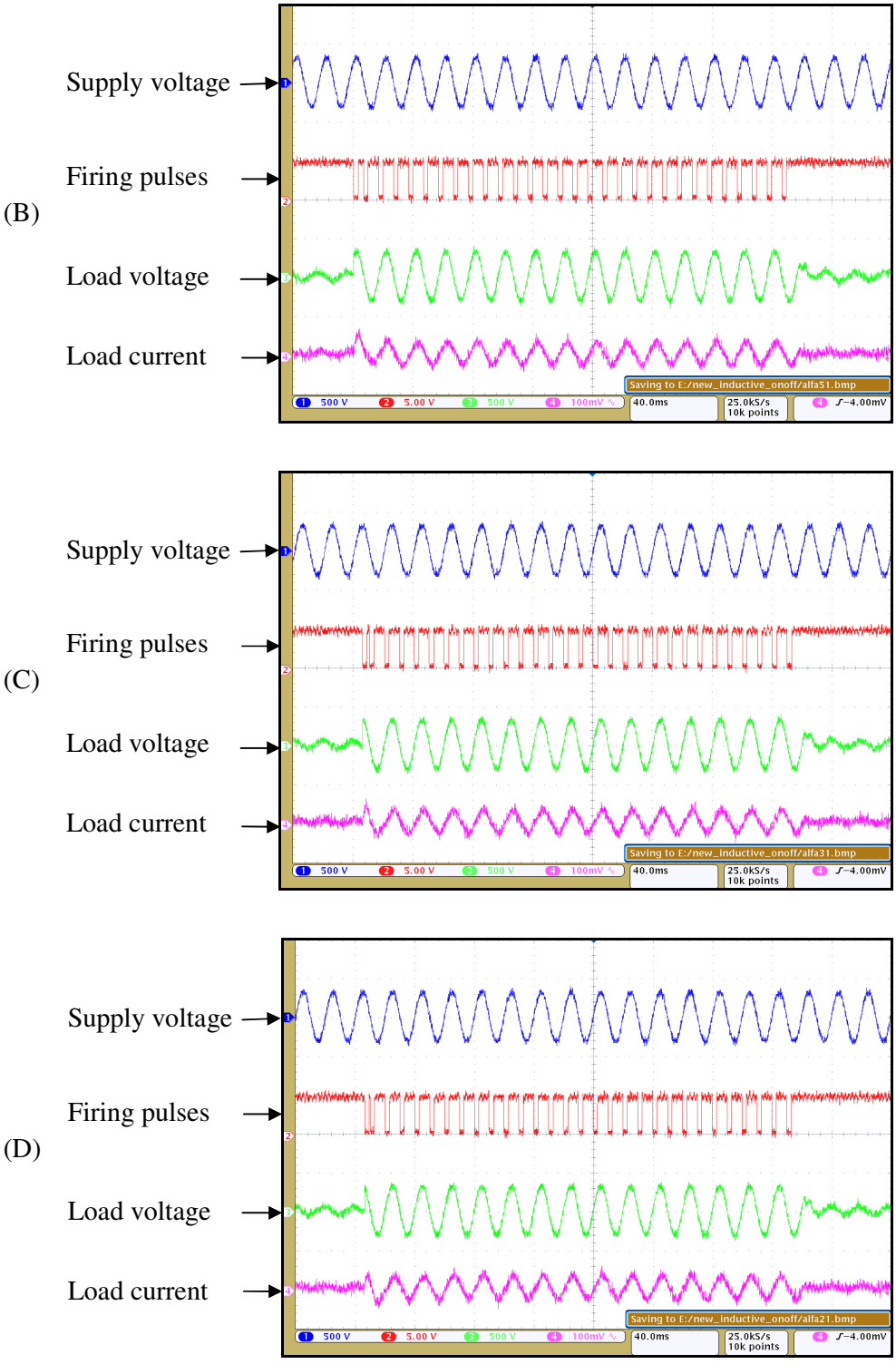
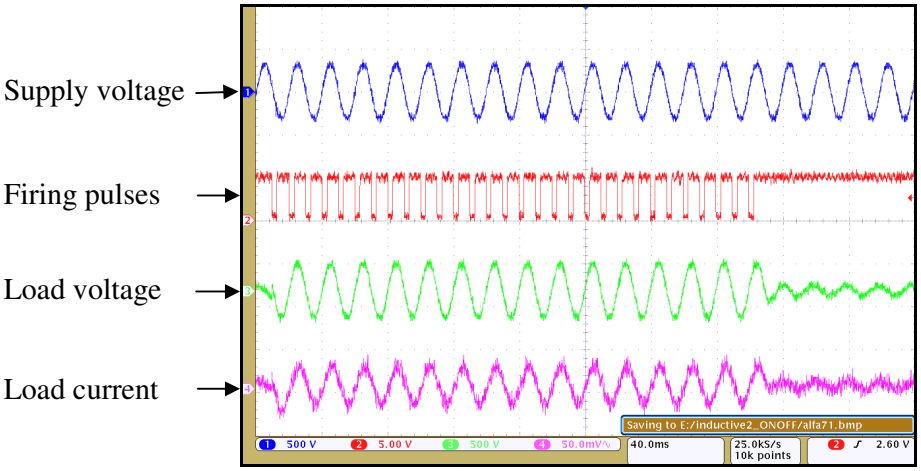
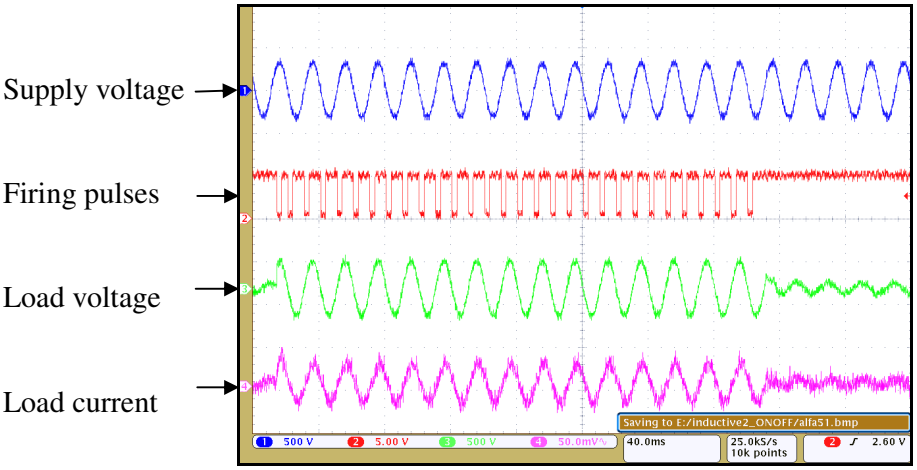


Fig. 4.11 Effect of phase delay in inductive load ZL1 using burst switching for various values of α (A) α = 0° (B) α = 72° (C) α = 108°, and (D) α = 126°.

(A)


Supply voltage
Firing pulses
Load voltage
Load current
Saving to E:/inductive2_ONOff/alfa71.bmp
500 V
5.00 V
500 V
50.0mV
40.0ms
25.0kS/s
10k points
2.60 V

(B)


Supply voltage
Firing pulses
Load voltage
Load current
Saving to E:/inductive2_ONOFF/alfa51.bmp
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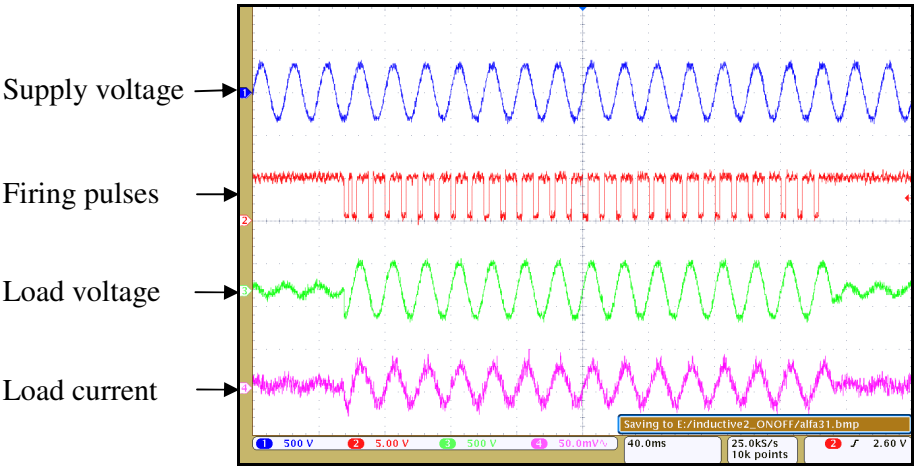
5.00 V
500 V
50.0mV
40.0ms
25.0kS/s
10k points
2.60 V

(C)


Supply voltage
Firing pulses
Load voltage
Load current
Saving to E:/inductive2_ONOFF/alfa31.bmp
500 V
5.00 V
500 V
50.0mV
40.0ms
25.0kS/s
10k points
2.60 V

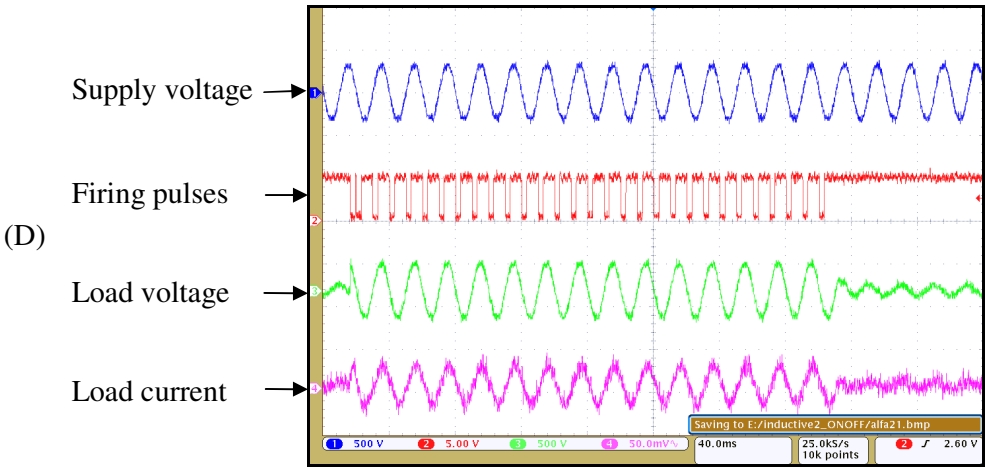
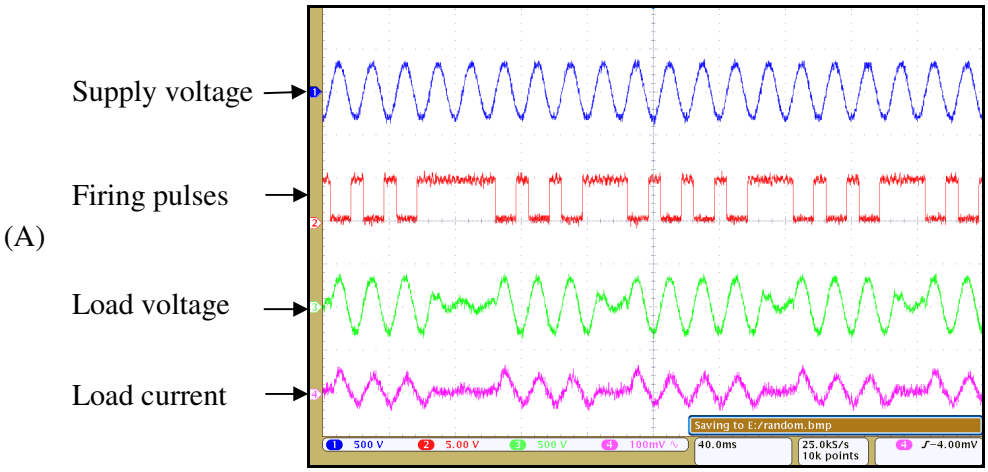


Fig. 4.12 Effect of phase delay in inductive load ZL2 using burst switching strategy for various values of α (A) α = 0° (B) α = 72° (C) α = 108°, and (D) α = 126°.

4.8 Effect of phase delay for removing short-time dc transient in inductive loads with random switching

In this scheme, the on-cycles are randomly distributed and triac is fired at different angles to remove the dc component in load current. The waveforms for ZL1 and Zl2 are shown in Fig. 4.13 and Fig. 4.14 respectively. It is seen that the short-time transient component present in load current of inductive load was reduced by adjusting the triac firing angle in the first cycle of a burst.



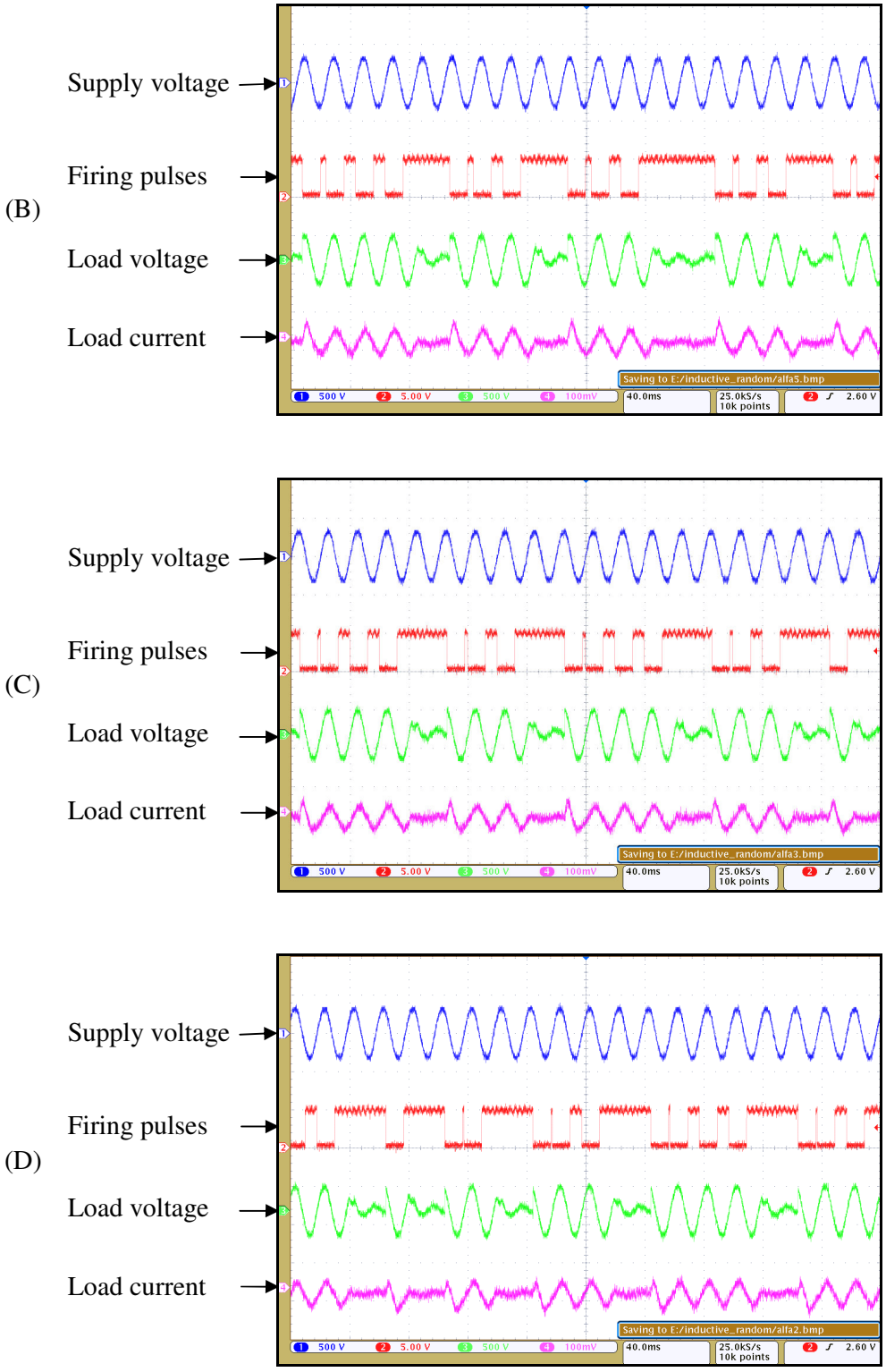
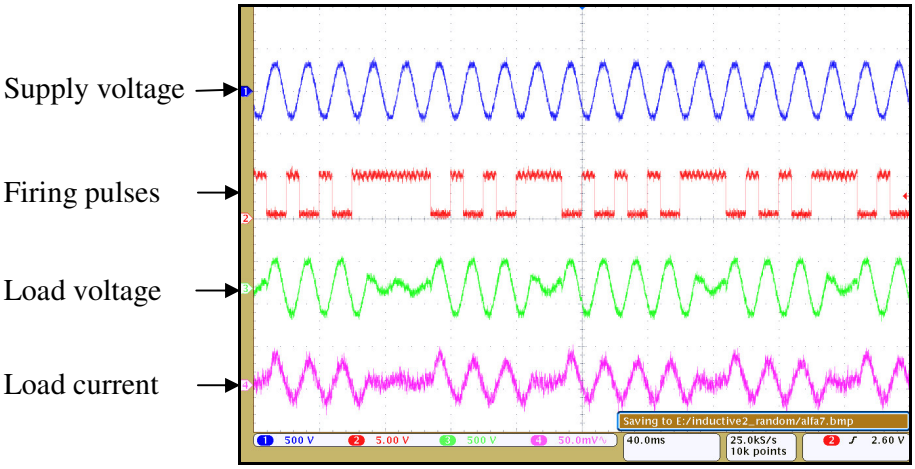


Fig. 4.13 Effect of phase delay in inductive load ZL1 using random switching strategy for various values of α (A) α =0°, (B) α = 72°, (C) α = 108°, and (D) α = 126°.

(A)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Firing pulses
Load voltage
Load current
Saving to E:/inductive2_random/alfa7.bmp
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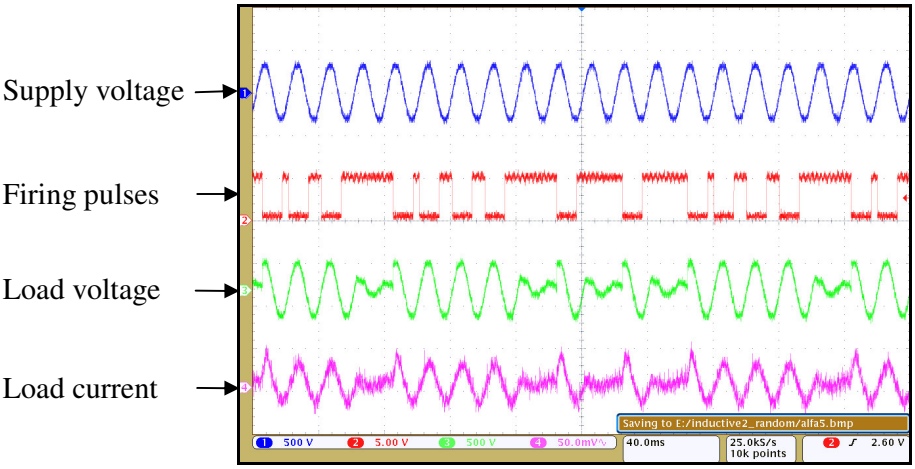
500 V
50.0mV
40.0ms
25.0kS/s
10k points
2.60 V

(B)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Firing pulses
Load voltage
Load current
Saving to E:/inductive2_random/alfa5.bmp
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500 V
50.0mV
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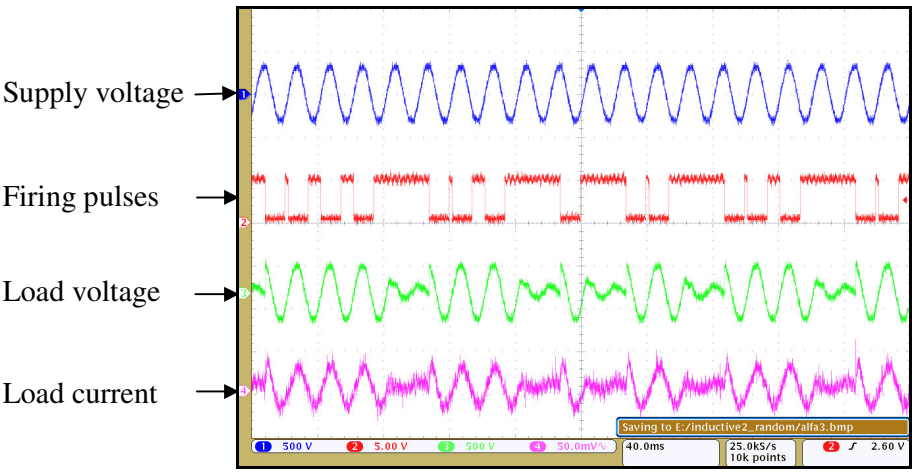
25.0kS/s
10k points
2.60 V

(C)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Firing pulses
Load voltage
Load current
Saving to E:/inductive2_random/alfa3.bmp
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500 V
50.0mV
40.0ms
25.0kS/s
10k points
2.60 V

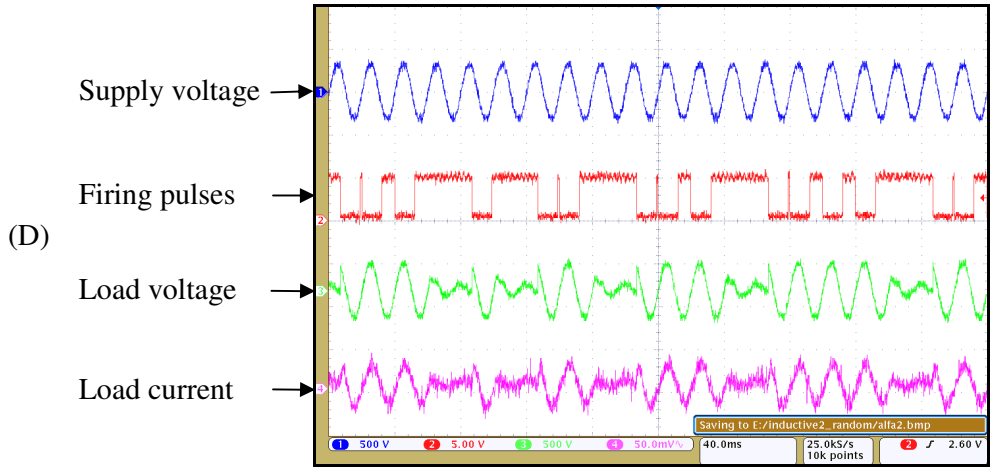

Fig. 4.14 Effect of phase delay in inductive load ZL2 using random switching strategy for various values of α (A) α = 0° (B) α = 72° (C) α = 108°, and (D) α = 126°.

4.9 Summary of results

Integral cycle controller designed in this project was tested under various conditions and both for the burst and random modes of operation. The controller worked satisfactorily for supply voltage down to 43 V_{RMS}, in the frequency range 42 – 82 Hz and with different wave-shapes. For inductive loads, the load current exhibited short-time transient which may cause core saturation. By firing the triac at an angle closer to load power factor angle, this transient can be reduced. For the table fan used as an inductive test load, delaying of the triac firing to 126° in the first cycle of a continuous sequence resulted in removal of the transient in the load current.

Chapter 5
SUMMARY AND CONCLUSION

The objective of project was to develop a microcontroller-based integral cycle power controller to control the ac power delivered to single-phase ac loads. The controller developed gives fine control steps and distributes the on cycles over a control period by using a switching strategy based on a pseudo-random sequence. An IIR filter which simulates the load inertia is used for controlling the duty cycle within specified tolerance about the desired value. The controller's performance is tested for operation under variations in supply voltage, frequency, and wave-shape for resistive type load. It works properly for supply voltage down to 27 V_{RMS}, and for the frequency range 42 – 82 Hz. It is tolerant to variations in the supply waveform as long as the detection of zero crossings is not affected. A provision for removing short-time dc transient present in case of inductive loads is also implemented. The controller has been used for controlling the speed of a fan as an inductive load.

User input to the controller has to be changed from switches to a more convenient rotary control and the circuit has to be assembled on a PCB and boxed before being used as a prototype. Some additional testing and software modification is needed. The sequence length of the pseudo-random sequence generator needs to be increased and the effect of the length of the sequence on the distribution of harmonics needs to be studied. Effectiveness of discontinuous phase control in the initial cycle of burst for removal of transient dc component in inductive loads has to be tested. An optimal strategy for distributing the discontinuous switching depending on the history of switching sequence may be needed.

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Vidyadhar V. Kamble

30th June 2010