A SYNCHRONOUS DEMODULATOR WITH AUTOMATIC BASELINE RESTORATION FOR IMPEDANCE CARDIOGRAPHY

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by

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M.Tech. Dissertation Approval

This dissertation entitled **"A synchronous demodulator with automatic baseline restoration for impedance cardiography"**
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is approved, after the successful completion of *viva voce* examination,
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ABSTRACT

Impedance cardiography is a noninvasive technique used for estimating the stroke volume and cardiac output by sensing the variations in the electrical impedance of the thorax during each cardiac cycle. The impedance is measured by injecting a high-frequency low-level current into the thorax using a pair of electrodes and sensing the voltage developed across it using another pair of electrodes. The sensed voltage is demodulated to extract the impedance variation signal. The objective of the project is to develop a demodulator for extracting a noise- and distortion-free signal. A demodulator based on synchronous current steering and sampling at the peaks has been developed to improve noise rejection, interference rejection, carrier ripple rejection, and sensitivity. A baseline restoration has been incorporated in the demodulator in order to extend the range of the basal impedance over which the impedance can be measured. The demodulator has been realized as part of a microcontroller-based instrument. A direct digital synthesizer (DDS) has been used for generating the sinusoidal excitation waveform with high amplitude stability and digital control over frequency. A digital potentiometer is used to set the amplitude of the excitation current from a voltage-to-current converter. Another digital potentiometer controls the signal amplitude for baseline correction. Another DDS is used to generate a square wave, synchronous with the sinusoidal waveform and with a settable phase shift, to serve as the reference for synchronous demodulation. The microcontroller has an isolated serial interface for control and data transfer. The entire circuit operates with a single supply. The operation of the demodulator has been verified for ripple and noise rejection and baseline restoration. The circuit has to be assembled as an impedance cardiograph and detailed tests need to be carried out before its clinical use.

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Chapter 1

INTRODUCTION

1.1 Background

Bio-impedance in general refers to the electrical impedance offered by biological materials such as blood, tissue, bone, muscle etc. The measurement of this impedance can be used to noninvasively determine physiological parameters and monitor physiological activity. When a low amplitude and high frequency current is injected into the thorax and the voltage developed across it is measured, an amplitude modulated voltage is obtained [1], [2]. The amplitude variations (or the envelope) of the voltage waveform are related to the variations in the thoracic impedance caused due to inflow of blood into the thorax in each cardiac cycle [2]. This voltage is demodulated to extract the impedance variation signal. Stroke volume and several other cardiovascular indices can be estimated from these variations which are used in the assessment of various cardiac disorders. This method, known as impedance cardiography is noninvasive, and low-cost technique and it has the potential of being used for the estimation of stroke volume, as an alternative to the established methods like thermo dilution, Fick's method, and Doppler echocardiography [3], [4].

In impedance cardiography, the impedance measurement is carried out at a frequency in the range of 20 – 100 kHz with the amplitude of the injected current kept less than 5 mA to avoid the risks of physiological effects [1]. The sensed impedance in this frequency range is almost purely resistive. The basal impedance of the thorax is about 20 - 200 Ω and the impedance variation during each cardiac cycle is less than 2% [5], [6]. Hence highly sensitive demodulation techniques are required to sense these variations.

1.2 Project Objective

The objective of the project is to develop an instrument for impedance cardiography, overcoming the major problems in the existing instruments. The designs of the instruments developed earlier in our lab [7] - [10] and those reported by other groups [6] were studied. An impedance cardiograph consists of a current source, an impedance detector, a differentiator, and an ECG extraction circuit. The current source consists of a waveform generator and a voltage-to-current converter and the impedance detector consists of a voltage-sensing amplifier, a demodulator and a baseline restoration circuit. The ECG extraction circuit is used

for sensing ECG from the voltage-sensing electrodes to serve as a reference for processing of ICG.

The baseline restoration circuit was simplified by using on-chip ADC and DAC in microcontroller. A direct digital synthesizer (DDS) [11] based waveform generator has been used to achieve high amplitude stability and to have digital control over frequency and phase. A transformer based voltage-to-current converter has been designed to provide balanced outputs and hence reduce common mode pick-up. A modified Howland current source, with one terminal of the load being grounded, has been used for implementing the voltage-to-current converter to avoid instability due to stray capacitances at the op amp input terminals and to achieve high output impedance. A new demodulation scheme based on synchronous current steering and sampling at the peaks has been developed to improve noise rejection, interference rejection, carrier ripple rejection, and achieve high sensitivity. The circuit is powered by a single battery. An isolated RS232 interface has been provided for setting the frequency and excitation current as well as for acquiring the waveforms.

1.3 Report Outline

Chapter 2 covers the basics of impedance cardiography. Chapter 3 reviews the hardware blocks of the impedance cardiograph instrument developed earlier at IIT Bombay and other circuits reported in the literature. It also describes a modified baseline restoration circuit and the synchronous demodulation scheme used in this project. The fourth chapter gives the details of hardware and software design of the instrument developed during this project. The test and results are presented in Chapter 5. Summary and conclusions are given in the last chapter, and supplementary information is provided in the appendix.

Chapter 2

BASICS OF IMPEDANCE CARDIOGRAPHY

2.1 Heart Anatomy

Heart consists of four chambers, namely, left atrium, left ventricle, right atrium, and right ventricle as shown in Figure 2.1 [12], [13]. The atrio-ventricular (A-V) valves regulate the flow of blood from atria into the ventricles. The right atrium receives deoxygenated blood from all peripheral organs. It pumps this blood into the right ventricle which then pumps it to the lungs for oxygenation, through the pulmonary artery. The flow of blood from the right ventricle into the pulmonary artery is regulated by pulmonary valve. The oxygenated blood from the lungs is received by the left atrium. The left atrium pumps it into the left ventricle which then contracts and pushes the oxygenated blood into the aorta from where it is circulated throughout the body. The flow of blood from the left ventricle into the aorta is regulated by the aortic valve. The pulmonary and aortic valves are collectively called as the semilunar valves.

The mechanical activity of the heart occurs because of spontaneous generation of action potential in the sino-atrial (S-A) node located in the anterior wall of right atrium [13]. This action potential travels from the atria to the ventricle making them depolarize and repolarize, and hence contract and relax, alternatively in a rythmic fashion.

2.2 Cardiac Cycle and Cardiac Output

The period from the end of one heart contraction to the end of the next one is called as the cardiac cycle [12]. It includes all the events that occur in the heart during one heart beat. A complete cardiac cycle includes systole and diastole of the atria and systole and diastole of the ventricles. The atria and ventricles contract and relax alternatively to force blood from areas of higher pressure to lower pressure.

The relationship between electrocardiogram (ECG), atrial pressure, ventricular pressure, aortic pressure, and the ventricular volume is shown in Figure 2.2 [12]. It shows the pressure curves corresponding to the left side of the heart. The pressure curves in the right side are lower in magnitude but have the same shape [13]. The cardiac cycle lasts for 0.8 s for a heart rate of 75 beats/min [13]. The P wave in ECG corresponds to the depolarization of atrial muscles which result in atrial systole. As the atria contract, the pressure inside them increases forcing the blood into ventricles. The end of atrial systole corresponds to the end of

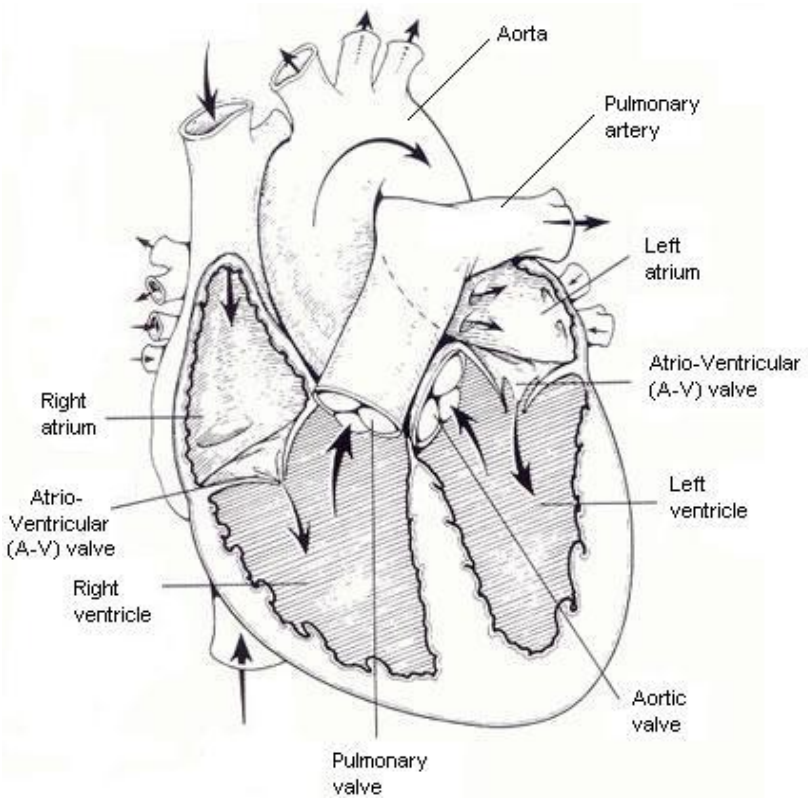

Figure 2.1 Different chambers of the heart and their associated blood vessels (adapted from [14]).

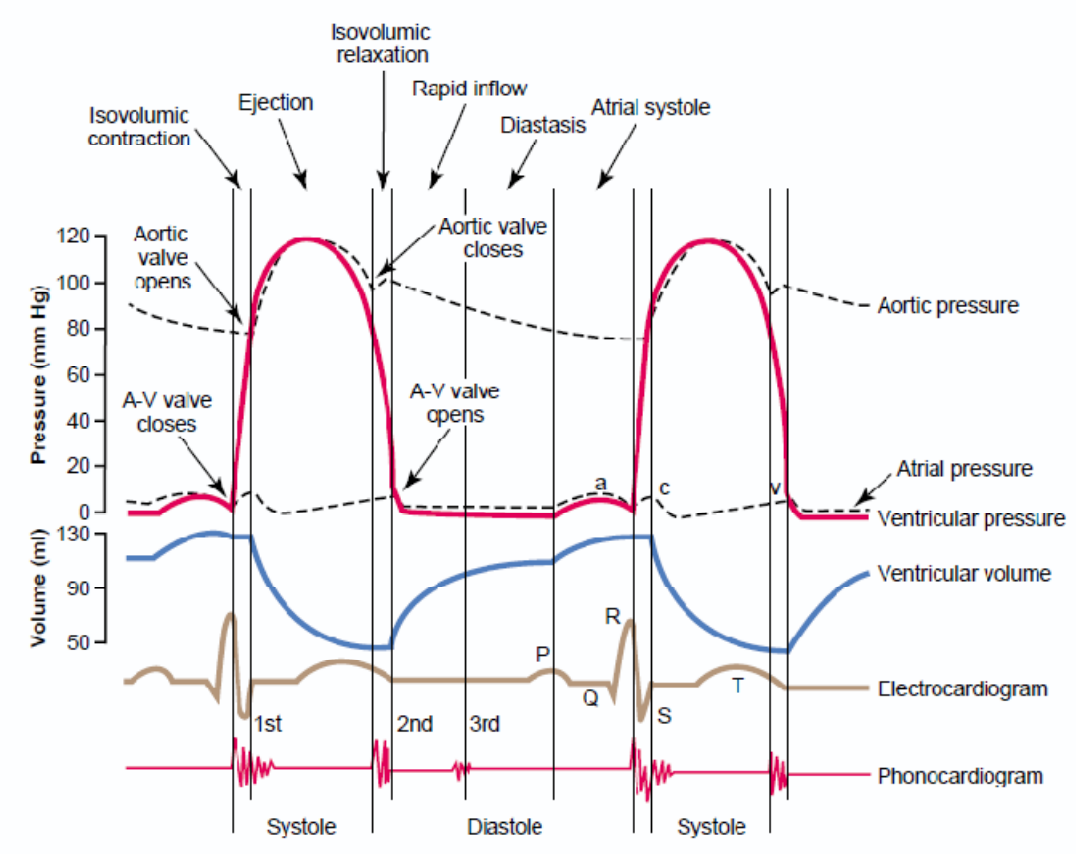

Figure 2.2 Different events of cardiac cycle [12].

the ventricular diastole. The volume of blood inside each ventricle after its diastole is called end-diastolic volume (EDV). The QRS complex in the ECG corresponds to the onset of the ventricular depolarization. The ventricular depolarization causes ventricular systole during which the ventricles are contracting and the atria are relaxed (diastole). As the ventricles contract, the pressure inside them increases and forces the A-V valves to close. This is followed by a period of iso-volumetric contraction during which the semilunar and the A-V valves are closed and the pressure inside the ventricles is building up. When the pressure inside the right and left ventricles become more than the pressure inside the pulmonary artery and aorta respectively, the semilunar valves open and the ejection of blood from the ventricles begins. The semilunar valves remain open for a period of about 0.25 [13]. The volume of blood remaining inside each ventricle after the ventricular systole is the end-systolic volume (ESV). The difference between EDV and ESV represents the volume of blood ejected from each ventricle during one heart beat. This volume is called stroke volume (SV) [12], [13]. The T wave in ECG corresponds to onset of ventricular repolarization which leads to relaxation of the ventricles. As the ventricles relax, the pressure inside them falls which leads to back-flow of blood from the aorta and pulmonary artery. This back-flow forces the semilunar valves to close. This is followed by a period of iso-volumetric relaxation during which the semilunar and A-V valves are closed and the pressure inside the ventricles is decreasing. When the ventricular pressure becomes less than the atrial pressure, the A-V valves open and there is a rapid inflow of blood into the ventricles. This is followed by atrial systole and the whole cycle repeats itself.

Cardiac output (CO) is the amount of blood ejected from each ventricle in one minute. It is equal to the product of stroke volume (SV) and heart rate (HR), that is,

$$\text{CO (mL/min)} = \text{SV (mL/beat)} \times \text{HR (beats/min)}$$

For a normal healthy adult, the average stroke volume under resting condition is approximately 70 mL/beat and heart rate is around 75 beats/min [13]. Hence the average cardiac output is 5.25 L/min. As the total blood volume in a normal adult is about 5 L [13], the entire blood volume circulates through the circulation system in one minute. The cardiac output is an important parameter in diagnosis and treatment of various disorders of the heart and the circulatory system.

2.3 Impedance Cardiography

Impedance cardiography is a noninvasive technique used for continuously measuring the variations in the thoracic electrical impedance and can be used for monitoring the stroke volume and the cardiac output [1], [2], [15] – [17]. It involves injecting a low intensity and high-frequency current into the thorax and measuring the voltage developed across it as

shown in Figure 2.3. During ventricular systole the total volume of blood in the thorax increases. Since blood has lower resistivity as compared to bone, muscle, and other tissues present in the thorax [1], [2], there is a decrease in the thoracic impedance during the ventricular systole. As a result, the voltage sensed across the thorax gets amplitude modulated, with its envelope representing the variations in the thoracic impedance with each cardiac cycle. This voltage is then demodulated to extract the amplitude variations, from which, the stroke volume and cardiac output are estimated using appropriate models and equations. It is a low-cost, noninvasive technique and it can be used for measuring stroke volume. Thus it can serve as an alternative to the established techniques like thermodilution, Fick's method, and Doppler echocardiography [3], [4].

The impedance measurement is carried out at a frequency in the range 20 kHz - 100 kHz and a low intensity current (< 5 mA) to avoid stimulation of muscles and nerves [1], [18]. The lower limit of 20 kHz is used to easily separate the impedance signals from the frequency range of other bio-electric signals such as ECG and EMG [1] and reduces the electrode-tissue contact impedance. The upper limit of 100 kHz is used since at higher frequencies parasitic impedances come into play causing errors in the measurement process. In the selected frequency range the impedance is almost resistive and although the term impedance is used, it basically refers to resistance.

The thoracic impedance consists of two components. One component is the basal impedance due to the organs, muscle, bone etc. present in the thorax, which stays relatively constant with time. The other is the time-varying component superimposed on the basal

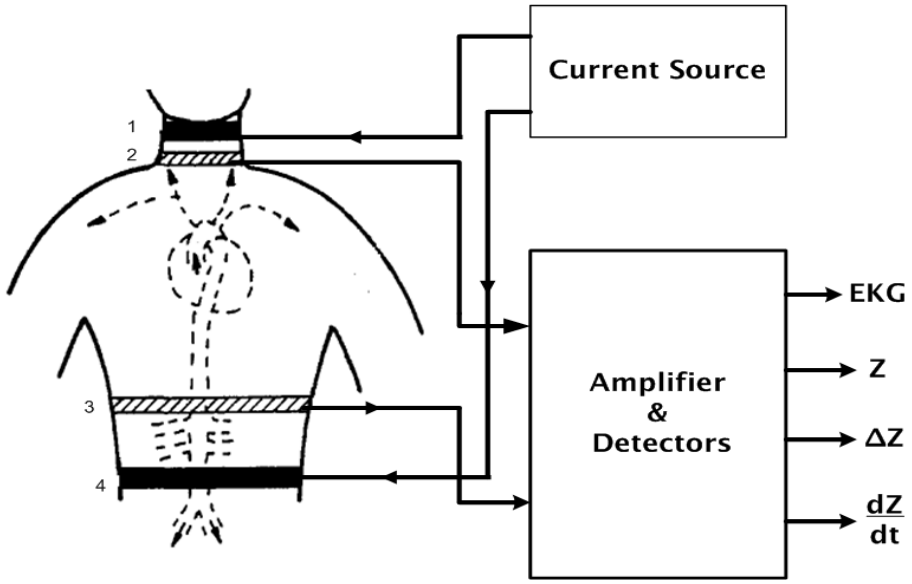

Figure 2.3 Block diagram of an impedance cardiograph (adapted from [19]).

impedance, and it varies with the cardiac cycle. Typically the basal impedance of the thorax is around 25 Ω and the change in impedance is around 0.1 - 0.2 Ω [5], [6].

2.4 Electrodes

In impedance cardiography, electrodes are used for injecting current into the thorax and sensing voltage developed across it. The current-injecting electrodes are placed across the thorax with one electrode placed at the base of the neck and the other electrode placed around the thorax at the xiphoid level [19] as shown in Figure 2.3. The voltage developed across the thorax can be sensed using the same electrodes. Although this electrode arrangement requires less number of electrodes but the changes in the contact impedance of either electrode corrupts the sensed voltage [1]. A four-electrode arrangement is more widely used in which the voltage-sensing electrodes are different from the current-injecting electrodes. These electrodes are placed in the region enclosed by the two current injecting electrodes. As a high input-impedance amplifier is used to sense the voltage, the voltage measured is not affected by the contact impedance of the voltage-sensing or current-injecting electrodes [1], [18]. The voltage sensing electrodes should be placed in the region having approximately uniform current density so that the impedance variations can be faithfully correlated with the stroke volume.

The current density in the thorax to a large extent depends on the type of current injecting electrodes used [1]. Generally two types of electrodes, namely, spot and band electrodes are used. The current density excited by these electrodes in a homogeneous conductivity cell is

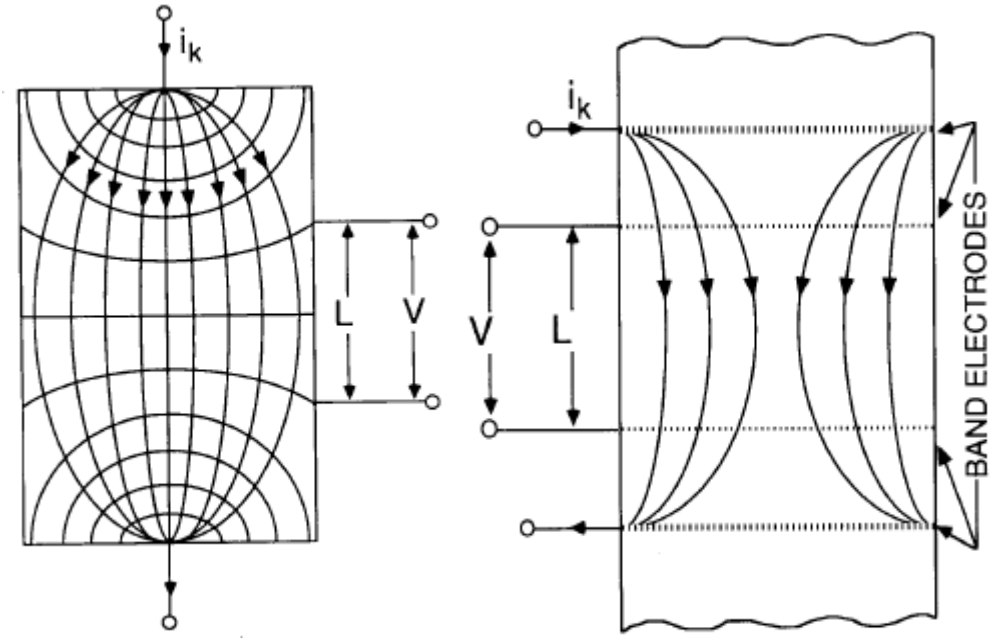

Figure 2.4 Current and potential distribution in a conductivity cell when excited using spot and band electrodes (adapted from [1]).

shown in Figure 2.4 [1]. As can be observed, the current density distribution is non-uniform along the length and becomes approximately uniform as one moves away from the current injecting electrodes. Hence some distance should be maintained between the current injecting and voltage sensing electrodes to obtain a linear relationship between the stroke volume and impedance change. On the thorax surface, placing of spot electrodes is more practical, but the corresponding current density is highly non-uniform [1]. Hence relating the changes in the impedance to the voltage recorded externally becomes difficult. The band electrode arrangement results in a relatively more uniform current density and provides a consistent and repeatable signal with lesser amplitude and waveform shape variability [2]. But they are difficult to apply in clinical settings, are uncomfortable to wear, and expensive [15]. It has also been reported that spot electrodes result in lower motion artifact [6].

2.5 Models and Equations

A typical impedance waveform along with its negative first derivative called impedance cardiogram (ICG) [5] and ECG is shown in Figure 2.5. In the ICG waveform as shown in Figure 2.5, the A point is the downward deflection due to the contraction of atria, the B point coincides with the opening of the aortic valve, the C point is the peak occurring during systole due to increased blood flow in the aorta, the X point coincides with the closure of the aortic valve, and the O point is the diastolic upward deflection, the maximum of which coincides with the opening snap from the mitral valve [15], [16]. The duration T_{LVET} is the left ventricular ejection time and $-(dZ/dt)_{\max}$ is the ICG peak and occurs during the systole.

To quantify the change in impedance in terms of the volume changes in the thorax during systole, a parallel column model [2] is used. The thorax is modeled to have conducting material with constant impedance Z_o connected in parallel with a cylindrical column with variable impedance having a uniform cross-sectional area A, length L, and a known resistivity ρ, as shown in Figure 2.6. As the cross sectional area (and hence volume) of the cylinder varies from zero to a finite value, a variable impedance change, $\Delta Z(t)$, is measured across the parallel columns. This model assumes that there is no outflow of blood from the thorax during systole and the volume of the variable impedance column is zero before systole. Hence the maximum change in the impedance ΔZ and the maximum change in the volume ΔV can be related as [2],

$$\Delta V = \frac{\rho L^2}{Z_0^2}\Delta Z \tag{2.1}$$

To take into account the blood that leaves the thorax during the later part of the systole, a forward extrapolation technique is used [2]. This procedure assumes that the blood flow profile is a square wave lasting until the end of the systole. The extrapolation of ΔZ is

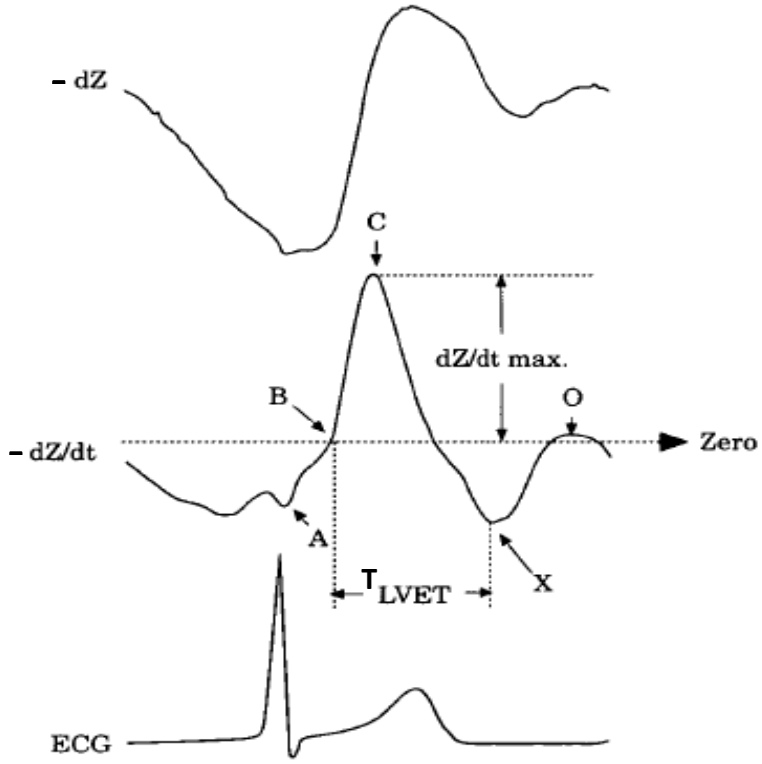

Figure 2.5 A characteristic dZ and –dZ/dt waveform obtained from the thorax, adapted from [15].

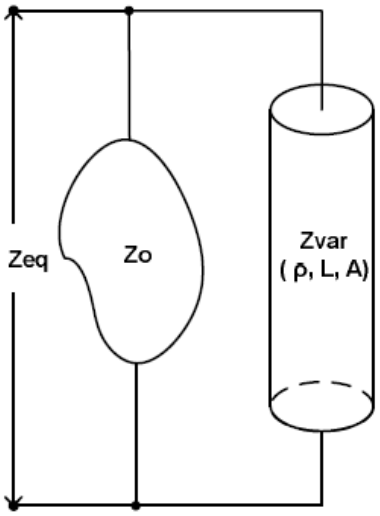

Figure 2.6 Parallel column model [2].

obtained by using the product of $(-dZ/dt)_{\max}$ and T_{LVET}. The modified form of equation [2], also known as Kubicek's equation, is given as

$$\Delta V = \left(\frac{\rho L^2}{Z_0^2}\right)\left(-\frac{dZ}{dt}\right)_{\max} T_{LVET} \tag{2.2}$$

The volume change ΔV is an estimate of the stroke volume, ρ is the resistivity of blood, and L is the distance between the voltage sensing electrodes. The Kubicek's equation has limitations like assumption of thorax as a cylinder, difficulty in determining the resistivity ρ of blood and in the measurement of L [17]. Sramek *et al.* [15], [17] proposed an alternative equation, modeling the thorax as a truncated cone. In this equation, the resistivity value is replaced by a value dependent on Z_o, L, and volume V. The volume is estimated to $L^3/4.25$ and L was found to be equal to 17% of a person's height H [17]. So the Sramek equation is,

$$\mathrm{SV} = \frac{(0.17H)^3}{4.25Z_0}\left(-\frac{dZ}{dt}\right)_{\max} T_{LVET} \tag{2.3}$$

The Sramek equation introduces an error if a person's morphological makeup significantly differs from the ideal body make-up assumed in deriving the equation. Bernstein gave a correction factor δ to scale the equation for deviation from ideal body weight [15], [17], leading to the Sramek-Bernstein equation

$$\mathrm{SV} = \delta\frac{(0.17H)^3}{4.25Z_0}\left(-\frac{dZ}{dt}\right)_{\max} T_{LVET} \tag{2.4}$$

The Sramek-Bernstein equation uses both height and weight to estimate the electrode distance and the thoracic area instead of using the actual electrode distance L. The benefits of this formula include the ability to account for the morphological makeup of an individual, elimination of the need to determine resistivity of blood ρ, and a decreased effect of basal impedance Z_o [17].

Chapter 3

INSTRUMENTATION FOR IMPEDANCE CARDIOGRAPHY

3.1 Introduction

Impedance cardiograph generally consists of a current source, current injecting and voltage sensing electrodes, impedance detector, differentiator, and ECG extractor [7] - [10]. A block diagram of the ICG hardware is shown in Figure 3.1.

The current source injects a high frequency and low amplitude current into the thorax through the current-injecting electrodes. The voltage developed across the thorax is sensed by the voltage-sensing electrodes and given to the impedance detector. The impedance detector consists of a high input impedance voltage-sensing amplifier, a demodulator and a baseline restoration circuit. The voltage-sensing amplifier amplifies the high frequency signal while rejecting artifacts and other noises. The demodulator extracts the impedance variation signal by amplitude demodulation. The baseline restoration removes the DC component for further amplification of the signal. The differentiator differentiates the impedance signal to give the ICG - (dz/dt) waveform. The ECG extraction circuit extracts the ECG signal from the voltage

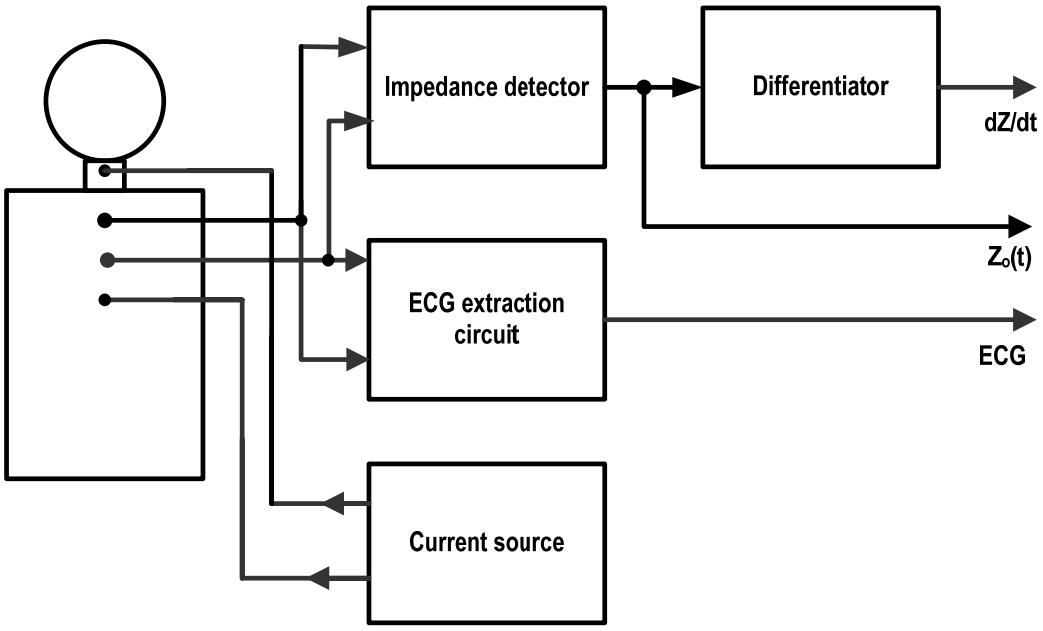

Figure 3.1 Block diagram of the instrumentation for impedance cardiography [10].

sensed by the voltage-sensing electrodes which is then used as a reference signal for processing of the ICG waveform.

3.2 Current Source

The current source basically consists of an oscillator which generates a voltage at a particular frequency and a voltage-to-current converter which converts the generated voltage into current.

The current injected by the current source should remain constant while the impedance is being measured. Hence the oscillator used should have high amplitude stability, as any variation in the amplitude contributes to noise in the demodulated output. Several realizations of the oscillator have been reported. Manigandan [7] and Naidu [8] used Wein-bridge oscillators to realize the current source. To improve the amplitude stability Venkatachalam [9] modified the Wein-bridge oscillator by introducing an amplitude stabilization loop using a peak detector and error amplifier. The frequency of a Wein-bridge oscillator cannot be varied easily. Use of voltage controlled oscillator (VCO) based circuits [20] permits a convenient control of the frequency using analog or digital means. Sarvaiya *et al.* [21] used a precision function generator IC and Patil [4] reported a circuit based on direct digital synthesizer (DDS) IC. The DDS based implementations have excellent waveform stability [10].

The voltage-to-current converter converts the voltage signal generated by the oscillator into a current. It should provide high output impedance so that the current injected into the thorax is independent of the impedance. Also its functioning should not get affected by common mode pick up, stray currents, and stray capacitances. The simplest realization of a voltage-to-current converter is an op amp based inverting amplifier with the load connected in feedback as shown in the Figure.3.2. I1 and I2 are the current-injecting electrodes and E1 and

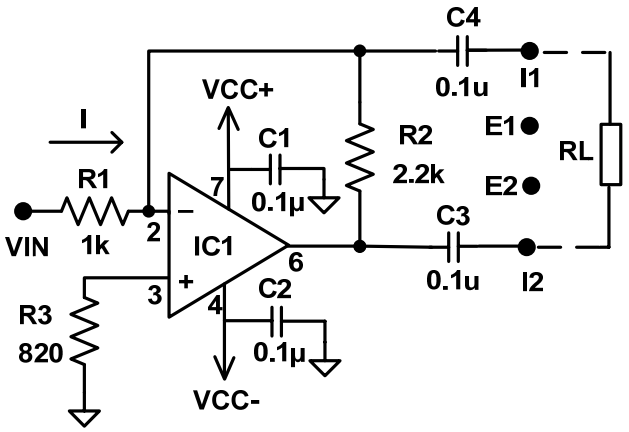

Figure 3.2 Circuit diagram of V-I converter with the load connected in feedback [10]. (IC1: LF356)

E2 are the voltage-sensing electrodes. The current injected (I) is given by, $I = V_{in} / R_1$. The capacitors are used to block DC current flow through the electrodes. The problem with this circuit is that one of the electrodes is at virtual ground and hence the terminal voltages are imbalanced with respect to ground. Therefore this circuit is prone to stray currents and common mode pick up [7] - [10]. Also stray capacitances on the virtual ground terminals may lead to instability. Venkatachalam [9] used a pulse transformer to connect the load and hence generate a balanced current source. Manigandan [7] and Naidu [8] used a transformer-less balanced current source as shown in Figure. 3.3. The load current is given as, $I = - V_{in} / R_1$. The voltage at the load terminals are given as,

$$V_X = -V_Y = 0.5\frac{R_L}{R}V_{IN} \tag{3.1}$$

Thus the terminal voltages are balanced with respect to ground. But, as one of the load terminals is still connected to op amp inverting input, it can lead to instability due to stray capacitances.

Patil [10] used a modified Howland current source as shown in the Figure 3.4, with

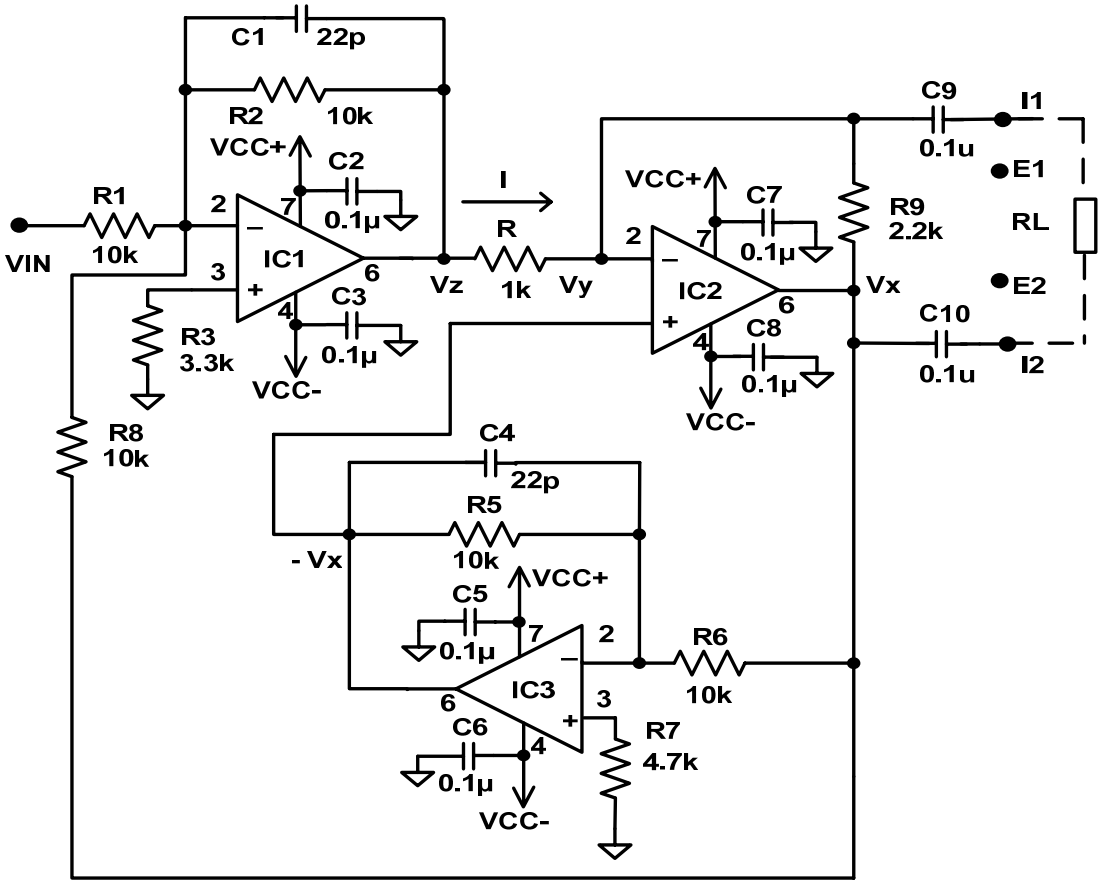

Figure 3.3 Circuit diagram of transformerless balanced current source [7], [8]. (IC1 - IC3: LF 356)

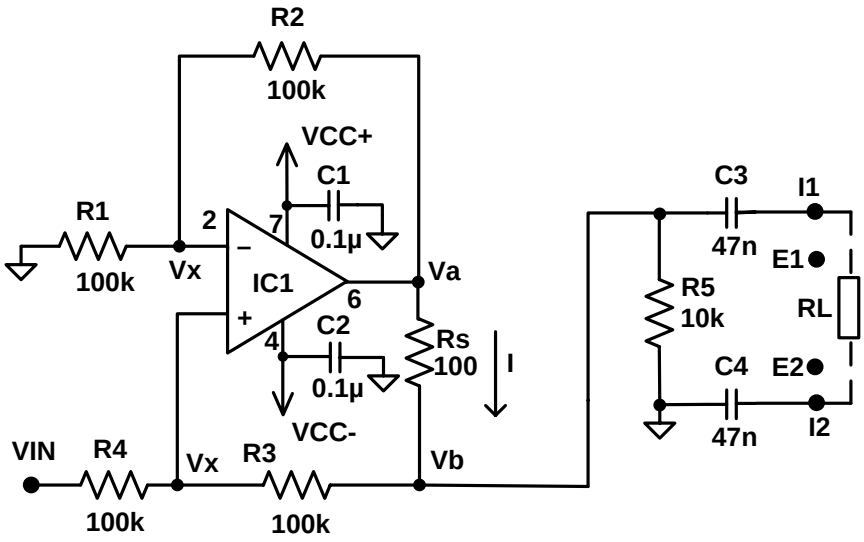

Figure 3.4 V-to-I converter based on modified Howland current source [10]. (IC1: LF356)

one terminal of the load being grounded. In this circuit, $I_L \approx I = \text{Vin} / R_s$. Since none of the load terminals are connected to the op amp inverting terminal, instability due to stray capacitances at the op amp input terminals is reduced. Also, in this circuit, high output impedance can be achieved if the resistance ratios R_2 / R_1 and R_3 / R_4 are matched. Hence high output impedance can be achieved if the resistances are properly matched. One circuit reported by Lee *et al.* [22] used digital potentiometers to achieve matching between the resistances. In this circuit, the output current was measured by sensing the voltage across a small resistance placed in series with the load and then varying the digital potentiometers to achieve the desired output impedance. This circuit can be connected to the load through a transformer to reduce the problems of the common mode pick up.

3.3 Voltage-sensing Amplifier

The voltage sensed by the voltage-sensing electrodes is amplified by the voltage-sensing amplifier in the impedance detector. This amplifier should have high input impedance, high CMRR, and a high pass response (> 10 kHz) so that it amplifies only the desired high frequency signal while rejecting the artifacts and other bio-potential signals [7] - [10]. Three op amp instrumentation amplifier was used by Manigandan [7] and Naidu [8]. To improve the performance, Venkatachalam [9] and Patil [10] used instrumentation amplifier IC as it provides very high CMRR over a wide frequency range.

3.4 Demodulator

The voltage sensed by the impedance detector is amplitude modulated and after amplification by the voltage-sensing amplifier it must be demodulated to get the signal related to impedance variation. The major challenge in demodulation is that the impedance of the thorax varies by a

very small amount and hence the modulation index is very low (0.2 - 2%). Hence the demodulator should provide high sensitivity, carrier ripple rejection, and noise rejection.

Manigandan [7] and Venkatachalm [9] used a diode based full-wave precision rectifier, as in [6], to rectify the sensed voltage and then low-pass filtered it to remove the carrier ripple and obtain the demodulated signal. To improve the high-frequency performance of the diode based circuit, Sarvaiya *et al.* [21] used a voltage-clamp amplifier IC (AD8037) for the rectification. Naidu [8] reported a demodulation scheme based on vector lock-in amplifier with synchronous detection.

Patil [10] reported a slicing amplifier based demodulation circuit as shown in Figure 3.5. This circuit uses the concept of slicing the top of the amplitude modulated voltage up to the modulation depth and then amplifying the sliced signal prior to synchronous detection, as reported earlier by Fourcin [23] The circuit uses two voltage clamp amplifier ICs, IC1 and IC2. If the lower threshold pin V_L of the IC is connected to the input it acts as a full-wave rectifier and if it is set to some other threshold value then the input signal gets clipped at that threshold. IC1 is configured as a full-wave rectifier and IC2 is used as a slicing amplifier for slicing the full wave rectified output at the slicing threshold set by the potentiometer R_{pot}. The

$$V_Y = \frac{R_7}{R_7 + R_6} V_X \tag{3.2}$$

When $V_2 > V_Y$, the output is given as

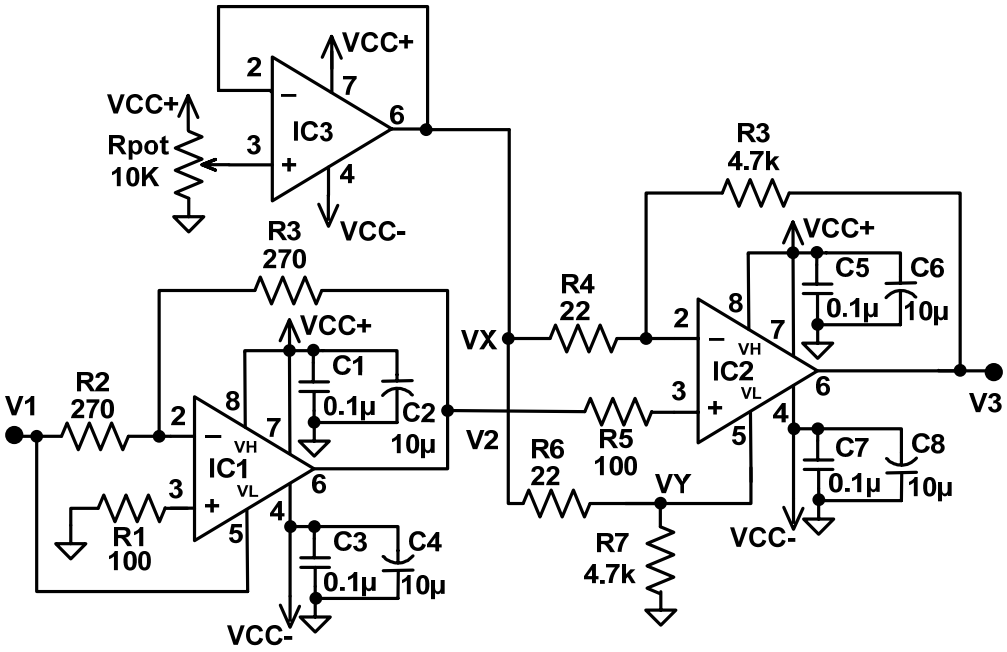

Figure 3.5 Slicing amplifier using voltage clamp amplifier IC [10]. (IC1: LF356, IC2 and IC3: AD8037)

$$V_3 = V_2\left(1+\frac{R_3}{R_4}\right) - \frac{R_3}{R_4}V_X \tag{3.3}$$

With $R_7 = R_3$ and $R_6 = R_4$, Eq. (3.10) can be written as,

$$V_3 = \left(V_2 - V_Y\right)\left(1+\frac{R_3}{R_4}\right) \tag{3.4}$$

For $V_2 < V_Y$, the output is given as

$$V_3 = V_Y\left(1+\frac{R_3}{R_4}\right) - \frac{R_3}{R_4}V_X \ = 0 \tag{3.5}$$

For $V_I > V_Y$, the output voltage is the difference between input and reference voltage set using the potentiometer, and the difference voltage is amplified with the gain set by the ratio R_3/R_4. For $V_I < V_Y$, the output is zero. Thus the circuit works as a slicing amplifier with a gain of $1+R_3/R_4$ and the slicing threshold V_Y set by the potentiometer R_{pot}.

The slicing method significantly improves the demodulator sensitivity but introduces a large amount of carrier ripple. Hence a higher order low pass filter is required to reject the carrier ripple which further leads to more phase distortion. To achieve high sensitivity as well as good ripple rejection without introducing distortion, demodulation using synchronous sampling was used by Patil [10]. In this technique a sample-and-hold circuit is used for sampling the sliced signal near the peak and holding the value until the next peak. Hence the carrier ripple is eliminated. Although this method provides high sensitivity and good ripple rejection but it is sensitive to noise since any noise near the peaks will also get sampled and corrupt the output.

3.5 ECG Amplifier

The ECG amplifier is used to extract the ECG signal from the voltage signal sensed by the voltage sensing electrodes. The R peaks of the ECG waveform are used as a reference. The ECG signal is extracted by using an active band pass filter in the range 1.6 Hz to 20 Hz [7] - [10]. The signal obtained is used only as reference and is not suitable for physiological assessment.

3.6 Baseline Restoration Circuit

Bio-electric signals like ECG and ICG have the signal component superimposed on a baseline. In practical setups, the baseline varies over a large range which can be many times greater than the signal excursion. This drift in the baseline may be caused by body movement and other motion artifacts, change in environment and/or body temperature, offset drift in analog signal conditioning circuits etc. There is a need to correct this baseline drift as it can

lead to saturation of the analog processing circuits and reduction in the input dynamic range of the data acquisition circuits. It is possible to efficiently correct the baseline drift using digital signal processing algorithms as reported in [24]. But these methods can be useful only if the combined signal (signal + drift) can be digitized by high-precision ADC without crossing its input range.

Although the drift in the baseline is relatively slow, it cannot be removed by high pass filtering since its spectrum partially overlaps with the impedance signal spectrum. One method to cancel the drift as reported in [25] first amplifies the signal and then divides it into two channels. In one channel, the signal is low pass filtered to extract the drift component and in the other channel the signal is delayed using an analog time delay circuit. The drift is then subtracted from the delayed signal to obtain a drift free signal. This method requires the delay of the analog time delay circuit to be exactly matched to the delay required by the low pass filter to extract the drift signal. As no drift correction is applied in the first amplifier stage, it can get saturated and the correction in the next stage will not be of any help. Other methods like self-balancing method [26] and successive approximation register (SAR) based method [27] have also been reported. Depending upon the extent of the drift the self balancing system can require upto $2n$ clock cycles for an n-bit DAC. The SAR method requires n clock cycles for an n-bit SAR but the signal is not usable during the correction interval. One can introduce some kind of gain control before the signal is sampled by the ADC, but that would attenuate the signal as well, resulting in loss in SNR.

Tracking can be used for a faster restoration of the baseline to keep the signal within the input range of the ADC. If required, digital signal processing can be used for further correction. A tracking based baseline restoration circuit was developed by Pandey *et al.* [28], [29] as a part of an impedance cardiograph instrument. The circuit tracks the input signal to determine whether it is lying between two predefined threshold levels or going out of the threshold range as described below.

3.6.1 Tracking Based Baseline Restoration Circuit

As shown in the block diagram in Figure 3.6, the output of the amplifier (A) is given to a threshold detector which determines whether the signal is within the threshold limits [V_{t1}, V_{t2}]. Whenever the signal crosses the threshold limits the threshold detector drives an up/down counter which increases or decreases its count depending upon the direction in which the signal is drifting. The counter value is then fed to a DAC which produces the correction voltage to be subtracted from the signal.

In the implementation reported in [29] the up/down counter was implemented in software inside a microcontroller. The complete circuit diagram of the circuit is shown in Fig 3.7. In this circuit, the threshold detector is formed by the op amps IC1B and IC1C which are used as

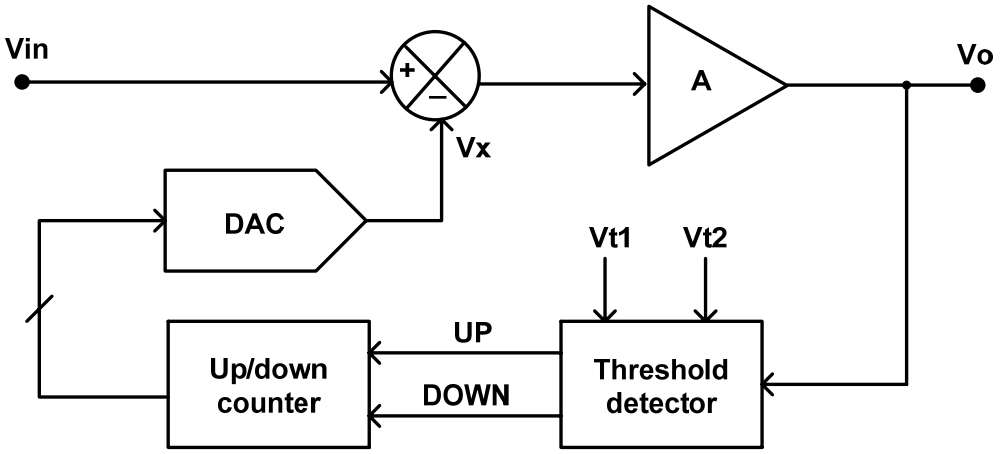

Figure 3.6 Block diagram of the baseline restoration circuit. [29]

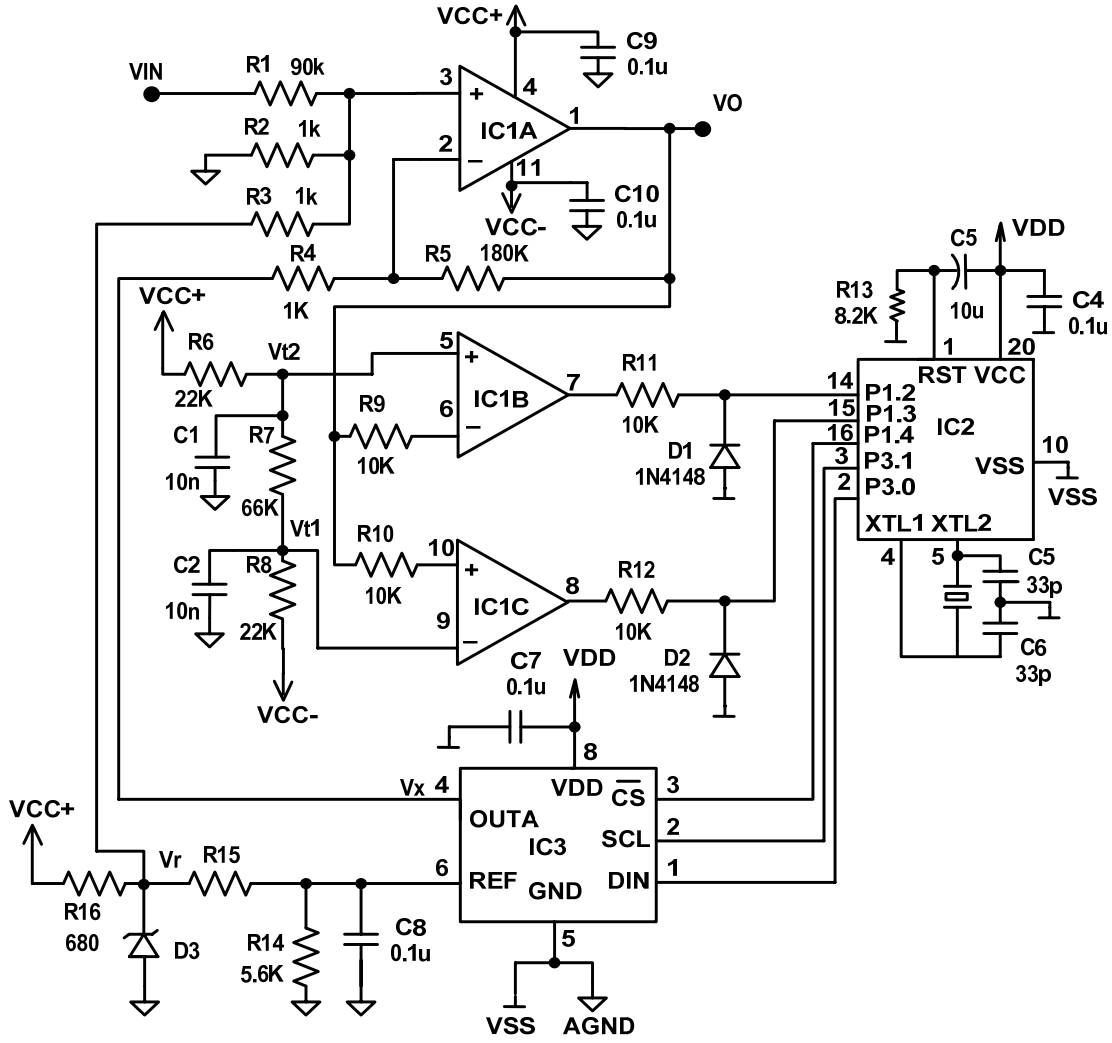

Figure 3.7 Circuit diagram of baseline restoration circuit as used in [29]. (IC1: TL084, IC2: AT89C2051, IC3: TLV5618A, Vcc+=5V, Vcc-=-5V, VDD=+5V)

comparators. They compare the output voltage V_o with the threshold levels [V_{t1}, V_{t2}] which are set using a resistive divider. The output of each comparator is given to separate pins of the microcontroller IC2. The microcontroller scans these pins and updates a software counter if any of the comparator outputs go low. In order to generate the correction voltage, the counter value is given to a serially interfaced (SPI) 12-bit DAC (IC3). The correction voltage generated by the DAC is given to the op amp IC1A which is used as a summer for the input voltage V_{in}, reference voltage V_r, and the correction voltage V_x. The microcontroller and DAC are powered by a single 5 V supply and the quad op amp IC1 is powered by ± 5 V supplies. Hence the circuit is capable of handling bipolar inputs. The output of the summer is given as,

$$V_o = A_s V_{in} - A_x\,(V_x - A_r\,V_r/A_x) \tag{3.6}$$

where $A_s = (R_2 || R_3/(R_1 + R_2||R_3))(1 + R_5/R_4)$, $A_r = (R_1 || R_2/(R_3 + R_1||R_2))(1 + R_5/R_4)$ and $A_x = R_5/R_4$.

The signal gain A_s is selected such that for no baseline drift, the amplified input does not make the output V_o cross the output threshold range, that is, $A_s = (V_{t2}\text{-}V_{t1})/(V_{s\,max} - V_{s\,min})$ If the output V_o goes above the upper threshold the up/down counter is incremented by one step and hence the correction voltage from the DAC gets incremented by one step. Similarly the DAC correction voltage is decremented by one step whenever the output crosses the lower threshold. Thus, the correction voltage V_x is given by,

$$\begin{aligned} V_x(t_{n+1}) &= V_x(t_n) + \Delta V_x, && V_o(t_n) > V_{t2} \\ &\quad V_x(t_n) - \Delta V_x, && V_o(t_n) < V_{t1} \\ &\quad V_x(t_n)\ , && \text{otherwise} \end{aligned} \tag{3.7}$$

The step voltage ΔV_x depends on the number of steps 'N' in the DAC and is equal to $\Delta V_x = (V_{x\,max} - V_{x\,min})/N$ where $(V_{x\,max} - V_{x\,min})$ is the full scale swing of the DAC. Accordingly the correction gain A_x is selected as $A_x = 0.5(V_{t2}\text{-}V_{t1})/\Delta V_x$ so that one step increment in the correction voltage brings the signal back to the middle of the output threshold range.

The circuit can be modified so that the microcontroller and the op amps are powered by a single supply eliminating the need of generating a negative supply.

3.6.2 Modified Circuit

The circuit can be further simplified by using a microcontroller which has an inbuilt ADC and DAC as shown in the block diagram in Figure 3.8. The use of inbuilt ADC eliminates the need of comparator based external threshold detection circuitry. Once the

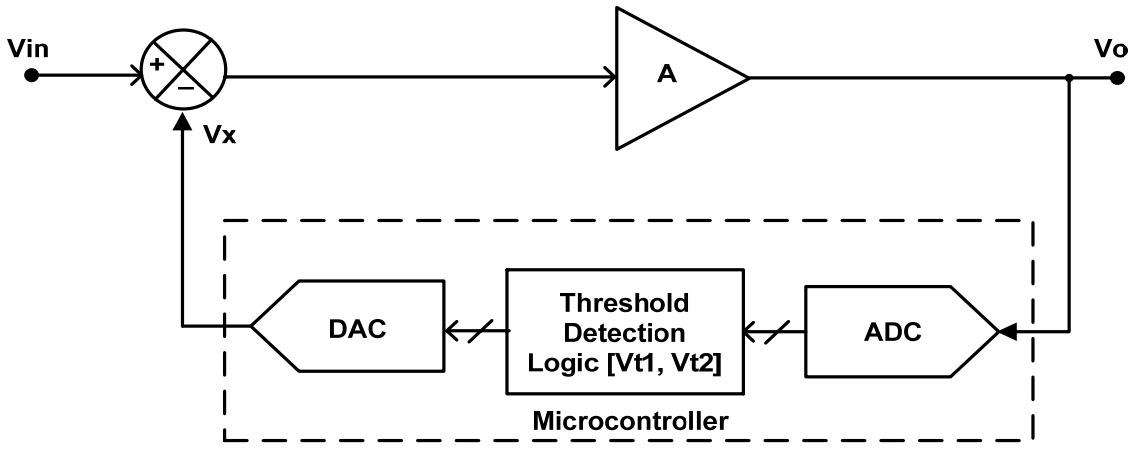

Figure 3.8 Block Diagram of modified baseline restoration circuit.

signal has been sampled by the ADC, the threshold detection can be in software itself and accordingly a data byte can be written to the DAC to generate the correction voltage. As the thresholds are set in the software, they can be changed easily. Also by using interrupts, the ADC and DAC modules can be made to run independent of the CPU of the microcontroller keeping it free for doing other operations. Since the circuit is to be used as a part of an ICG instrument, the overall circuit can be simplified by using microcontroller which can be used for other operations of the circuit as well.

As evident from Eq. (3.13), the signal gain A_s and the correction gain A_x cannot be set independently of each other in the previous circuit. The summer implementation can be simplified so that the two gains become independent and the need of generating the reference voltage V_r is eliminated.

The modified circuit is shown in Figure 3.9. The microcontroller selected for the implementation is dsPIC33FJ128GP802, a 28-pin chip from Microchip. It is a 16-bit digital signal controller that has all the features of a microcontroller along with a DSP engine supporting a number of DSP operations. The controller has an on-chip10-bit/12-bit ADC and 16-bit on-chip DAC [30]. The circuit requires only two pins, namely, RA0 for ADC input and RB12 for DAC output. The quad op amp IC1 is powered by a single supply of 5V and an analog reference (AREF) of 2 V generated by op amp IC1A is used to bias the signals within the supply range. The DAC output is buffered using op amp IC1C and applied as input to the inverting summer realized using IC1D. The summer adds the voltage V_s with the correction voltage V_x and generates the output voltage V_o. The output V_o is given to the pin RA0 of the microcontroller where it is sampled by the on-chip ADC. The on-chip DAC is configured to operate at a sampling rate of 1 kHz. As a result, after every 1 ms the DAC raises an interrupt

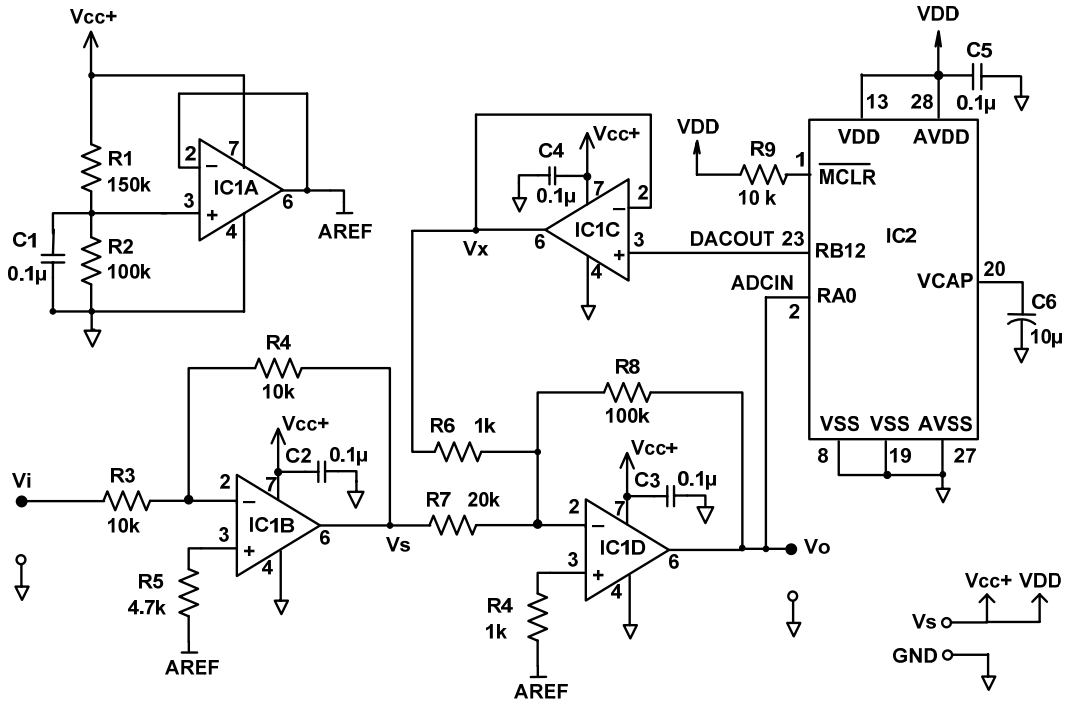

Figure 3.9 Circuit diagram of modified baseline restoration circuit. (IC1: LM324, IC2:dsPIC33FJ128GP802, Vcc+=5V, VDD=3.3V, AREF=2V)

flag and in the interrupt service routine the current value of the input, as sampled by the ADC, is compared with pre-defined upper and lower thresholds. If the sampled value is greater than the upper threshold, the output to the DAC is increased by a step corresponding to the correction step ΔV_x. Since the summer is implemented in inverting configuration the increase in the correction voltage will result in a decrease in the offset at its output. The correction gain A_x has to be selected such that for a step increase ΔV_x in the correction voltage, $A_x \Delta V_x$ brings the output V_o back to the center of the threshold range. Similarly when the sampled value crosses the lower threshold, the output to the DAC is decreased by a step which results in an increase in the offset at the output and hence the signal comes back to the center of the output threshold range. The output V_o is given as,

$$V_o = -(A_s V_s + A_x V_x) + V_{AREF} \tag{3.8}$$

or,

$$V_o = (A_s V_i - A_x V_x) + V_{AREF} \tag{3.9}$$

where $A_s = R_8/R_7$, $A_x = R_8/R_6$, and $V_{AREF} = 2$ V.

For proper operation of the circuit, the correction voltage V_x should normally be the same as the analog reference V_{AREF} and the correction voltage steps ΔV_x should be generated about this voltage. Initially if there is no offset drift in the input but the correction voltage V_x

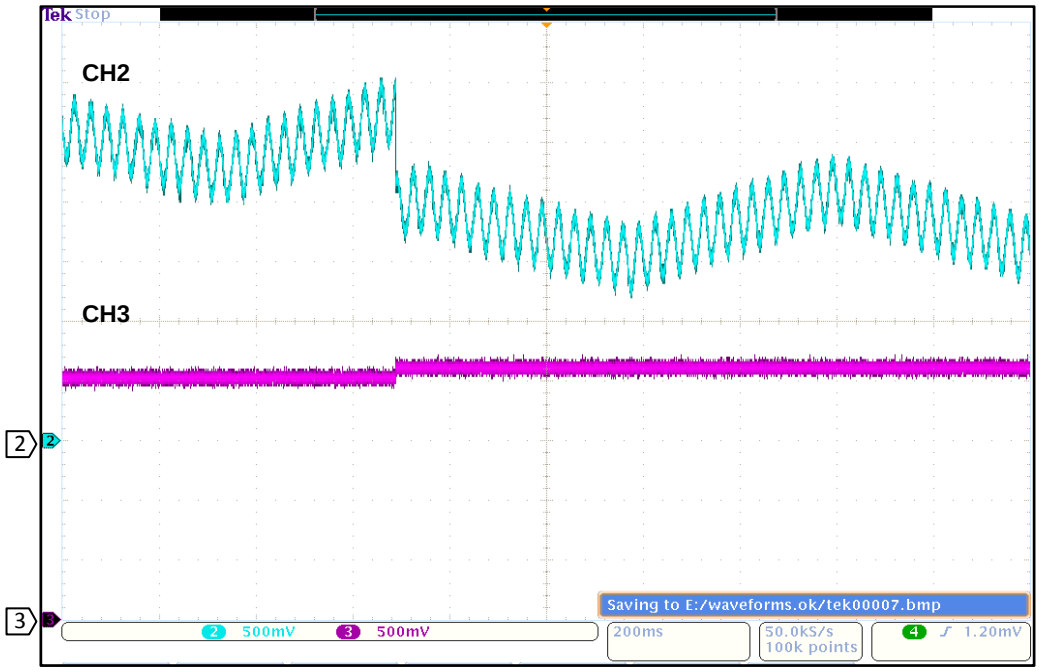

Figure 3.10 Waveforms of output V_o (CH2) and DAC correction voltage V_x (CH3).

is not matched to the analog reference, the difference will get amplified by the correction gain and can make the output signal cross the threshold range and saturate if the correction gain is considerably large. This matching either requires a high resolution DAC or changing the analog reference itself if the resolution is limited. The DAC in the selected microcontroller has 16-bit resolution and was sufficient for the application. Also if the signal gain is very large and baseline can drift over a large range then many correction steps might be required at the output. The number of correction steps depends upon the correction gain A_x, the DAC resolution and the full scale output swing of the DAC. The DAC in the microcontroller had full scale swing of 1.2 V (p-p) with maximum and minimum levels of 2.4 V & 1.2 V respectively. The microcontroller was programmed such that after power-on the DAC output was set to (V_{AREF}) and generated correction steps of 10 mV about this value. Hence it can generate 40 increasing steps and 80 decreasing steps about analog reference (V_{AREF}) depending upon the direction of baseline drift. The total number of correction steps between the full scale output levels is equal to 120.

The correction gain A_s and the correction gain A_x can be set independently of each other by changing the resistors R5 and R6, respectively. Hence the circuit can be reconfigured easily for any application depending upon the DAC resolution available and the characteristics of the input signal.

The circuit was tested by applying a sine wave input of 100 mV (p-p) swing and 30 Hz frequency superimposed on a triangular wave changing from 1.9 V to 2.1 V with a

frequency of 1 Hz. The output threshold limits were set to 3 V and 1 V and the signal gain A_s was set to 5. The DAC was configured to generate a correction voltage step (ΔV_x) of 10 mV. The correction gain A_x was set to 100 so that $A_x \Delta V_x$ resulted in 1 V (100 × 10 mV) step at the output which is half of the output threshold range. The drift cancellation done by the circuit when the input signal crosses the threshold range is shown in Figure 3.10.

3.7 Further Improvements

A study of various blocks of the hardware showed that amplitude demodulation of the voltage sensed across the electrodes is the most critical operation. The amplitude demodulation circuits generally have carrier ripple in the output. Low-pass filter for suppressing the ripple results in phase distortion. For improving the sensitivity, we need to amplify the signal, which can be done either by high-pass filter or after baseline restoration. High-pass filtering results in signal distortion. Any noise present in the input also contributes to error in the output. Synchronous demodulation, using a local reference related to the carrier, can be employed for reducing the noise. However its sensitivity is lower than that of the peak detector and almost same as the rectifier detector. Use of slicing amplifier with synchronous sampling, as used by Patil [31], improves the sensitivity and reduces the ripple, but degrades the noise performance.

To improve the noise performance, a synchronous demodulation scheme using current steering as illustrated in Figure 3.11 can be used [32]. The single-pole double-throw (SPDT) switches are controlled by a clock (V_{ref}) which is synchronous with the sinusoidal current source. The input signal V_{in} is given directly to switch S1 whereas it is inverted before being given to switch S2. During each half of the clock cycle, the switches are either connected to the op amp inverting terminal or to the analog ground. When the clock is high, switch S1 is connected to the analog ground and switch S2 is connected to the op amp input, and vice versa when the clock is low. Hence the current entering at the inverting terminal of the op amp is an inverted full-wave rectified signal. The rectified signal is then inverted and low-pass filtered by the op amp with R1 and C1 in feedback, to get the final demodulated output. Since the rectification is synchronous, only those components in the input signal are passed which are in phase with the clock signal. Noise and offset in the input get rejected in the demodulation. Hence this approach has better noise and interference rejection capability.

Resistances are used in series with the input of the switches to convert the input voltage into current so that it is either steered to the analog ground or to the op amp inverting terminal which is at virtual ground. Since the switches are either connected to the analogground or to the op amp inverting terminal which is at virtual ground the voltage across the switches remains zero. Hence there is no noise due to transients caused by voltage switching. This approach is based on synchronous current steering and it does not result in

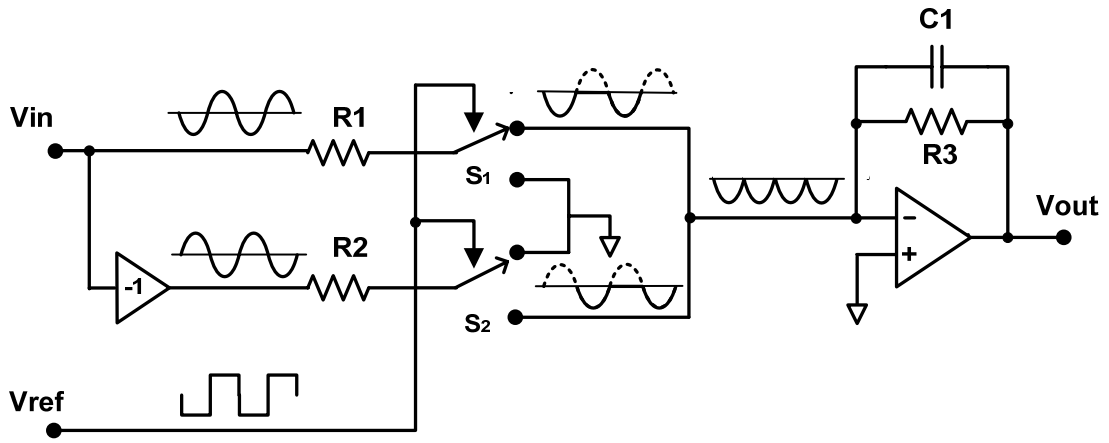

Figure 3.11 Demodulation using synchronous current steering. R1=R2.

any sharp transitions at the input and output terminals of the op amp. Hence the circuit performance is not affected by the slew rate of the op amp. In circuit with analog switches, the output generally gets corrupted due to charge injection through the stray capacitance between the control input and the output terminals of the switch. A correction for this charge injection is often needed [33]. Our demodulator circuit uses a SPDT switch which internally has two analog switches with complementary controls and hence the charge injection through the two controls should approximately cancel each other. In case the two controls have a delay, there may be a glitch at the output which will get filtered out by the low-pass filter at the output.

The current I_{bc} injected at the op amp input terminal using V_{bc} and R_{bc} can be used for introducing a negative offset and hence can be used for baseline correction. Use of a fixed dc bias for baseline correction restricts the gain (R3/R1) of the circuit and hence its sensitivity. As a further improvement in the circuit, we can use a sinusoidal voltage for baseline correction as shown in Figure 3.12. Switches S3 and S4 operate in the same fashion as switches S1 and S2, but, since their input polarities are reversed, the full-wave rectified signal at their output is of opposite polarity and hence gets subtracted from the rectified signal. A large gain (R3/R1) can be used in the low-pass filter to amplify the difference and hence achieve high sensitivity. The baseline can be controlled by varying the amplitude of the signal V_{bc}.

This circuit can be used for automatic baseline correction within the demodulator itself by continuously monitoring the demodulated output and controlling the amplitude of the correction signal (V_{bc}) for keeping the demodulated output within a predefined threshold range, by implementing the tracking baseline correction method of [29]. In this circuit, the

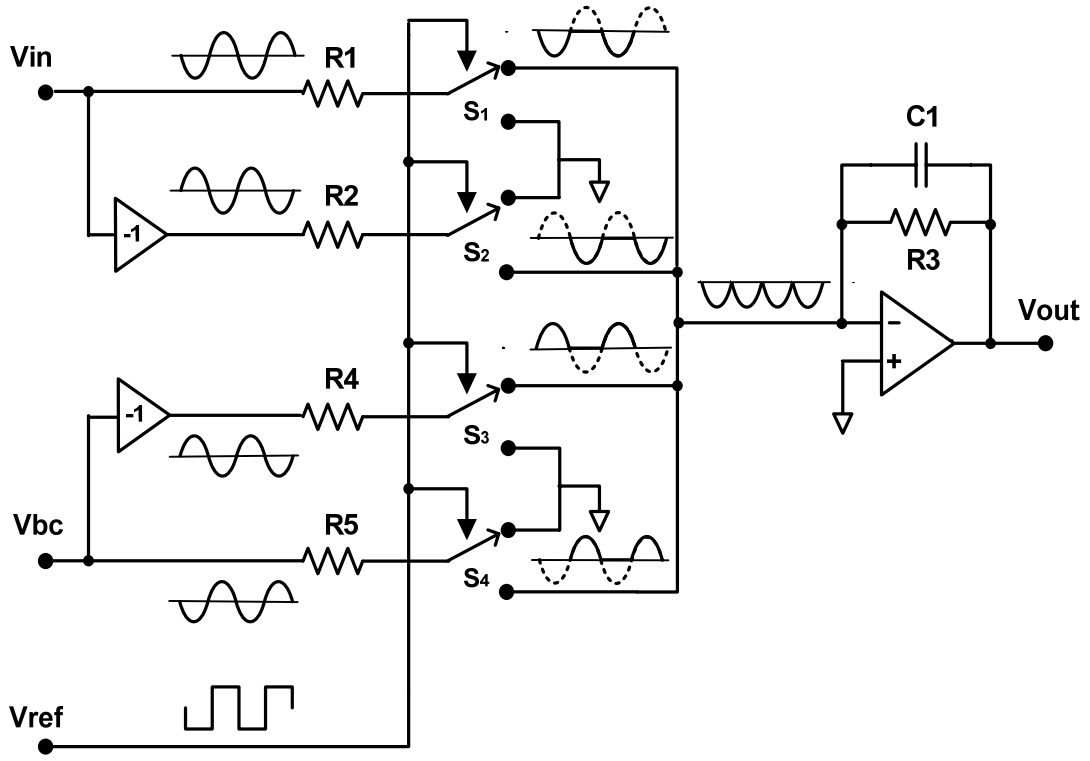

Figure 3.12 Demodulation using synchronous current steering with baseline correction. R1=R2, R4=R5.

difference between half-wave rectified versions of the input and baseline correction signal varies slowly. Hence the output can be tracked by the baseline correction loop while simultaneously achieving high sensitivity.

Any carrier ripple present in the output can be rejected by sampling the output using an ADC with the sampling instant synchronized with the peaks of the carrier signal. Hence this demodulation approach provides better carrier ripple rejection, in addition to noise rejection and high sensitivity. The baseline correction loop is a part of the demodulator itself and no separate hardware is required as used in the earlier designs [7] - [10].

In summary, this circuit can be used for improving the performance of an impedance cardiograph for sensing a noise and distortion-free ICG signal. For realizing this circuit, we need high speed analog switches, and the two switches forming the 1:2 demultiplexer should have symmetry in their operation. An instrument design based on this synchronous demodulator is presented in the next chapter.

Chapter 4

HARDWARE AND SOFTWARE DESIGN

4.1 Introduction

Hardware for impedance cardiography mainly involves a current source, a voltage-sensing amplifier, a demodulator and an ECG extraction circuit [7] – [10]. The current source generates a low level current (< 5 mA) in the frequency range of 50 – 500 kHz. It consists of an oscillator for generating a sinusoidal voltage of desired frequency and a voltage-to-current (V-to-I) converter. The oscillator should have high amplitude stability and the voltage-to-current converter should have output impedance much larger than the thoracic impedance. The current generated by the current source is injected into the thorax using a pair of electrodes. In the frequency band used for impedance cardiography, the thoracic impedance is nearly resistive. Due to the variations in the thoracic impedance during each cardiac cycle, an amplitude modulated voltage is developed across the thorax. This amplitude modulated voltage is sensed using another pair of electrodes and amplified by the voltage-sensing amplifier. The amplifier should have high CMRR and it should amplify the desired high frequency signal while rejecting other bioelectric signals and noise. A high-pass filter with cut-off greater than 10 kHz can be used before the amplifier for this purpose. The demodulator demodulates the amplitude modulated voltage amplified by the voltage-sensing amplifier to extract the impedance variations. Since the thoracic impedance varies by a very small amount (0.1 – 2%), the modulation index is very low. Hence the major challenge in the design of demodulator is its sensitivity so that it is able to detect the small amplitude variations. Also it should provide good noise rejection, carrier ripple rejection and low distortion. The ECG extraction circuit uses the same pair of electrodes as used for voltage sensing. It consists of an instrumentation amplifier and a band-pass filter that rejects dc as well as high frequency signals above the normal ECG range. The ECG obtained is used as a reference for processing the ICG signal and is generally not used for diagnostic purpose.

After studying the earlier designs [7] – [10] it was decided to use DDS based waveform generator as it provides high amplitude stability and convenient frequency control. Further in our synchronous demodulator as described in Section 3.7, we need a square wave for controlling the analog switches. Two DDS ICs have been used to generate synchronized sinusoidal and square waveforms with an adjustable phase shift. The sinusoidal signal is used for generating the excitation current and the square wave is used as the reference clock for

synchronous demodulation. The phase shift can be adjusted to compensate for any phase shift in the sensed voltage. A modified Howland current source has been used in the V-to-I converter to achieve high output impedance. A transformer has been used at the output of current source to achieve balanced outputs and hence reduce the common-mode pick-up. The major contribution in the new design is the demodulator block wherein a synchronous demodulation scheme has been implemented using analog switches to achieve high sensitivity, interference rejection, noise rejection, and low carrier ripple without phase distortion. Further, the design has baseline correction provided in the demodulator stage itself.

The hardware block diagram of the impedance cardiograph is shown in Figure 4.1. It consists of two DDS chips clocked by a 40 MHz clock generator. DDS 1 generates sinusoidal signals at the desired frequency. Its complementary outputs are given to a differential amplifier. The amplifier output gives input to the V-to-I converter and also as a correction signal to the demodulator for baseline restoration, with digital potentiometers 1 and 2 providing independent amplitude control for the two voltages. DDS 2 generates a square wave synchronous with the sinusoidal output of DDS 1 which is given to the demodulator for synchronous demodulation. The frequency and phase settings of DDS 1 and 2 and the wiper settings of the digital potentiometers 1 and 2 are configured by a microcontroller through an SPI bus. The DDS 2 output is also used to clock a timer inside the microcontroller so as to control the number of cycles after which the demodulator output is sampled by the on-chip ADC of the microcontroller.

The balanced current output from the current source is injected into the thorax through electrodes I1 and I2. The voltage developed across the thorax is sensed using the electrodes E1 and E2 and given to the voltage-sensing and ECG amplifier. The voltage-sensing amplifier output is then given to the demodulator. The demodulator uses synchronous demodulation for extracting the impedance variation $z(t)$ from the amplitude modulated output of the voltage-sensing amplifier. The clock input to the demodulator is synchronous with the voltage-sensing amplifier output. The correction signal is used for baseline restoration. The scheme of demodulation is described in detail later. The output of the demodulator $z(t)$ is given to a differentiator to get the ICG signal. It is also given to a contact impedance indicator which interrupts the controller whenever the electrode contacts are loose. The ECG acquisition block consists of an instrumentation amplifier which amplifies the signal sensed by the voltage sensing electrodes and a cascade of a low-pass and a high-pass filter that filter out other unwanted signals to extract the ECG signal. The signals $z(t)$, ICG, and ECG are also given to the microcontroller where they are sampled by the on-chip ADC. The microcontroller communicates with any external device using an isolated RS232 interface.

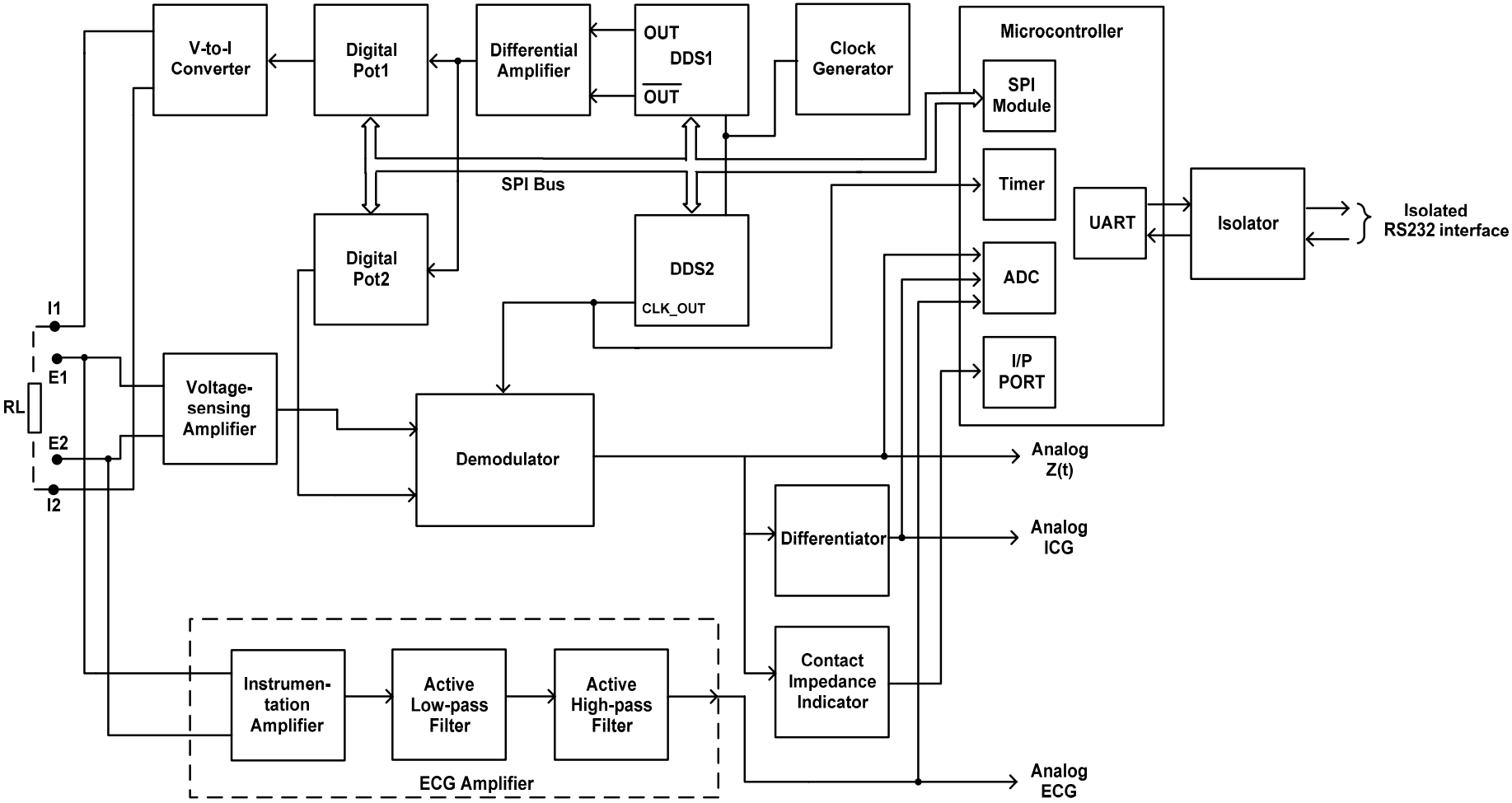

Figure 4.1 Block diagram of the hardware of the impedance cardiograph.

4.2 Current Source

The current source consists of a waveform generator which generates a voltage waveform with programmable frequency and phase, amplitude controller, and a voltage-to-current converter for converting the voltage into current.

4.2.1 Waveform Generator

The waveform generator uses two direct digital synthesizer (DDS) chips for generating voltage waveforms with programmable frequency and phase shift. The DDS chips use an internal sine look-up table and a digital-to-analog converter (DAC) to produce the sinusoidal signal. Depending upon the desired output frequency, the values from the look-up table are output at an appropriate rate through DAC to generate the waveform. They provide precise control of the frequency and phase, fast switching of frequency and phase, and excellent amplitude stability.

The DDS IC used in this project is AD9834 [11]. It can function on a clock of up to 75 MHz. For a clock frequency f_{MCLK}, the output frequency can be set between 0 to f_{MCLK} /2. It can generate sinusoidal, square, and triangular outputs. It has a 28-bit wide frequency register and 12-bit wide phase register for controlling the frequency and phase. The frequency and phase of the output waveform can be controlled by loading appropriate counts into the frequency and phase registers through a serial peripheral interface (SPI). The output frequency and phase are given as,

$$f_{out} = (f_{MCLK} / 2^{28})\, N_{FREQREG} \tag{4.1}$$

$$\theta_{out} = (2\pi / 2^{12})\, N_{PHASEREG} \tag{4.2}$$

where $N_{FREQREG}$ and $N_{PHASEREG}$ are the counts loaded in the frequency and phase registers. Also AD9834 has separate analog and digital supplies which can be set between 2.7 to 5.5 V independent of each other. This provides flexibility in interfacing it to ICs having different logic levels.

Our design uses DDS chips, namely U7 and U21, as shown in Figure 4.2. A 40 MHz crystal oscillator module SG531H (U6) has been used to provide clock to the DDS chips. The frequency, phase, and the instant of synchronization of the output of the two DDS chips is controlled by the microcontroller dsPIC33FJ128GP802 (U5) through its SPI bus. The serial clock (SCLK) and data (SDATA) pins of both the DDS chips are connected to the microcontroller port pins RB8 and RB9, respectively. The FSYNC pin of the DDS acts as a chip select and data will be clocked in only when the FSYNC pin is driven low. FSYNC pin of U7 and U21 are connected to microcontroller port pins RB10 and RB11, respectively. U7

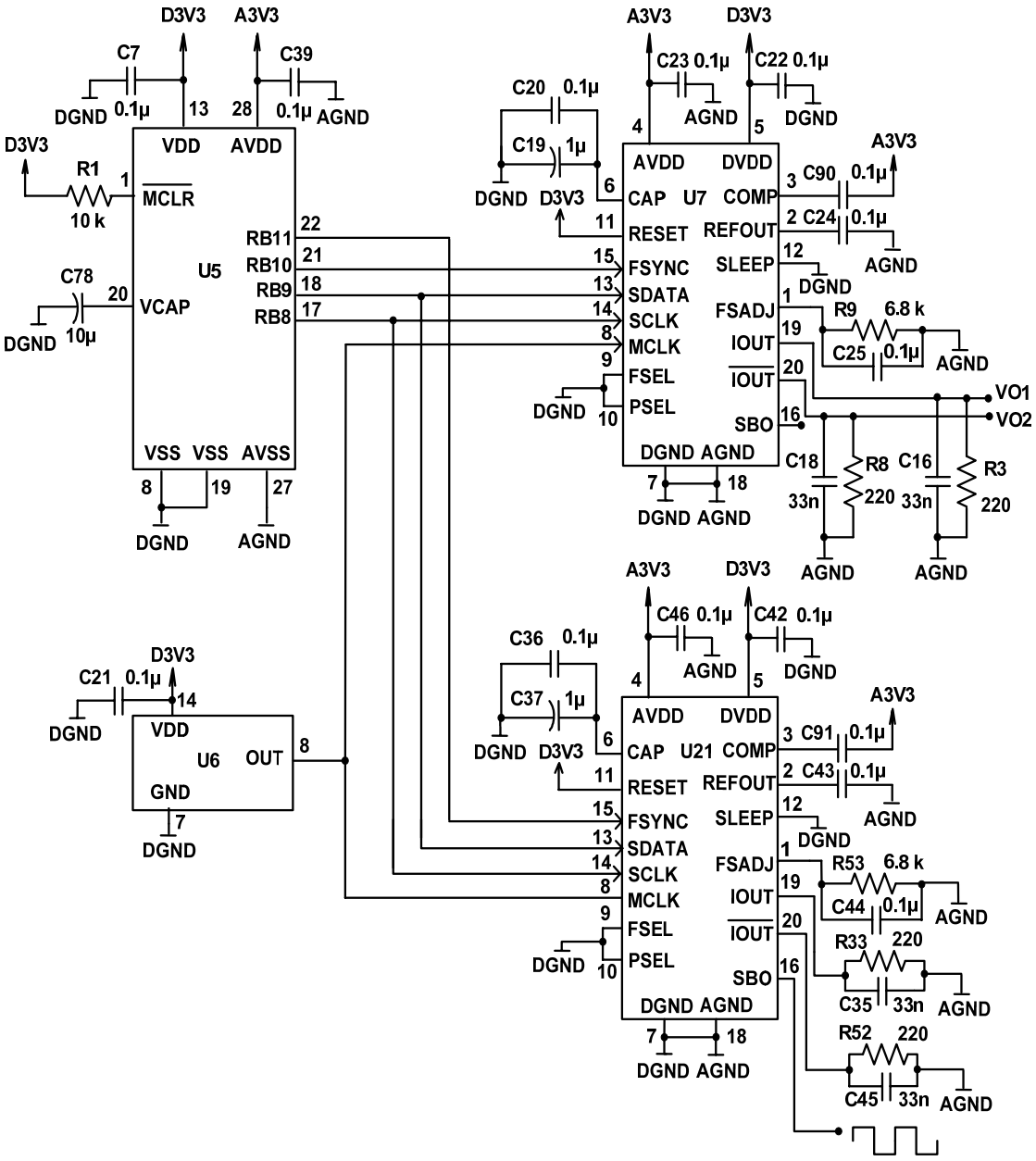

Figure 4.2 Waveform generator using AD9834. (U5: dsPIC33FJ128GP802, U7, U21: AD9834, U6: SG531H)

is configured to generate a sinusoidal signal and U21 is configured to generate a square wave by loading appropriate control words through the SPI bus. Before loading the frequency and phase registers of the DDS chips with appropriate counts, they are taken into reset state to avoid any spurious output during configuration. Resetting does not affect the frequency and phase settings, it only prevents any signals from appearing at the output. The reset can be issued in software through the SPI bus or in hardware through the RESET pin. The software approach has been used in this project as the hardware method requires an extra port pin of the microcontroller. Initialization of the DDS chips is shown in the form of flowchart in Figure 4.3. The frequency registers of both the DDS are loaded with the same count to get

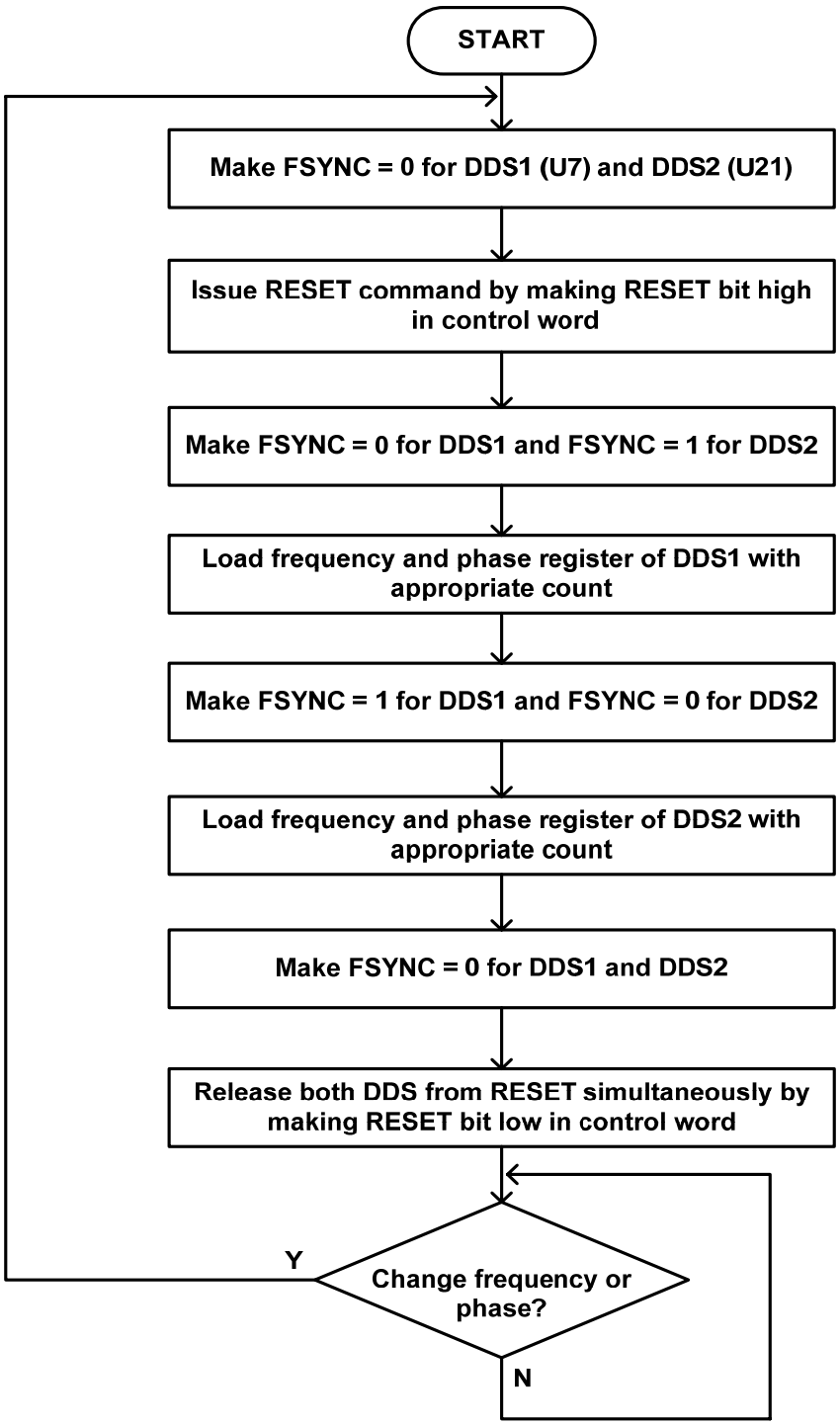

Figure 4.3 Flowchart showing programming of the two DDS chips for synchronized outputs.

the same excitation frequency of 100 kHz. The phase register of U21 is loaded with zero to get 0^{o} phase shift and that of U7 is loaded with the appropriate count to get the desired phase shift with respect to the output of U27. Both the DDS have to be synchronized by taking them out of reset simultaneously so that their output generation starts at the same instant and the

programmed phase relationship is maintained. For this the FSYNC pins of both DDS are driven low simultaneously and the appropriate control word is loaded through the SPI bus.

The AD9834 is a current output device and gives differential sinusoidal current outputs on pins 19 and 20 as shown in Figure 4.2. The output current amplitude is set by the resistor connected from pin 1 to ground according to the following equation [11],

$$I_{out} = 18\ \mathrm{Vref} / R \tag{4.3}$$

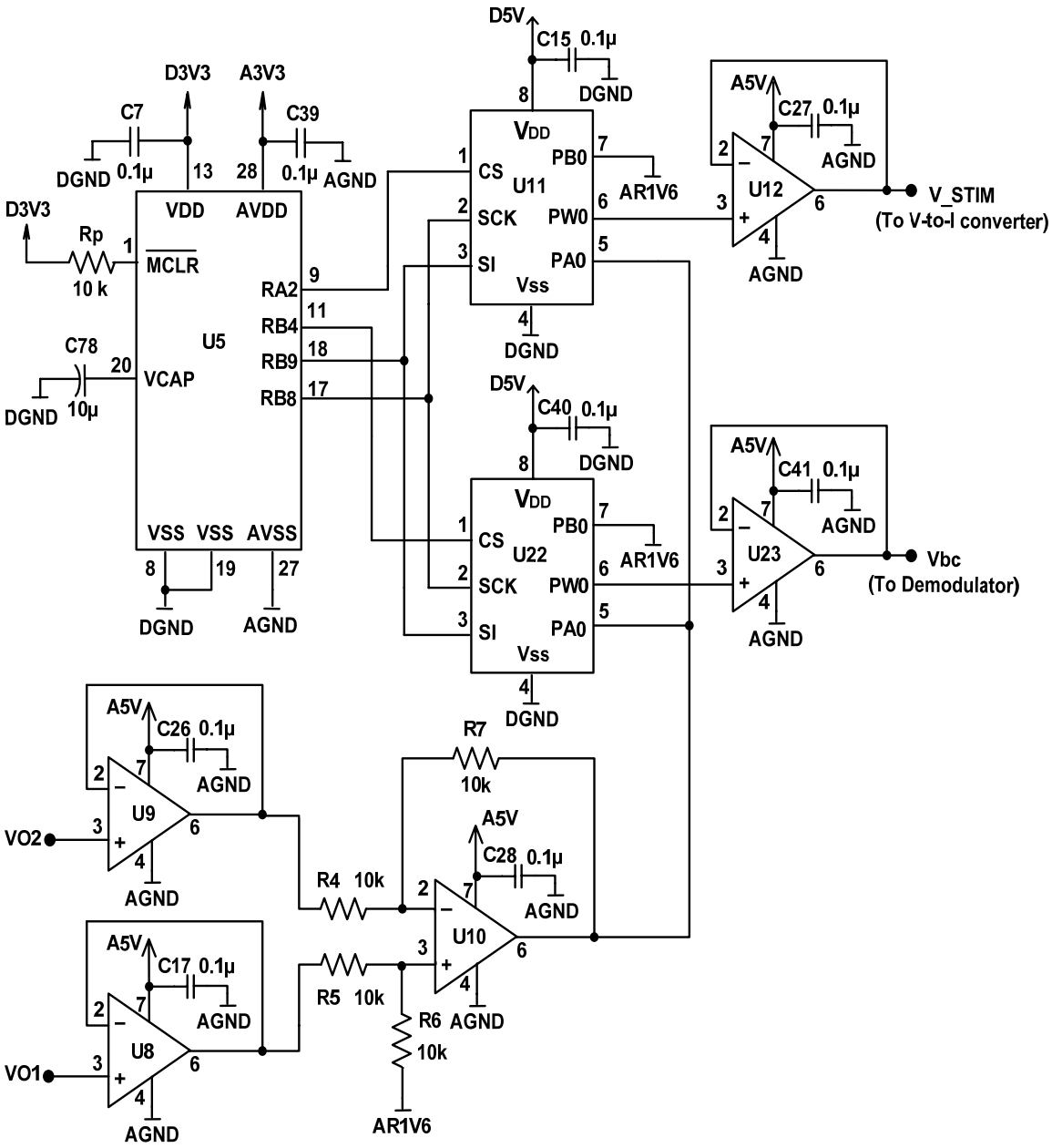

Figure 4.4 Waveform amplitude control using digital potentiometers. (U5: dsPIC33FJ128GP802, U11, U22:MCP4151-502, U8, U9, U12, U23: MCP6021)

where R is the resistance connected between pin 1 and ground, and V_{ref} is the internally generated constant reference output of 1.2 V on pin 2 [11]. The current output on pins 19 and 20 are converted to voltage by connecting a resistor between the pins and ground as shown in Figure 4.2. The resistor has to be selected such that the voltage developed across it does not exceed the voltage compliance limit of 0.8 V [11]. The square wave is generated on the sign-bit out (SBO) pin.

4.2.2 Waveform Amplitude Control

The sinusoidal signal generated by the waveform generator is given as input to the V-to-I converter and as a baseline correction signal to the demodulator. The output current of V-to-I converter is directly proportional to the amplitude of the input signal. Also the baseline shift in the demodulator is proportional to the amplitude of the baseline correction signal. In order to allow independent control of the output of the current source and the baseline correction in the demodulator output, two digital potentiometer ICs (MCP4151-502) have been used. This IC can operate in the supply range of 2.7 to 5.5 V and has a total resistance of 5 kΩ, with 256 steps and a wiper resistance of 75 Ω [34]. The wiper position can be controlled through SPI.

The amplitude control circuit is shown in Figure 4.4. The complementary outputs on the pins 19 and 20 of the DDS 1 marked as VO1 and VO2, are buffered by U8 and U9, and given to the differential amplifier formed using U10. Its output is given to the two digital potentiometer ICs, U11 and U22. The voltage at the wiper output of U11 is buffered by U12 and given as input to the V-to-I converter. The voltage at the wiper output of U22 is buffered by U23 and given as the baseline correction voltage to the demodulator. The wiper positions of both the potentiometers are controlled by the microcontroller through the same SPI bus that is used to configure the DDS chips. The chip select pins of U11 and U22 are connected to port pins RA2 and RB4 of the microcontroller, respectively.

4.2.3 Voltage-to-current Converter

The voltage waveform generated by the waveform generator is converted into current by using a voltage-to-current converter. This current is injected into the thorax through a pair of electrodes. The voltage-to-current converter has been realized using a modified Howland current source [10] as shown in Figure 4.5. All voltages are referred to the analog reference of 1.6 V marked as AR1V6. The output current is obtained as,

$$I = \frac{V_a - V_b}{R_{16}}$$

With $R_{12} = R_{13}$ and $R_{10} = R_{11}$, we get

$$V_x = \frac{V_{in} + V_b}{2} = \frac{V_a}{2}$$

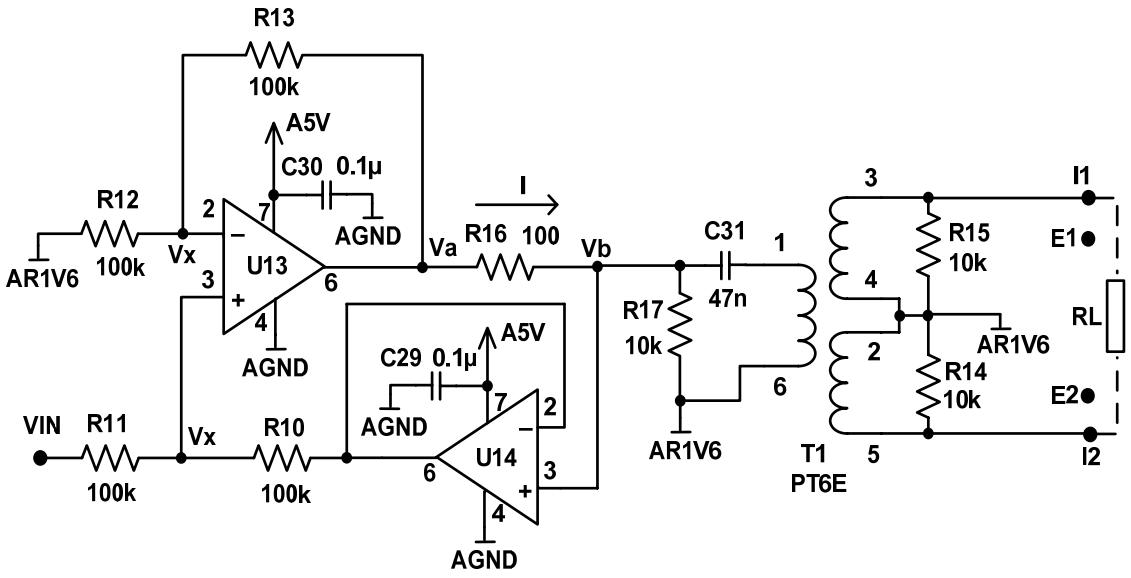

Figure 4.5 Voltage-to-current converter using modified Howland current source and transformer. (U13, U14: MCP6021, R12 = R13 and R10 = R11)

which results in, $V_a - V_b = V_{in}$. Hence the load current is given as,

$$I = \mathrm{V_{in}} / R_{16} \tag{4.4}$$

The output impedance depends on the matching of the resistance ratios R_{13}/R_{12} and R_{10}/R_{11} [35]. The op amp U14 in the feedback path makes the output impedance independent of $\mathrm{R_{16}}$. The op amps used in the current source are MCP 6021 from Microchip. This op amp can be operated with supply voltage in the range of 2.5 - 5.5 V and has rail-to-rail input and output [36]. It has a gain bandwidth product of 10 MHz and its output can source and sink current up to 30 mA. Hence it was considered to be suitable for a current source of up to 5 mA at 100 kHz. The op amps have been powered from a single supply of 5V and an analog reference of 1.6 V (marked as AR1V6) has been used to bias the signals within the supply range.

To reduce common mode pick-up and stray currents the current output is converted to complementary differential form using pulse transformer PT6E from OEP [37] having a turns ratio of 1:1+1. As shown in Figure 4.5, the terminals 2 and 4 of the two secondary windings have been shorted together and connected to the analog reference AR1V6 to create a center-tapped configuration. The signals at the terminals 3 and 5 are biased about the analog reference AR1V6 and are out of phase, hence creating a differential configuration. C31 provides ac coupling with an impedance of 33.86 Ω at 100 kHz.

4.3 Voltage Sensing Amplifier

The voltage developed across the thorax is sensed by the voltage sensing electrodes E1 and E2 and is then amplified by a voltage sensing amplifier. The instrumentation amplifier

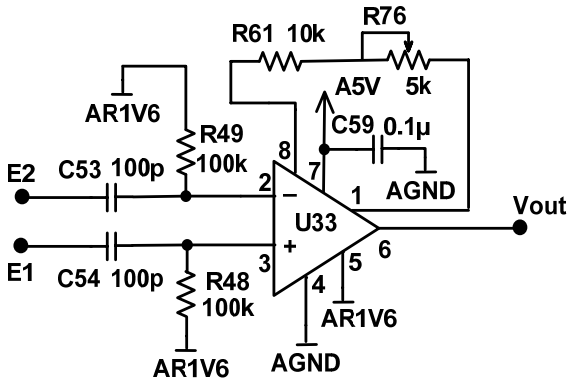

Figure 4.6 Voltage sensing amplifier using INA 155.

INA155 from Texas Instruments has been used as the voltage sensing amplifier as shown in Figure 4.6. The IC can be operated with supply voltage of 2.7 - 5.5 V and has rail-to-rail output swing. It has a gain bandwidth product of 5.5 MHz and a slew rate of 6.5 V/µs [38]. Hence it was considered suitable for operating frequency of 100 kHz. The instrumentation amplifier has a typical CMRR of 100 dB and the gain can be varied in the range 10 to 50 by varying the resistance connected between the pins 1 and 8 according to the equation [38],

$$G = 10 + \left(\frac{400\ \text{k}\Omega}{10\ \text{k}\Omega + R_G} \right) \tag{4.5}$$

where R_G is the external resistance connected between the pins 1 and 8.

The IC is powered by a single 5 V supply and the reference pin 5 is connected to the analog reference AR1V6 of 1.6 V for single supply operation. The two inputs are RC coupled to reject noise and other bio-electric signals. The resistor and capacitor values as given in the figure result in a cut-off frequency of 16 kHz. The resistances R48 and R49 also provide a path for the input bias currents which is crucial for the proper operation of the instrumentation amplifier. The chip's CMRR deteriorates with frequency and at 100 kHz it reduces to around 25 dB [38]. Also a mismatch between the values of C53 and C54 or between R48 and R49 will again adversely affect the CMRR.

4.4 Demodulator

The synchronous demodulation scheme described in Section 3.7 was implemented first using analog multiplexer CD4053 and subsequently using SPDT switches ADG734 as described in the following two subsections.

4.4.1 Demodulation Using Analog Multiplexer CD4053

The demodulation scheme was first tested using analog multiplexer CD4053 as shown in

Figure 4.7. It is a triple two-channel analog multiplexer having three separate digital control inputs A, B, and C [39]. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration. Since four such two-channel multiplexers are required for the entire demodulation scheme, two CD4053 ICs, namely IC6 and IC7 have been used. Two multiplexers, MUX A and MUX B, in each IC are used with the third being left open and has not been shown in the Figure 4.8 for clarity. The baseline correction signal V_{bc} is obtained from the input V_{in} by using the resistive divider formed by the resistance R6 and potentiometer R7. The potentiometer R7 is used for varying the correction signal amplitude. The input signal V_{in} and the baseline correction signal V_{bc} are

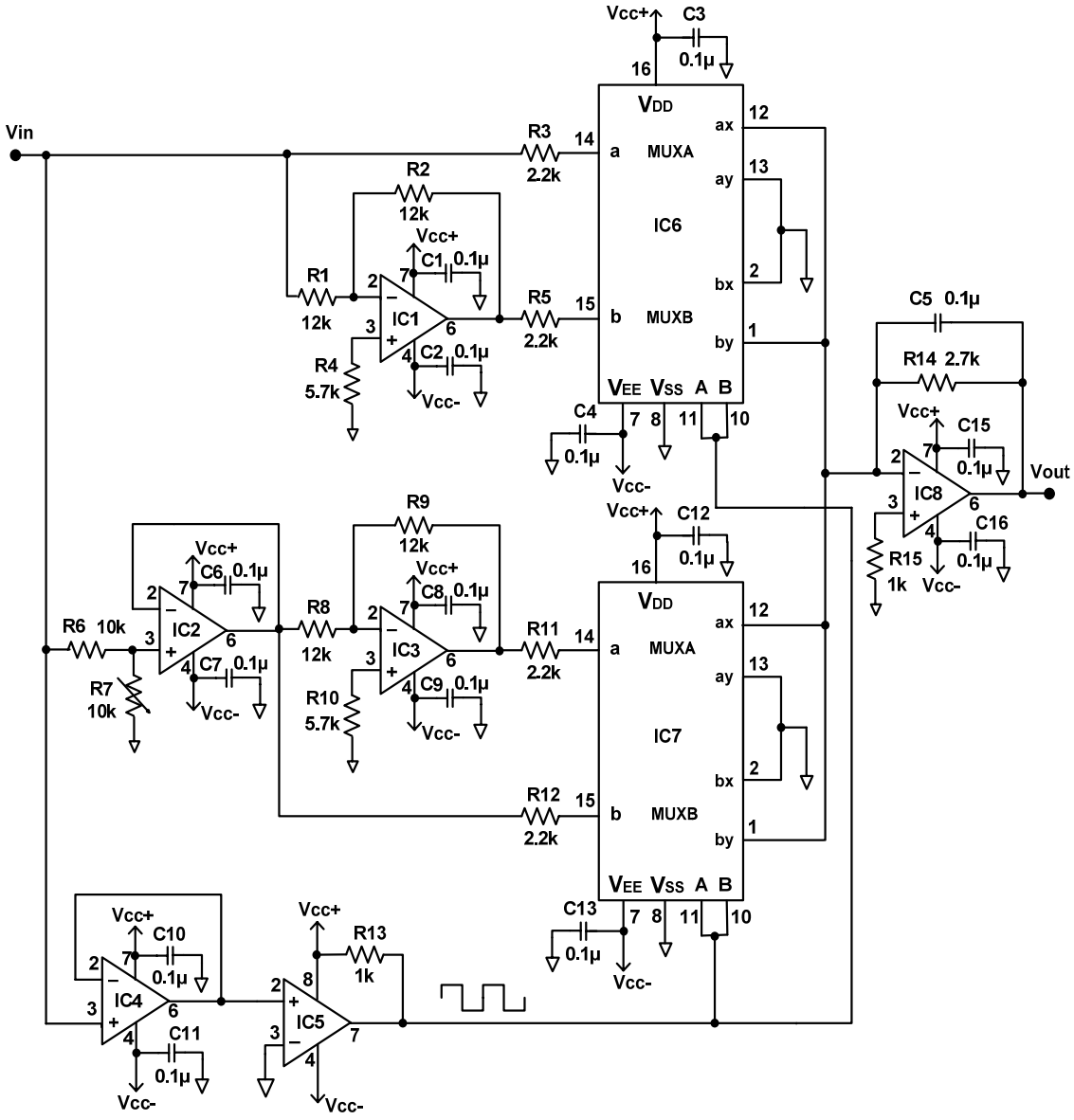

Figure 4.7 Demodulation using CD4053. (IC1-IC4, IC8: TL084, IC6, IC7: CD4053, IC5: LM311,Vcc+: +5V, Vcc-: -5V)

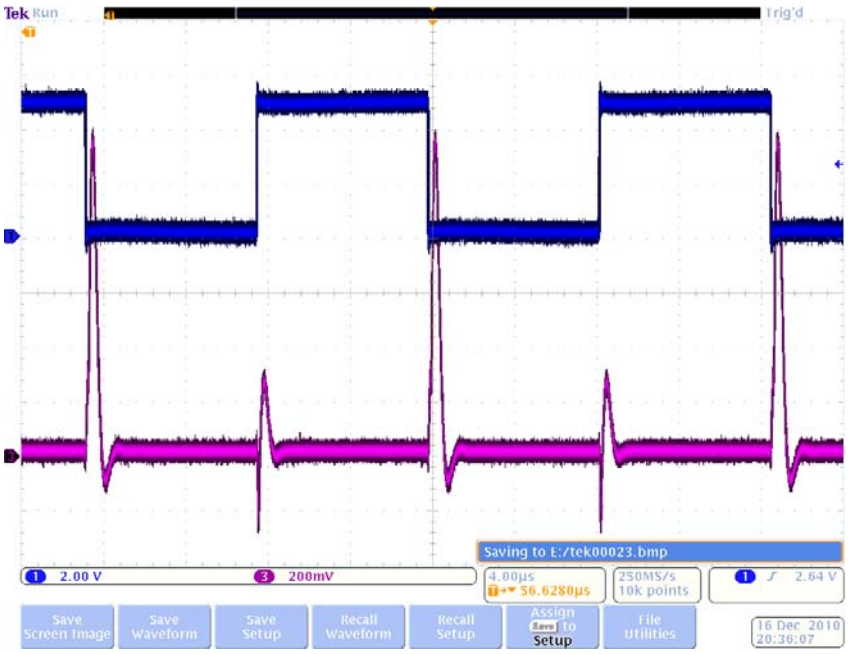

Figure 4.8 Spikes in the output due to clock-feedthrough.

inverted by the op amps IC1 and IC3 respectively before being given to the MUX B and MUX A of IC6 and IC7. For testing, the clock signal was generated from the input itself using the comparator IC LM311 (IC5). The same clock is given to the control inputs A and B of both IC6 and IC7. When the clock is low the MUX A and MUX B inputs ‘a’ and ‘b’ get connected to “ax” and “bx” respectively. Similarly they toggle to “ay” and “by” respectively when the clock is high. Since the signals at the inputs ‘a’ and ‘b’ are out of phase, the output is a full wave rectified signal. The full-wave rectified current outputs from IC6 and IC7 are low-pass filtered and converted into voltage by IC8 to get the demodulated output.

When the capacitor C5 was removed to observe the rectified signal without low-pass filtering, voltage spikes were observed in the output at the clock switching instants due to clock feed-through in the switches. This was further investigated by observing the output when the input and the baseline correction signal were made zero and only clock was given to the switches. The clock and the voltage spikes in the output for this configuration are shown in Figure 4.8. Hence the analog multiplexer CD4053 was found to have poor performance in terms of clock feed-through. As the internal analog switches connecting terminals ‘a’ to “ax” and ‘b’ to “by” receive inverted versions of the clock, the spikes due to clock feed-through should have cancelled at the output. Hence the presence of voltage spikes in the output indicated that there was a mismatch between the channels of the multiplexers because of the internal inversion of the clock. Hence it was decided to use switches that had better performance in terms of clock feed-through and channel to channel matching.

4.4.2 Demodulation Using Quad SPDT Switches ADG734

The ADG734 IC from Analog Devices consists of four independently selectable SPDT switches. Hence only a single IC is required in the demodulator. The IC can operate with a single supply in the range of 1.8 to 5.5 V or a dual supply of ± 2.5 V and has rail-to-rail input swing [40]. It has a 3-dB bandwidth of 160 MHz and switching time of 19 ns and hence is suitable for the operating frequency of 100 kHz. As shown in Figure 4.9, the four SPDT switches in U25 are connected in the same configuration as that of the CD4053 based demodulator. The clock input of all the four SPDT switches are shorted together and driven by the clock signal generated by the DDS in the waveform generator. The output of the voltage-sensing amplifier is given as input to the demodulator. The baseline correction signal is obtained from the waveform generator where its amplitude is controlled by a digital potentiometer under software control. The two inverting amplifiers for inverting the input and correction signal before giving them to switch 2 and 3 respectively are realized using U26 and U24. The current-to-voltage converter-cum-low-pass filter at the output is implemented using

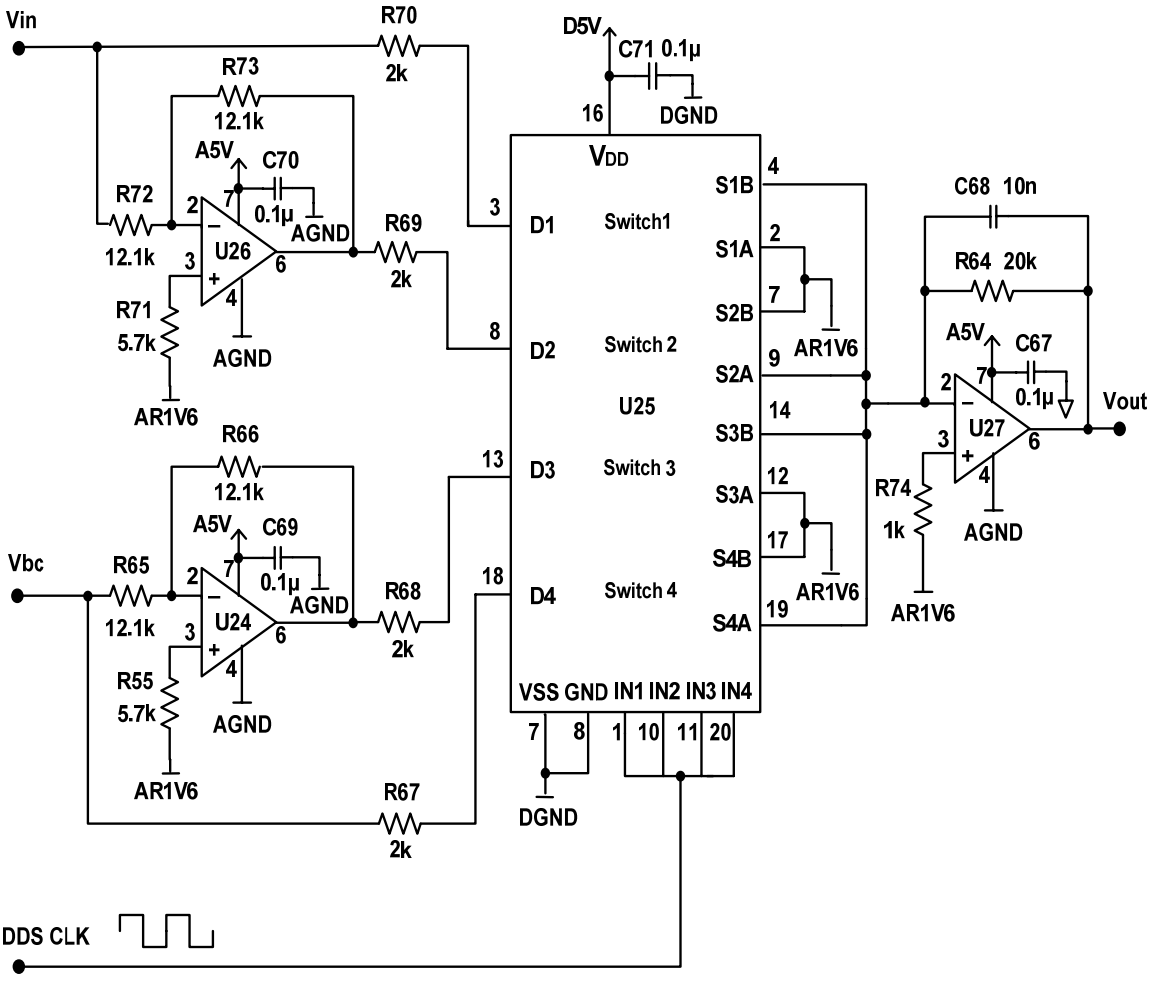

Figure 4.9 Demodulation using ADG734. (U24, U26, U27: MCP6021, U25: ADG734)

U27. Op amp MCP6021 has been used in these three places since it has a good high frequency response and rail-to-rail input and output swing. Since the whole circuit operates with a single supply of 5 V, an analog reference of 1.6 V (marked as AR1V6) has been used in the op amps and the switches. Since the switches have good high frequency performance and better channel-to-channel matching, no spikes are observed at the output.

The demodulated signal at the low-pass filter output is the impedance variation signal $z(t)$ and is made available as an analog output and is also given to the microcontroller where it is sampled by an on-chip ADC. The sampling rate and the sampling instant of the ADC is controlled by an on-chip timer in the microcontroller which is clocked by the same clock that is used for the demodulation. Hence the number of cycles after which the demodulated output is sampled and the synchronization of the sampling instant with peaks of carrier to reject the carrier ripple can be easily controlled in software.

4.4.3 Phase Correction

The clock signal generated by the DDS in the waveform generator directly reaches the demodulator. But the sinusoidal excitation signal travels through the current source, the electrode connecting cable, and the voltage-sensing amplifier before reaching the demodulator. Hence there may be some phase shift between the DDS output and the sensed voltage. This phase shift affects the average value of the demodulated output. The average value of the output will be maximum when the phase shift between the sensed voltage and the reference clock is zero and minimum when the phase shift is 90°. The phase shift can vary depending on the cables and subjects, and hence it has to be corrected for each recording.

As the phase and frequency of the signals generated by the waveform generator can be controlled in software by the microcontroller, the phase shift can be corrected by varying the phase of the DDS that generates the sinusoidal excitation with respect to the DDS generating the clock signal. The sinusoidal excitation can be advanced in phase with respect to the clock signal so that the sensed voltage and the clock are in-phase at the demodulator. To determine the optimum phase lead to be given to the sinusoidal excitation, a phase correction logic is implemented in software as shown in the flowchart in Figure 4.10. Starting from 0°, the phase of the sinusoidal excitation signal is incremented in steps of 5° up to 360°. After each 5° step increment, ten samples of the demodulator output are taken by the ADC in the microcontroller at intervals of 100 cycles of the excitation (1ms for 100 kHz). These ten samples are then averaged and stored in an array. After the whole range of phase shift from 0° to 360° is scanned, the maximum value in the array is located. The phase shift corresponding to this output is taken as the optimum phase shift. The total time required for the phase correction depends on the phase increment step size, number of samples taken after each step increment in phase, and the ADC sampling rate all of which can be controlled in software.

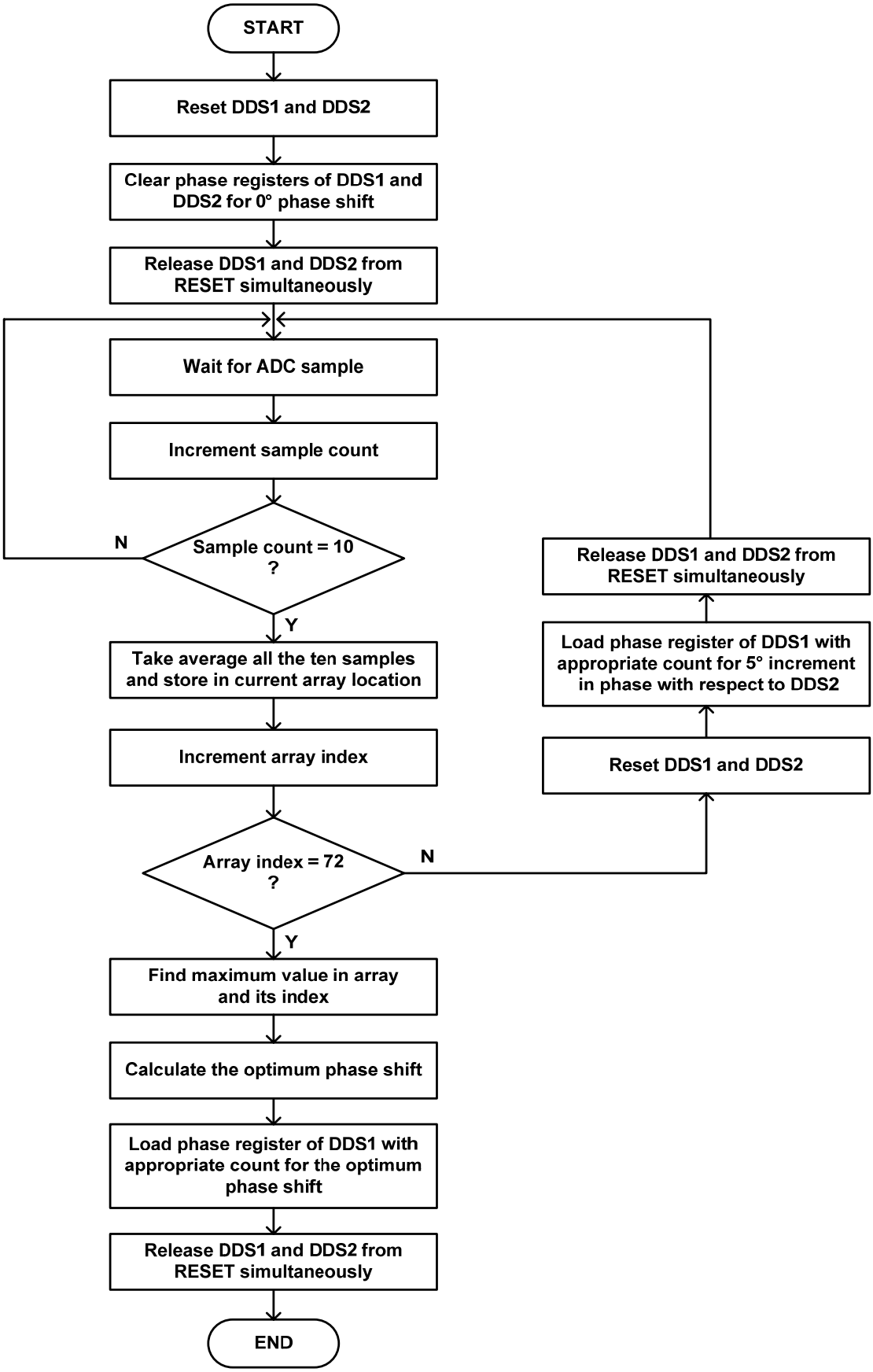

Figure 4.10 Flowchart of the phase correction logic.

4.4.4 Baseline Restoration

The baseline restoration circuits described in Section 3.5 require separate hardware for tracking and correcting the drift signal. In our demodulation scheme, the baseline restoration can be implemented within the demodulator itself and no separate hardware is required. Since the amplitude of the baseline correction signal for the demodulator is controlled by a digital potentiometer in the waveform generator, the demodulator output can be used in a feedback loop to control the correction signal amplitude and hence keep itself within the predefined upper and lower thresholds. Once the demodulator output is sampled by the ADC in the microcontroller, it is compared with the predefined threshold limits. If the output is greater than the upper threshold, the microcontroller updates the wiper of the digital potentiometer to increase the baseline correction signal amplitude and hence decreases the demodulator output. Similarly if the demodulator output crosses the lower threshold, the correction signal amplitude is decreased to bring the output within the threshold range.

4.4.5 Basal Impedance

The demodulated signal consists of a constant DC voltage which represents the basal impedance of the thorax and a time varying signal superimposed on the DC voltage representing the variations in the thoracic impedance with each cardiac cycle. As the baseline correction signal is subtracted from the input signal in the demodulator, the DC voltage in the output does not represent the actual basal impedance. But, since the demodulator output is sampled by the ADC in the microcontroller and also the wiper setting of the digital potentiometer controlling the baseline restoration signal amplitude is known, the actual basal impedance can be calculated in software.

4.5 ECG Extractor

The ECG extractor is used to extract the ECG from the signal sensed by the voltage-sensing electrodes. The R peaks of the ECG waveform are used as a reference in impedance cardiography. The ECG amplifier was adapted from earlier designs [9], [10] as shown in Figure 4.11. It is based on INA155 (U35), the same IC as used in the ICG section. The low-pass filter, with 3-dB cutoff frequency of 40 Hz, at the input of the instrumentation amplifier rejects the high frequency carrier. Resistances R3 and R4 provide a path for the bias currents of the instrumentation amplifier (U35). In this circuit, matching of C50 and C51, R38 and R41, and R39 and R40 is important for high CMRR. The instrumentation amplifier amplifies the low frequency signals and rejects any common-mode pick up. The output of the instrumentation amplifier is then filtered by the cascade of the low-pass and high-pass filter stages having cut-off frequency of 20 Hz and 1.6 Hz respectively to get the ECG with enhanced R peaks. The ECG signal is made available as an analog output and is also given to the microcontroller where it is sampled by its ADC. The ECG obtained is used only as

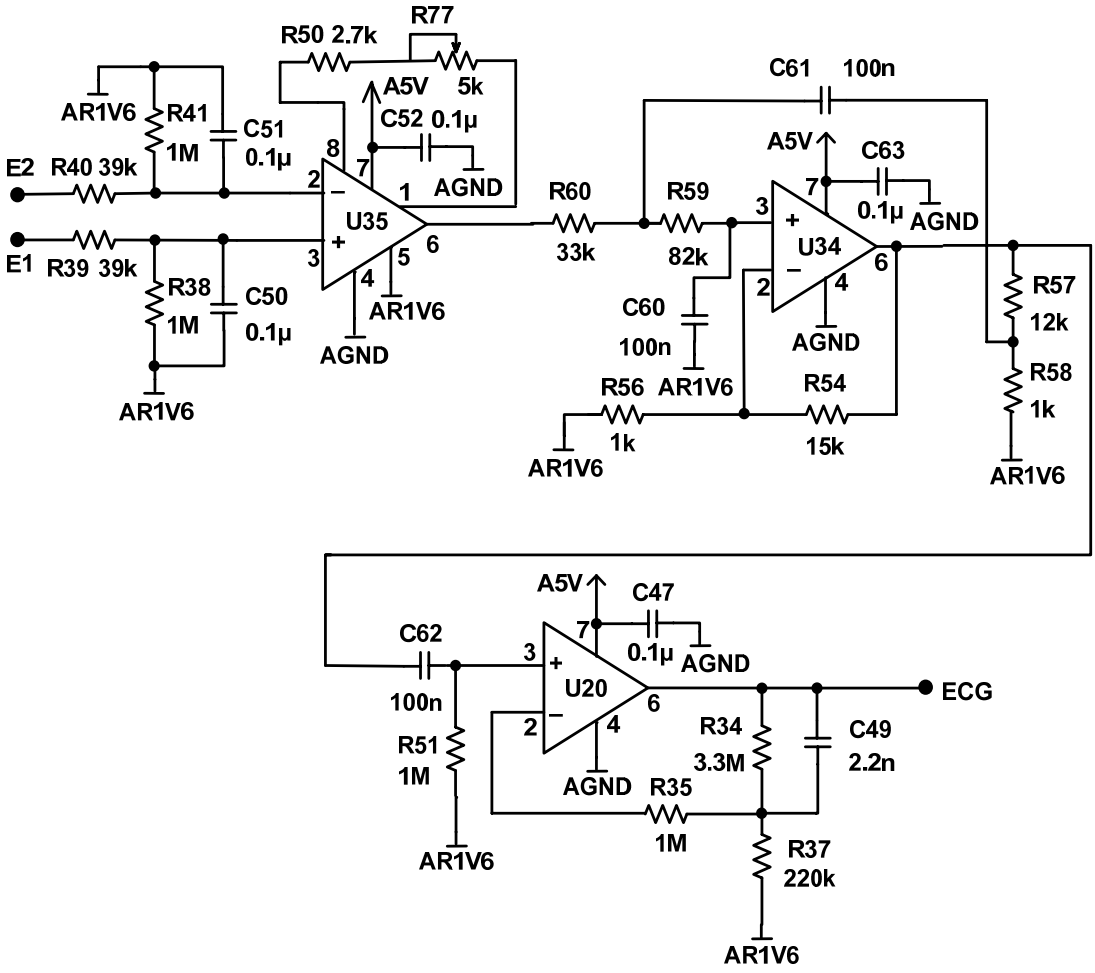

Figure 4.11 ECG extractor. (U35: INA155, U34, U20: MCP6021)

reference and is not suitable for physiological assessment.

4.6 Differentiator

The demodulator output represents the impedance variation signal $z(t)$. The differentiated version of this signal is known as the ICG (Impedance cardiogram) signal. As shown in Figure 4.12, a differentiator circuit is used for this purpose as used in the earlier design [9]. The ICG signal is made available as an analog output and is also given to the microcontroller where it is sampled by the on-chip ADC and can be stored in memory or transferred to an external interface. It may be noted that this output may be dropped in favour of a digital differentiator.

4.7 Contact Impedance Indicator

When the contact between the electrodes and the skin is not proper the impedance becomes very large. Hence the demodulator output will tend to saturate. A contact impedance indicator

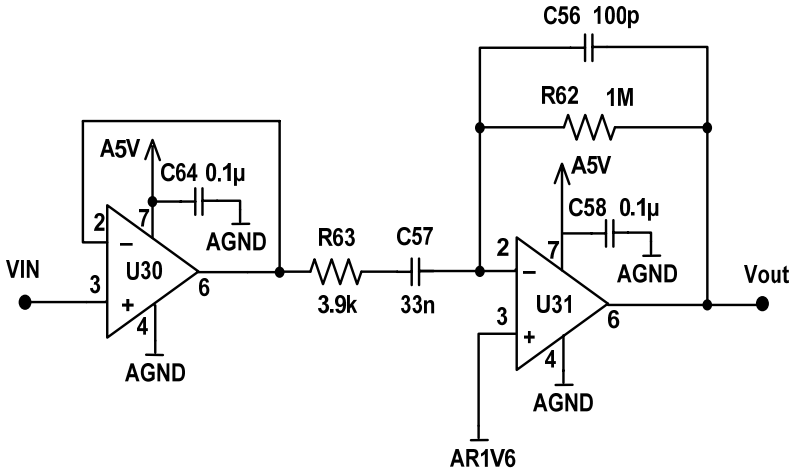

Figure 4.12 Differentiator. (U30, U31: MCP6021)

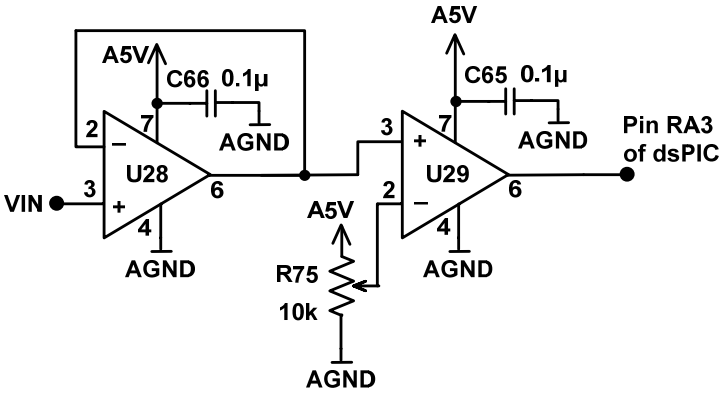

Figure 4.13 Contact impedance indicator.

is used [10] to indicate lack of a proper contact between the electrodes and skin as shown in Figure 4.13. The comparator is used to compare the output of the demodulator with a threshold voltage corresponding to normal value of the impedance. The output of the comparator is connected to a port pin of the microcontroller. Hence whenever the contacts become loose the port pin will be toggled to “low” state and the microcontroller will be notified of the loose contacts. The microcontroller can then take an appropriate action such as displaying on an LCD or glowing an LED to notify the user. The threshold level can be varied by using the potentiometer R1. This block is really not needed as this function can be performed by the ADC input of the microcontroller.

4.8 Microcontroller

The microcontroller used in the project is dsPIC33FJ128GP802 from Microchip. It can operate with power supply in the range of 3.0 – 3.6 V and has separate analog and digital supplies. It supports a maximum system clock of 80 MHz. The instruction clock is half of the

system clock and hence it supports operation up to 40 MIPS [30]. The system clock can be generated internally using an RC-oscillator and PLL thus avoiding the use of an external crystal.

The schematic showing the connection of the microcontroller U5 is shown in Figure 4.14. It has two on-chip 4-wire SPI modules which support both 8-bit and 16-bit data formats and support clock frequencies up to 10 MHz. One of the modules has been used to control the two DDS and the two digital potentiometers, in the waveform generator, via the SPI bus. The microcontroller also has an on-chip ADC which can support 10-bit or 12-bit conversion at a maximum frequency of 1.1 MHz and 500 kHz respectively. The ADC has 10 channels and can support four-channel simultaneous sampling in 10-bit conversion mode. Four channels of the ADC have been used to sample the demodulator output z(t), ICG, ECG, and battery voltage. The battery voltage input comes from the power supply and is described later in the power supply section. The microcontroller also has two on-chip UART modules which can be used for implementing RS232 communication. One of the modules has been used to implement an isolated RS232 interface as explained in the next section.

4.9 Isolated RS232 Interface

For communicating with any external device or PC, a RS232 interface has been provided in the instrument. Since medical devices have to be isolated to prevent possibility of electrical

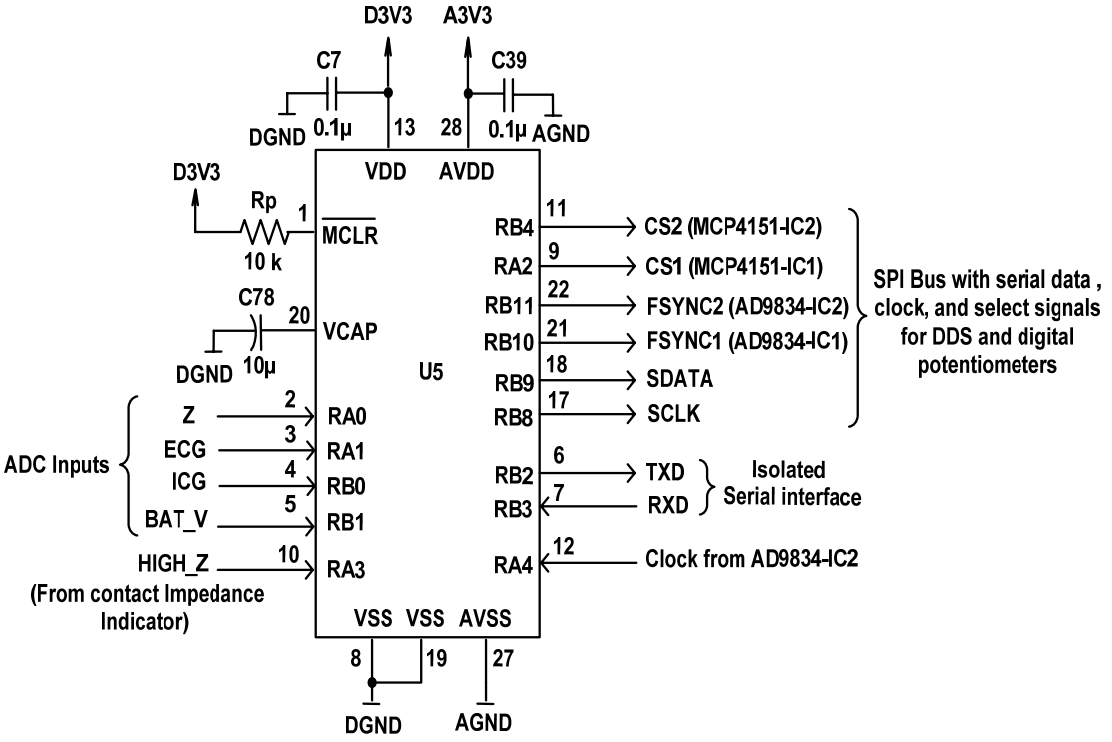

Figure 4.14 Microcontroller circuit.

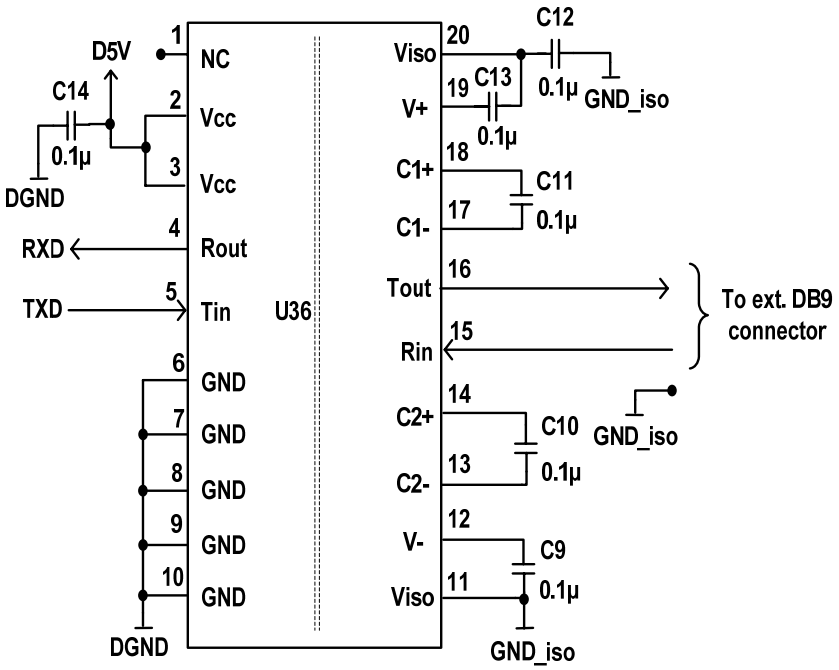

Figure 4.15 Isolated RS232 interface using ADM3251E.

shock to the patient, the RS232 interface has been isolated using the IC ADM3251E as shown in the Figure 4.15. ADM3251E is a high speed, 2.5 kV fully isolated, single-channel RS232 transceiver from Analog Devices [41]. It supports data rate up to 460 kbps and operates from a single 5V supply. Power to the isolated side is provided using an internal, isolated, integrated dc-to-dc converter [41]. Thus the circuit does not need power connection on the PC side. It has an integrated charge-pump voltage converter which uses four external 0.1 µF capacitors C9, C10, C11, and C13, as shown in Figure 4.15, for generating the RS232 levels.

4.10 Power Supply

The power supply circuit is shown in Figure 4.16. The circuit is powered by 9V supply. The regulator ICs, U2 and U3 supply power to the digital sections of the circuit and U1 and U4 supply the analog sections. U1 and U2 are LM7805 regulators which generate a regulated output of 5V. U3 and U4 are LM1117 regulators and generate an output of 3.3V from the 5V output of U2 and U1 respectively. The 5V and 3.3V analog supply voltages are labeled as A5V and A3V3 respectively. Similarly the digital 5 V and 3.3 V supply voltages are labeled as D5V and D3V3. The op amp U18 has been used to generate a reference voltage of 1.6 V, labeled as AR1V6, from the analog 3.3V supply. This reference voltage has been used as an analog reference for all the op amps since they operate with a single supply of 5 V. The reference was selected as 1.6 V since the ADC in the microcontroller is powered by 3.3 V. Hence one can have an equal swing of 1.6 V on either side of the reference. The resistive

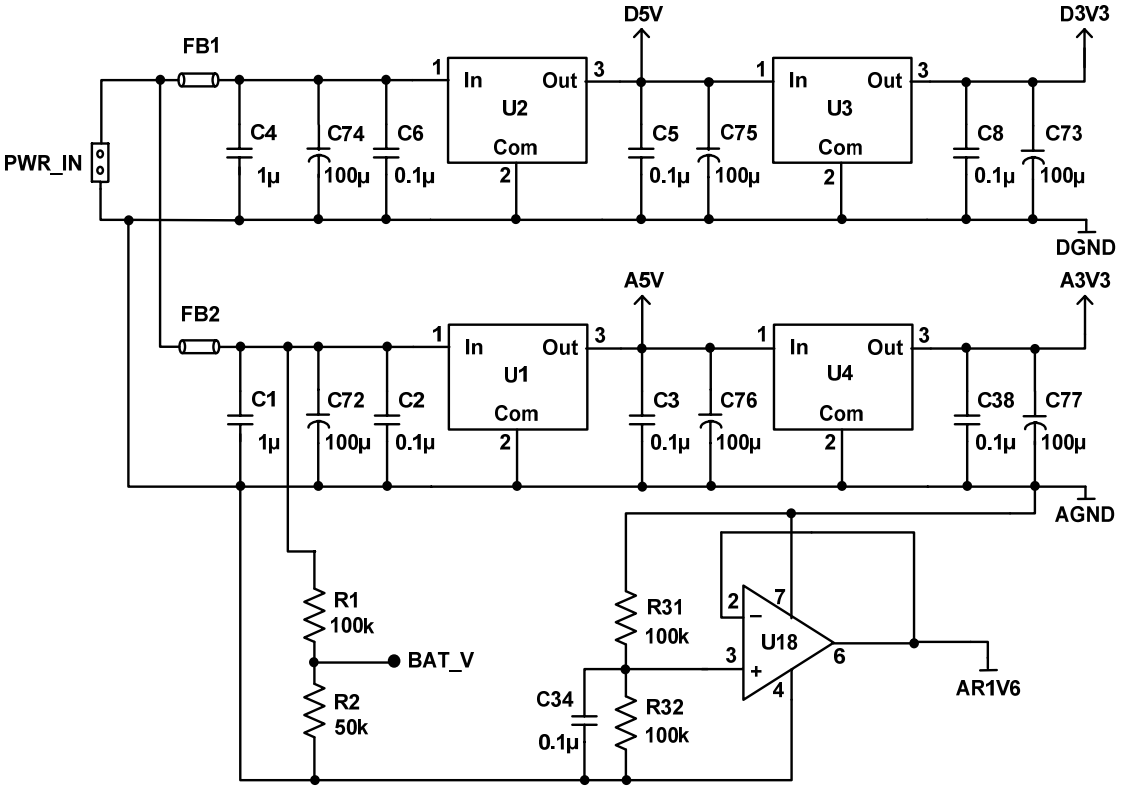

Figure 4.16 Power supply circuit.

divider formed by the resistors R1 and R2 divides the input supply by a factor of three to bring it within the ADC input range. This voltage is then given to an ADC input in the microcontroller for monitoring the battery voltage.

4.11 PCB Design and System Assembly

A two-layer PCB with PTH has been designed for the circuit. Most of the components used are in SMD package and they have been mounted on both the layers to reduce the number of track crossovers and the overall size of the board. The final size of the board is 144 mm x 94 mm. Wherever needed, the top and bottom side tracks have been connected by PTH having 0.8 mm diameter. Since the PCB contains analog as well as digital blocks, separate analog and digital power and ground planes have been used to avoid noise problems. The analog ground and digital ground are routed separately throughout the board and are shorted at the input power supply. The power supply pins of all the ICs have been decoupled using 0.1 µF capacitors. Digital 5 V and analog 5 V have been distributed as separate planes on the top side of the board. Similarly, digital and analog ground planes have been provided on the bottom side of the PCB. Shortest overall connection path have been chosen for pin-to-pin connections. The minimum signal track width used is 0.25 mm and the width of the power line tracks is 1.27 mm. A minimum clearance of 0.33 mm has been used between two signal

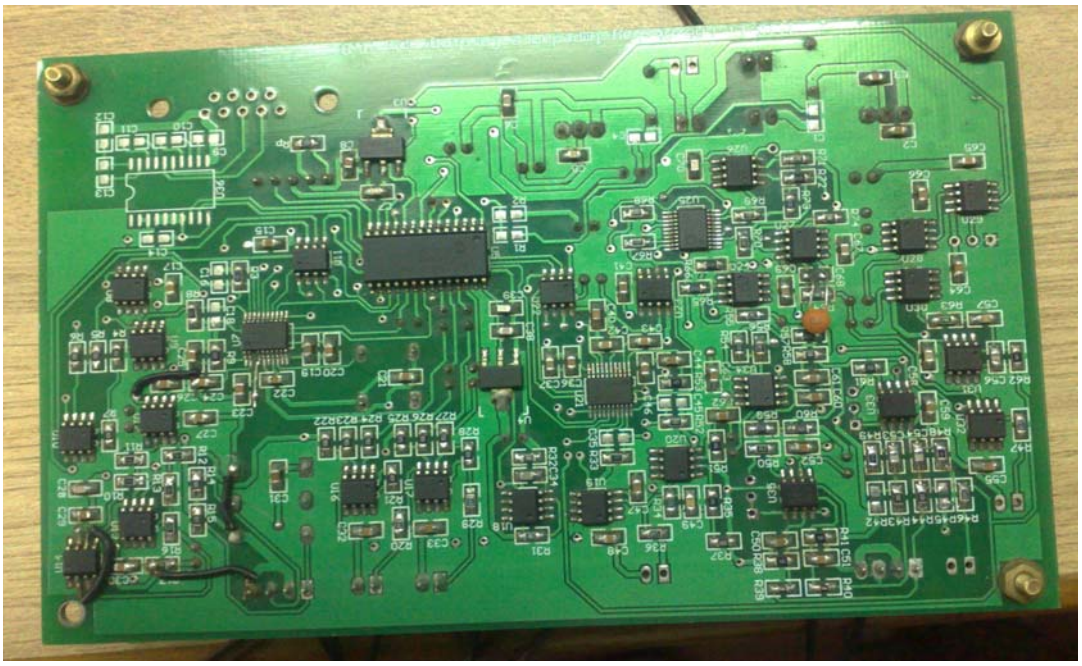

Figure 4.17 Bottom view of the assembled PCB.

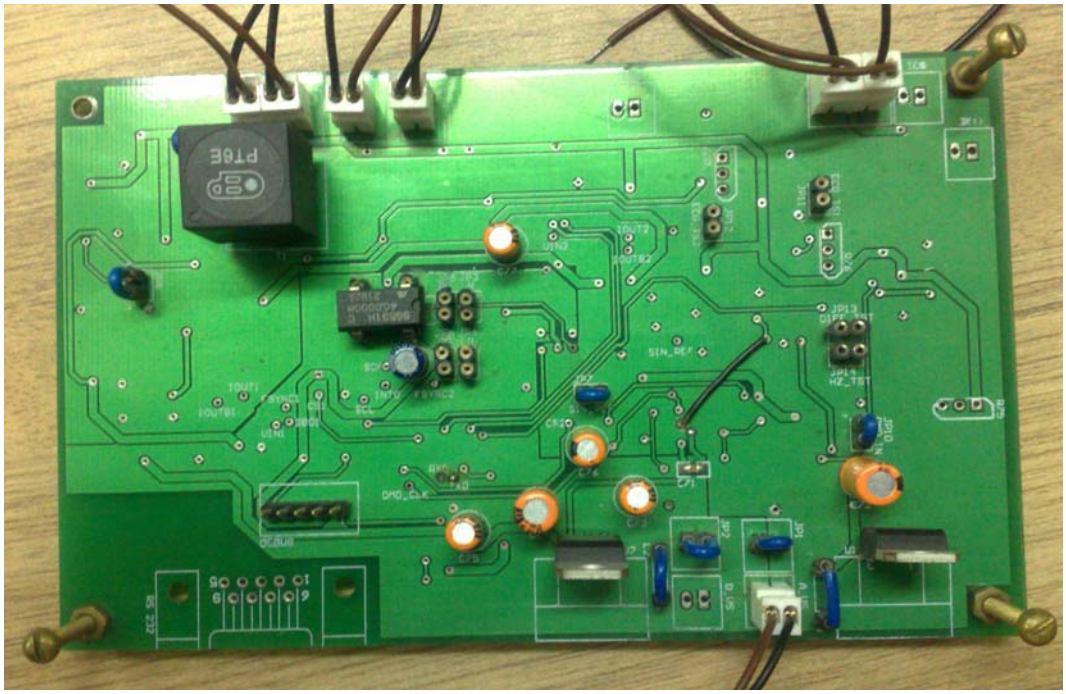

Figure 4.18 Top view of the assembled PCB.

tracks and between a signal track and polygon plane. A 45° corner style has been used for routing corners. The different hardware blocks of the instrument have been separated using jumpers so that they can be tested individually. The circuit schematic and the PCB layouts (top layer, top overlay, bottom layer, and bottom overlay) are given in Appendix A and B.

Before assembling the components on the PCB, a check on all the tracks was carried

out to ensure continuity and also to verify that there were no shorts between any neighboring track pairs. All components were soldered manually while taking special care not to exceed maximum lead temperature ratings for SMD packages. After assembling the components, the PCB was again thoroughly examined to ensure there were no shorts between IC pins due to formation of solder bridges and again a continuity check was performed to avoid the possibility of dry solder. The different hardware blocks were then tested separately to ensure their proper operation. A female DB9 connector has been provided for communicating with any external device or PC and 6-pin connector has been used for connecting Microchip's PICkit^{TM}3 debugger for programming and debugging the microcontroller. The two sides of the assembled PCB are shown in Figure 4.17 and 4.18.

CHAPTER 5

TEST RESULTS

5.1 Demodulator Output

The capacitor C68 in the low-pass filter stage of the demodulator was removed to observe the full-wave rectified signal. The excitation current amplitude and frequency were set to be 5 mA (p-p) and 100 kHz respectively. A 30 Ω resistance was connected as the load impedance across the current-injecting terminals (I1 and I2). The voltage developed across it was sensed using the voltage-sensing terminals (E1 and E2). A gain of 10 was used in the voltage-sensing amplifier. The analog reference AR1V6 was connected as the baseline correction signal (V_{bc}) A CRO capture of the input, rectified output, and the reference clock of the demodulator are shown in Figure 5.1. No clock feed-through was observed at the output but there was a phase shift between the input and the reference clock, indicating a delay due to the pulse transformer and the voltage-sensing amplifier. Hence the rectified output was distorted since the synchronous switching did not occur at the exact zero crossings.

5.2 Phase Correction

The phase correction algorithm was implemented in the microcontroller to compensate the phase shift between the demodulator input and its reference clock. The input, rectified output, and the reference clock of the demodulator after applying the phase correction logic are shown in Figure 5.2. As can be observed from Figure 5.2, once the phase shift between the input and the clock is corrected, a proper rectified signal is obtained at the output.

5.3 Sampling at the Peaks

To reject the carrier ripple remaining in the output after low-pass filtering, the output was sampled by the ADC in the microcontroller with its sampling instant synchronized with the peaks of the carrier signal. Timer1 in the microcontroller was clocked by the reference clock of the demodulator and was configured to generate an interrupt after 100 clock cycles (1 ms for 100 kHz clock frequency). This interrupt was used to start Timer2 to generate a delay of 2.5 μs (1/4th of the clock period). The Timer2 rollover interrupt was used to start the ADC sampling. Pin RB7 of the microcontroller was driven high while the ADC was sampling to observe the synchronization of the sampling instant with the peak of the carrier signal. The carrier input, rectified output, and the output pulse on pin RB7 are shown in Figure 5.3. As

can be observed from the figure, the sampling instant is synchronized with the peak of the carrier.

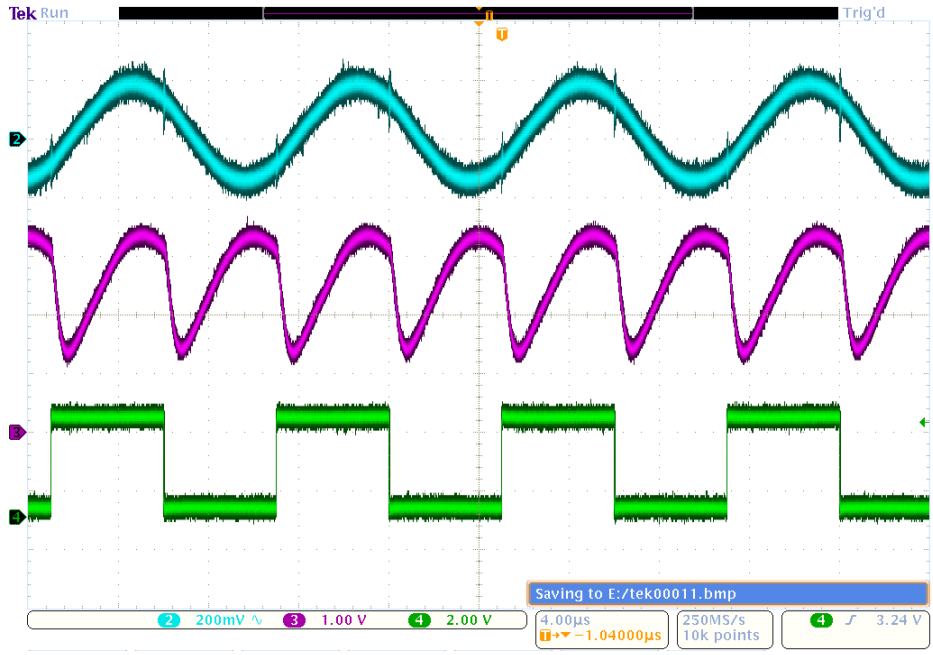

Figure 5.1 Demodulator input (CH2), rectified output (CH3), and reference clock (CH4) waveforms.

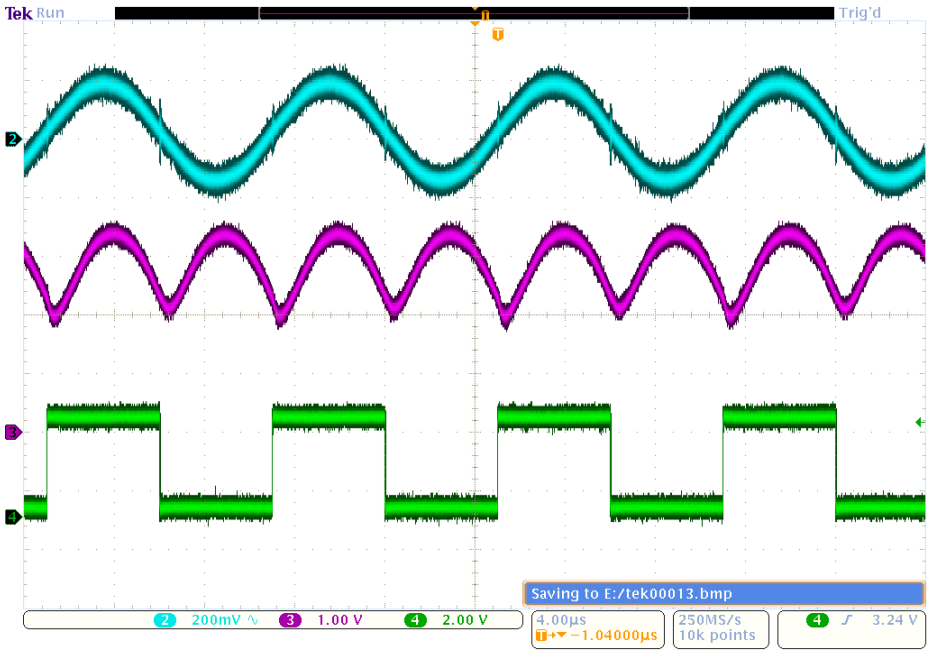

Figure 5.2 Demodulator input (CH2), rectified output (CH3), and reference clock (CH4) waveforms after phase correction.

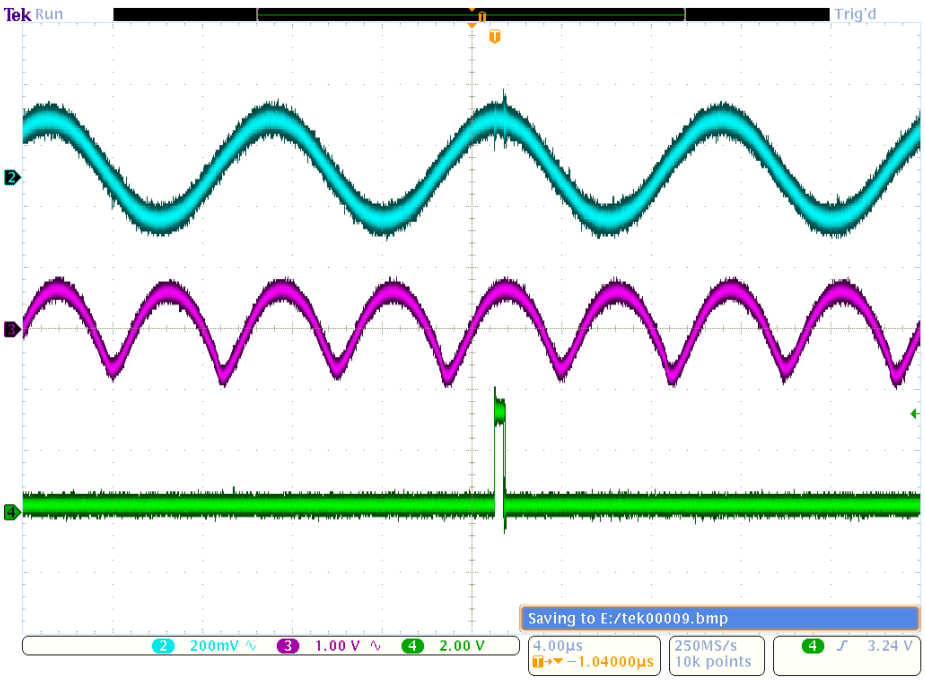

Figure 5.3 Waveforms showing synchronization of ADC sampling pulse (CH4) with demodulator input (CH2) and rectified output (CH3).

Table 5.1 Demodulator output voltages for equal increments in test resistance.

Resistance (Ω)	Demodulator output voltage (V)
10	2.00
20	2.40
30	2.75
40	3.00
50	3.44
60	3.78
70	4.00
80	4.00

5.4 Linearity

To test the linearity of the hardware, the demodulator output was measured for different values of resistances connected as the test impedance. The excitation signal frequency was kept at 100 kHz. The current-injecting terminals (I1 and I2) were connected across the resistance and the voltage developed across it was sensed using the voltage-sensing terminals (E1 and E2). The injection current amplitude was set as 5 mA (p-p). The capacitor C68 was

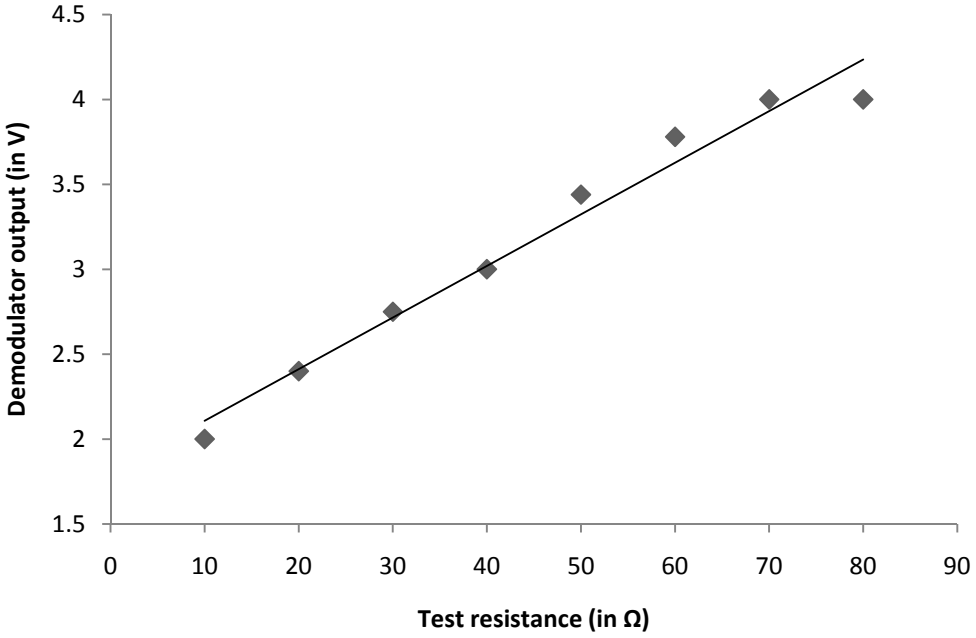

Figure 5.4 Plot of demodulator output voltage versus test resistance.

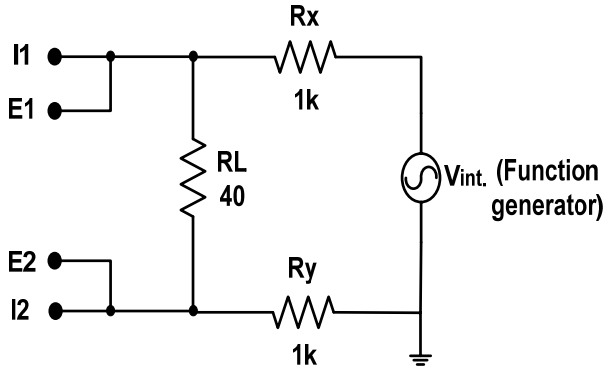

Figure 5.5 Setup for testing interference rejection.

connected to get the filtered demodulated output. The baseline correction signal (V_{bc}) input of the demodulator was kept at analog reference. The test resistance was increased in steps of 10 ohms and the corresponding increase in the demodulated output voltage was observed as shown in Table 5.1. The plot of demodulator output voltage versus test resistance is shown in Figure 5.4. As evident from the plot, the demodulator shows a good linearity over the tested range of resistances.

Table 5.2 Demodulator output at different interference frequencies.

Interference Freq. (kHz)	Demod. output ac (mVp-p)	Time period demod. output (ms)
0 - 98	-	-
99	320	1
99.5	400	2
99.6	440	2.5
99.7	460	3.4
99.8	470	5
99.9	470	10
100	470	600
100.1	500	10
100.2	480	5
100.3	460	3.4
100.4	440	2.5
100.5	400	2
101	320	1
102 – 298	-	-
299	140	1
299.5	170	2
299.6	180	2.5
299.7	180	3.4
299.8	200	5
299.9	200	10
300	200	210
300.1	200	10
300.2	200	5
300.3	180	3.4
300.4	170	2.5
300.5	170	2
301	140	1
302-499	-	-
500	50	120
600 - 1000	-	-

5.5 Interference Rejection

Interference rejection by the demodulator was tested by injecting interfering current at different frequencies for fixed test resistance of 40 Ω, as shown in Figure 5.5. The excitation current amplitude and frequency were set as 5 mA (p-p) and 100 kHz respectively. The interference voltage source amplitude was kept at 1 V (p-p) and its frequency was varied from 1 Hz – 1 MHz. The baseline correction signal (V_{bc}) input of the demodulator was connected to the analog reference. When there was no interference, the demodulator output was a constant DC voltage. There was no effect on the demodulator output voltage as the interference signal frequency was varied from 1 Hz – 1 MHz except at 100 kHz and its odd multiples. The peak-to-peak amplitude and time period of the variations in the demodulated output for different frequencies are shown in Table 5.2. A plot of peak-to-peak variation in the output vs. frequency is shown in Figure 5.6. With the interference frequency close to 100 kHz, a sinusoidal signal superimposed on the constant DC output of demodulator was

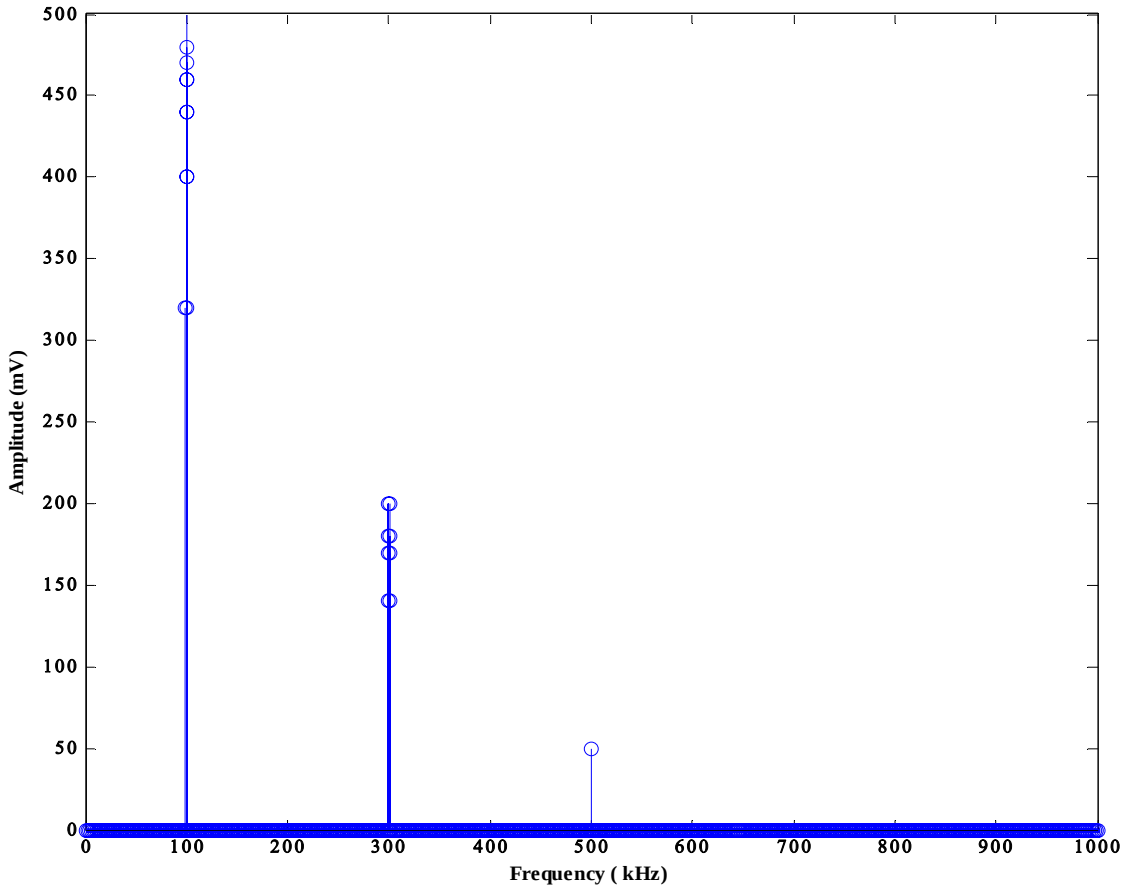

Figure 5.6 Plot of peak-to-peak variation in output vs. frequency.

observed with its amplitude increasing and frequency decreasing as the interference frequency came closer to 100 kHz. Similar behaviour was observed at 300 kHz except that the relative amplitudes were much lower. At higher odd multiples of 100 kHz the effect was negligible.

5.6 Validation of hardware using impedance simulator

The hardware was tested using an impedance simulator developed by Mandloi [42]. The excitation current amplitude and frequency were set to be 5 mA (p-p) and 100 kHz respectively. The current-injecting (I1 and I2) and voltage-sensing (E1 and E2) terminals of the hardware were connected to the terminals E1 and E2 of the simulator. A gain of 10 was used in the voltage-sensing amplifier. The capacitor C68 and the resistor R64 in the low-pass filter stage of the demodulator were selected as 270 pF and 1MΩ respectively which resulted in a 3-dB cut-off frequency of 589.5 Hz and a gain of 500. A square wave variation was selected in the simulator. The demodulator output waveforms are shown in Figure 5.7 – Figure 5.10 for the simulator settings given in Table 5.3. The sensitivity of the hardware was observed to be around 840 mV/Ω.

Table 5.3 Settings of the thorax simulator for the outputs shown in Figure 5.7 –Figure 5.10

Figure	R (Ω)	r (Ω)	F (Hz)	Impedance variation (%)
5.7	82	14	10	2
5.8	82	14	30	2
5.9	150	12	10	0.6
5.10	150	12	30	0.6

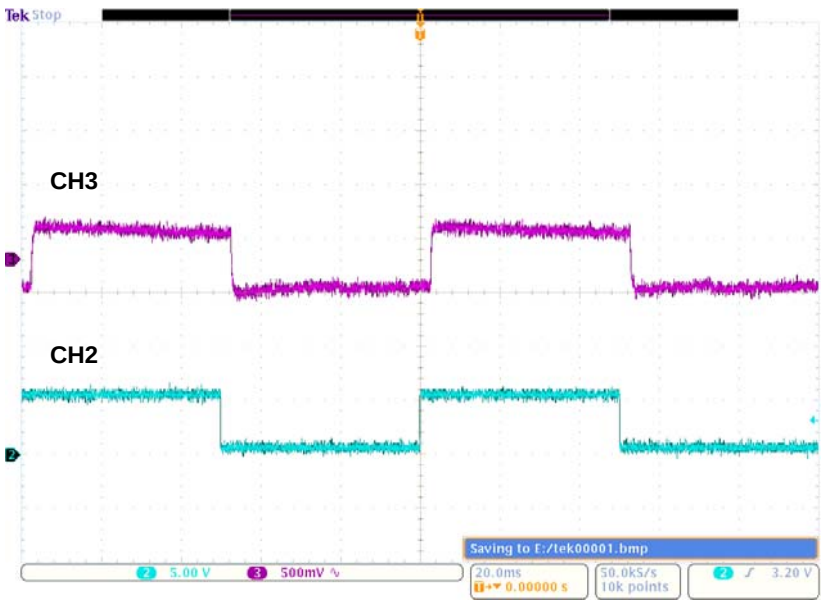

Figure 5.7 CH3: Demodulator output waveform for F = 10 Hz and impedance variation = 2%. CH2: Sync. test output from thorax simulator.

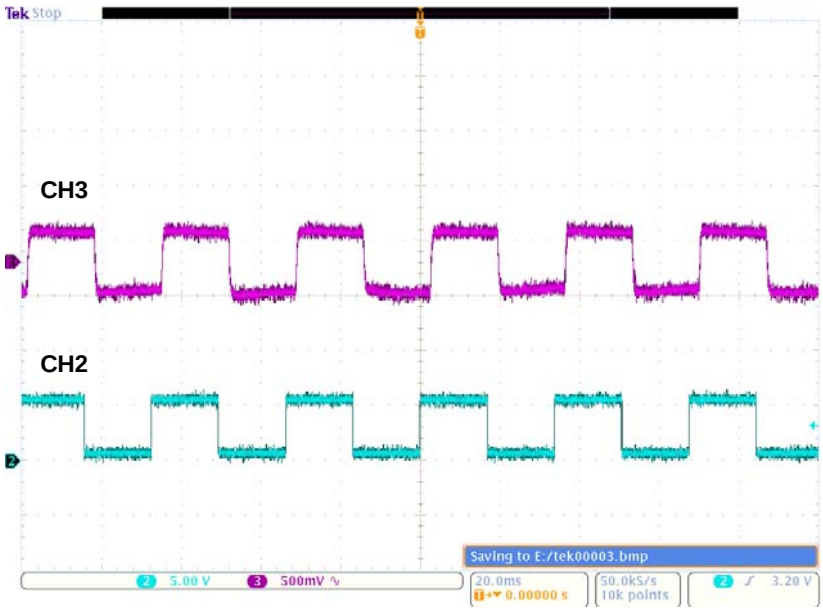

Figure 5.8 CH3: Demodulator output waveform for F = 30 Hz and impedance variation = 2%. CH2: Sync. test output from thorax simulator.

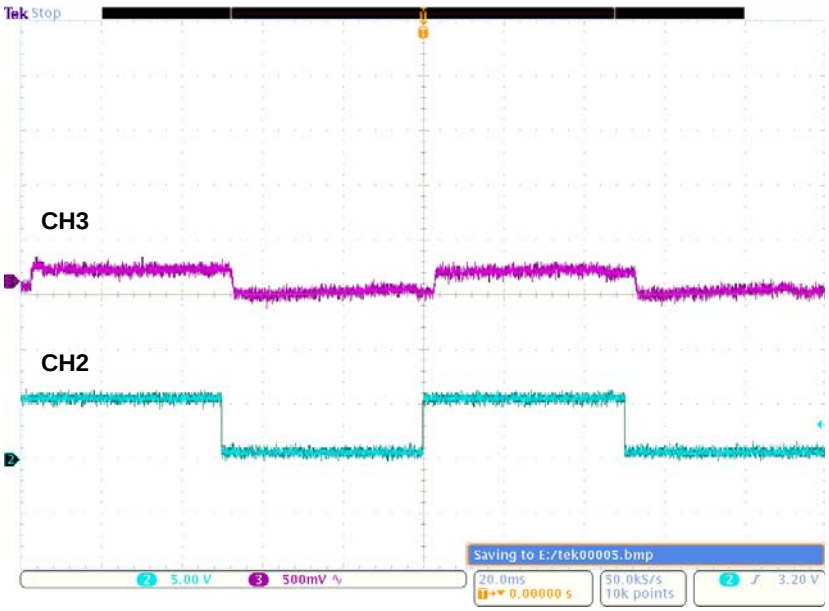

Figure 5.9 CH3: Demodulator output waveform for F = 10 Hz and impedance variation = 0.6%. CH2: Sync. test output from thorax simulator.

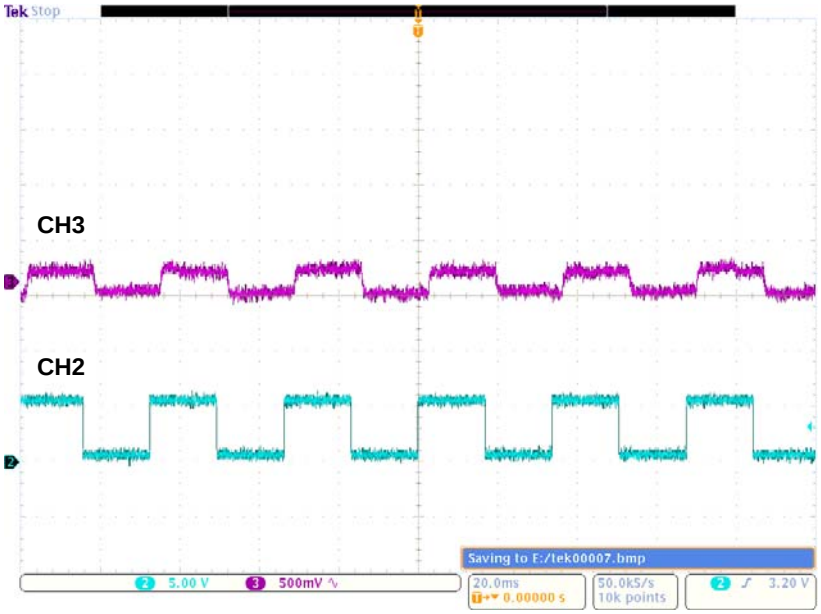

Figure 5.10 CH3: Demodulator output waveform for F = 30 Hz and impedance variation = 0.6%. CH2: Sync. test output from thorax simulator.

CHAPTER 6

SUMMARY AND CONCLUSION

The objective of the project was to develop a synchronous demodulator with automatic baseline restoration for impedance cardiography.

The entire circuit was designed to operate with a single supply. A direct digital synthesizer (DDS) based waveform generator was used to achieve high amplitude stability and to have digital control over frequency and phase. Two DDS chips were used in the waveform generator to generate synchronous sinusoidal and square waveforms with settable phase shift. The sinusoidal signal was given as input to the voltage-to-current converter and also as a baseline correction signal to the demodulator. Two digital potentiometers were used for independent control of the input to the voltage-to-current converter and the baseline correction signal. The square waveform was given to the demodulator for synchronous demodulation. A modified Howland voltage-to-current converter along with a transformer was used to provide balanced outputs and for reducing common mode pick-up. A new demodulation scheme based on synchronous current steering and sampling at the peaks was developed to improve noise rejection, interference rejection, carrier ripple rejection, and achieve high sensitivity. A tracking based baseline restoration logic was implemented as a part of the demodulator itself thus avoiding additional circuitry for implementing the same. An isolated RS232 interface was used to provide control of the instrument from a PC as well as for transfer of the acquired signals.

The entire hardware has been assembled on a two-layer PCB. The different hardware blocks were then tested and found to give satisfactory performance. Particularly the operation of the demodulator has been verified for ripple and noise rejection. The dynamic response of the demodulator, its sensitivity, and baseline restoration has to be tested using a thoracic simulator. Subsequently the circuit has to be assembled as an impedance cardiograph and detailed tests need to be carried out before its clinical use.

APPENDIX A

SCHEMATIC DIAGRAM OF THE IMPEDANCE CARDIOGRAPH

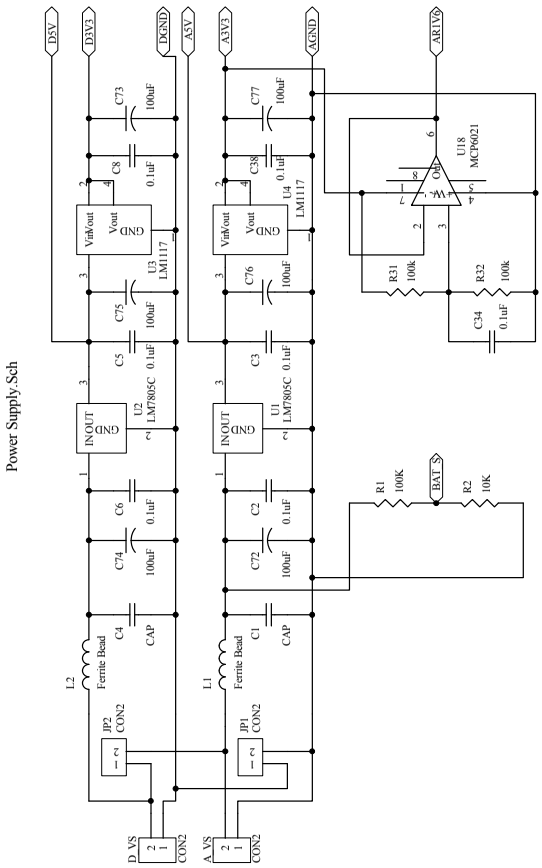

Figure A.1 Impedance cardiograph schematic sheet-1.

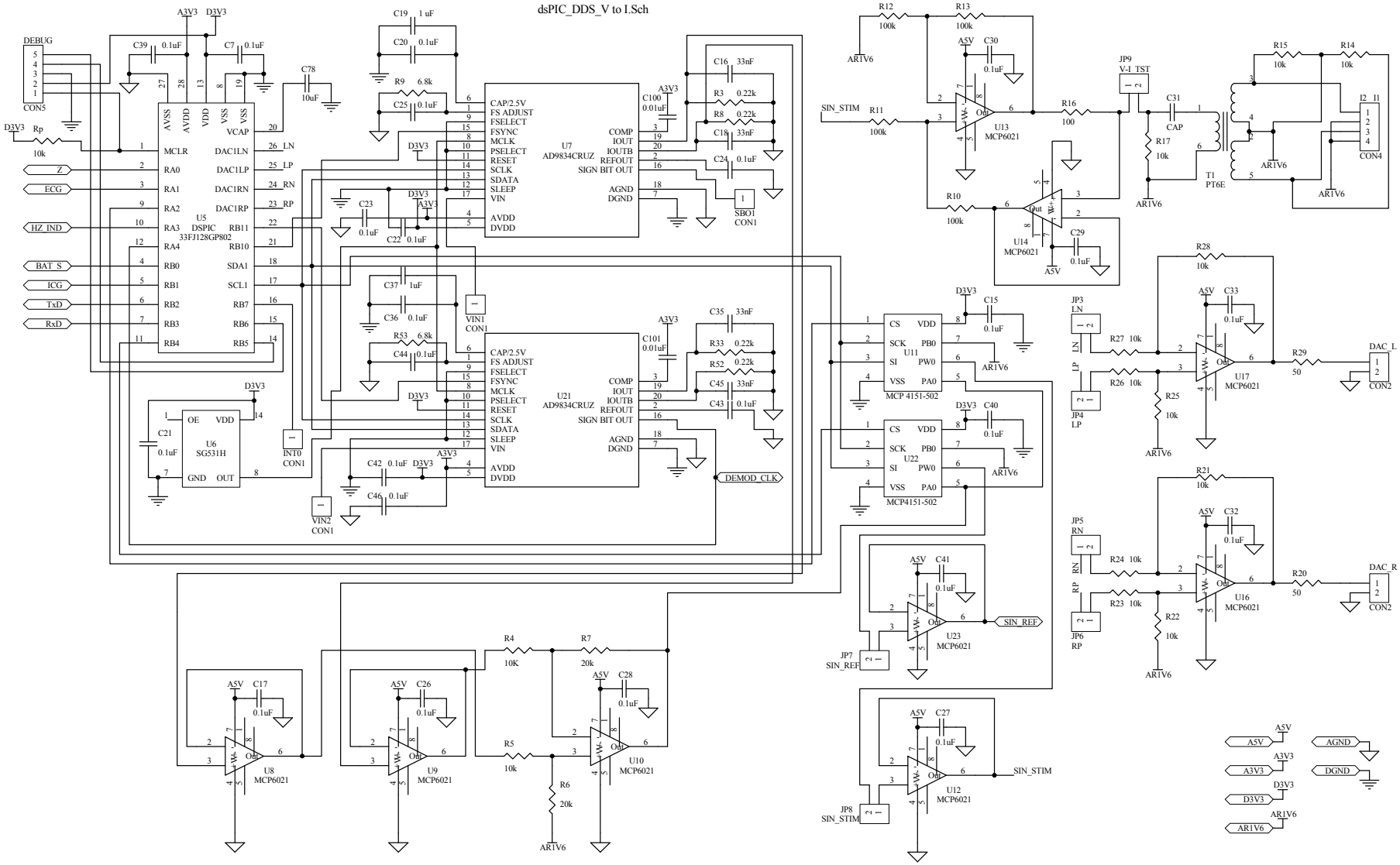

Figure A.2 Impedance cardiograph schematic sheet-2.

ECG & ICG Amp.Sch

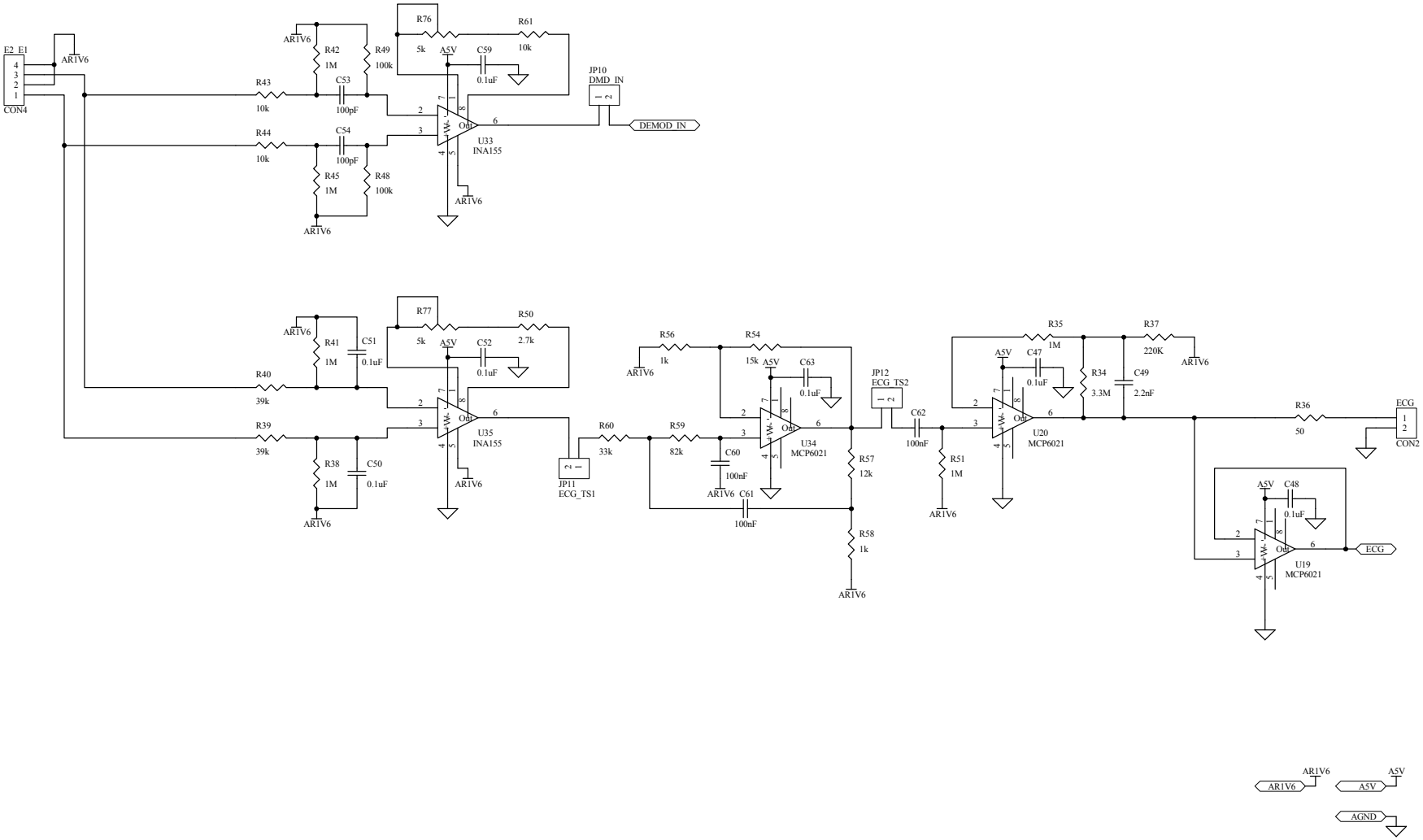

Figure A.3 Impedance cardiograph schematic sheet-3.

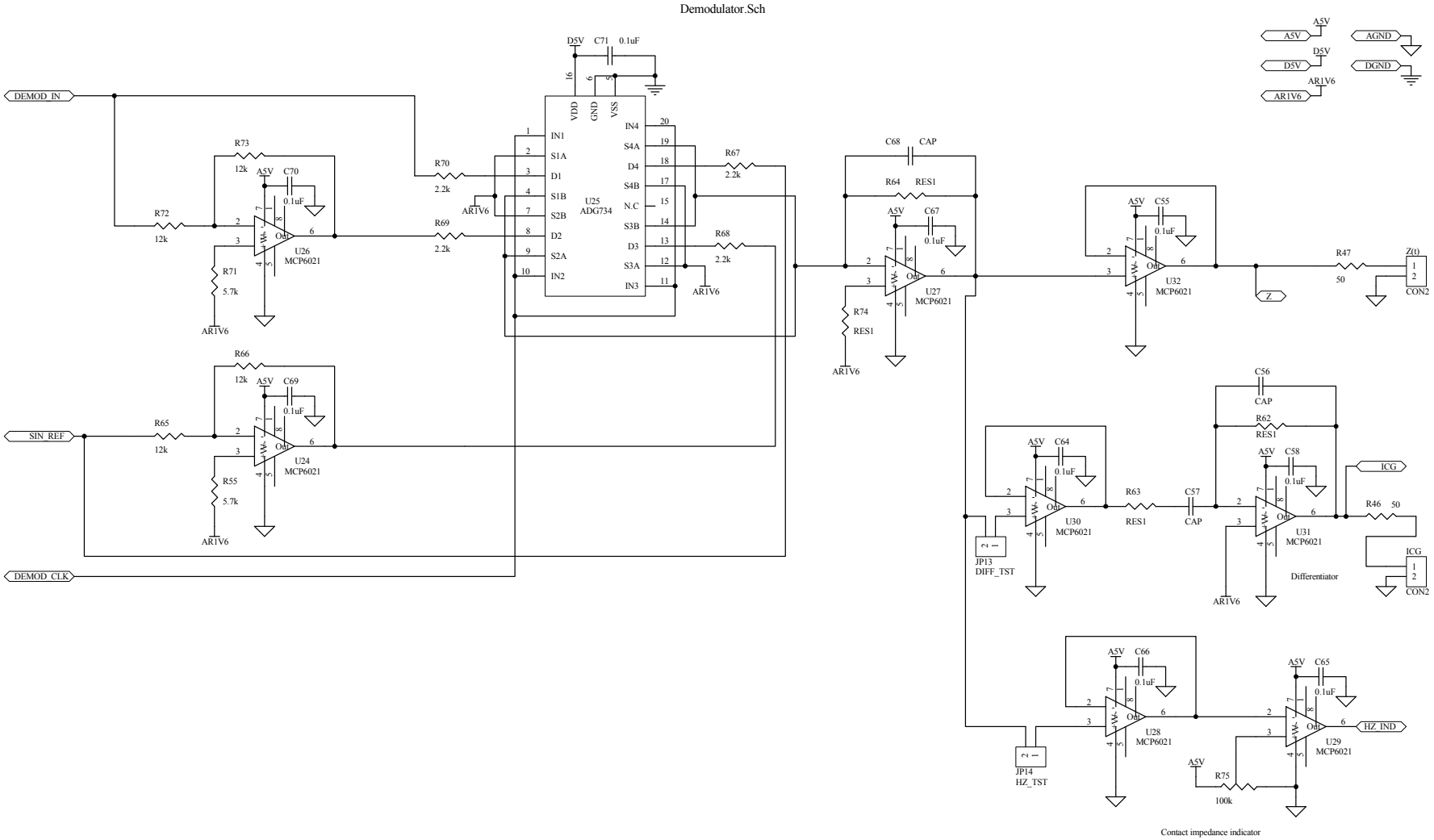

Figure A.4 Impedance cardiograph schematic sheet-4.

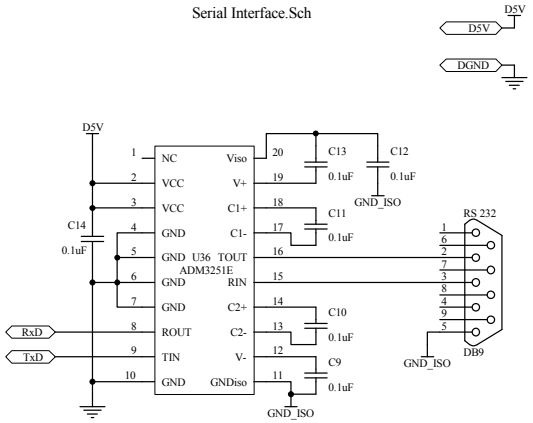

Figure A.5 Impedance cardiograph schematic sheet-5.

Master.sch (Inter-sheet connections)

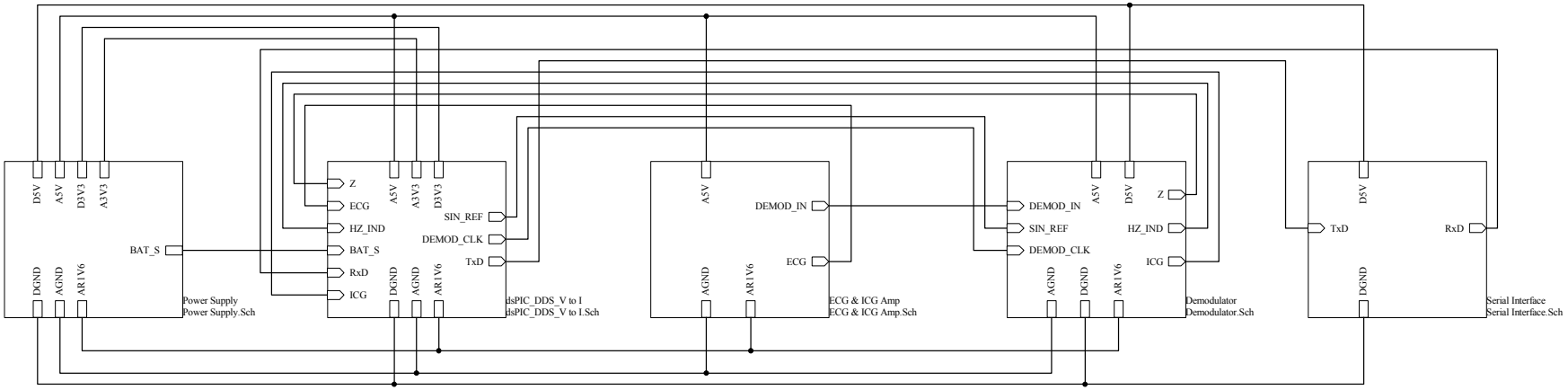

Figure A.6 Impedance cardiograph schematic sheet-6.

APPENDIX B

PCB LAYOUT OF THE IMPEDANCE CARDIOGRAPH

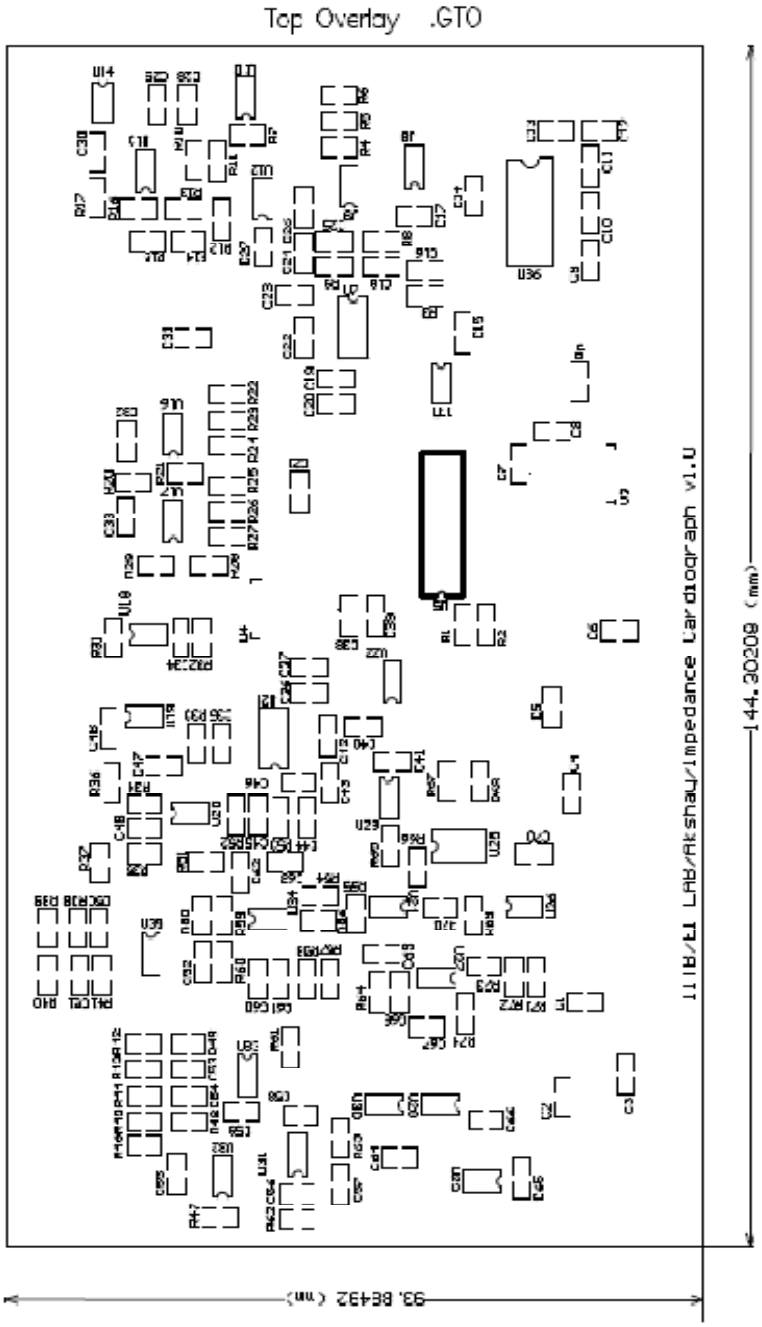

Figure B.1 Top overlay of the impedance cardiograph PCB.

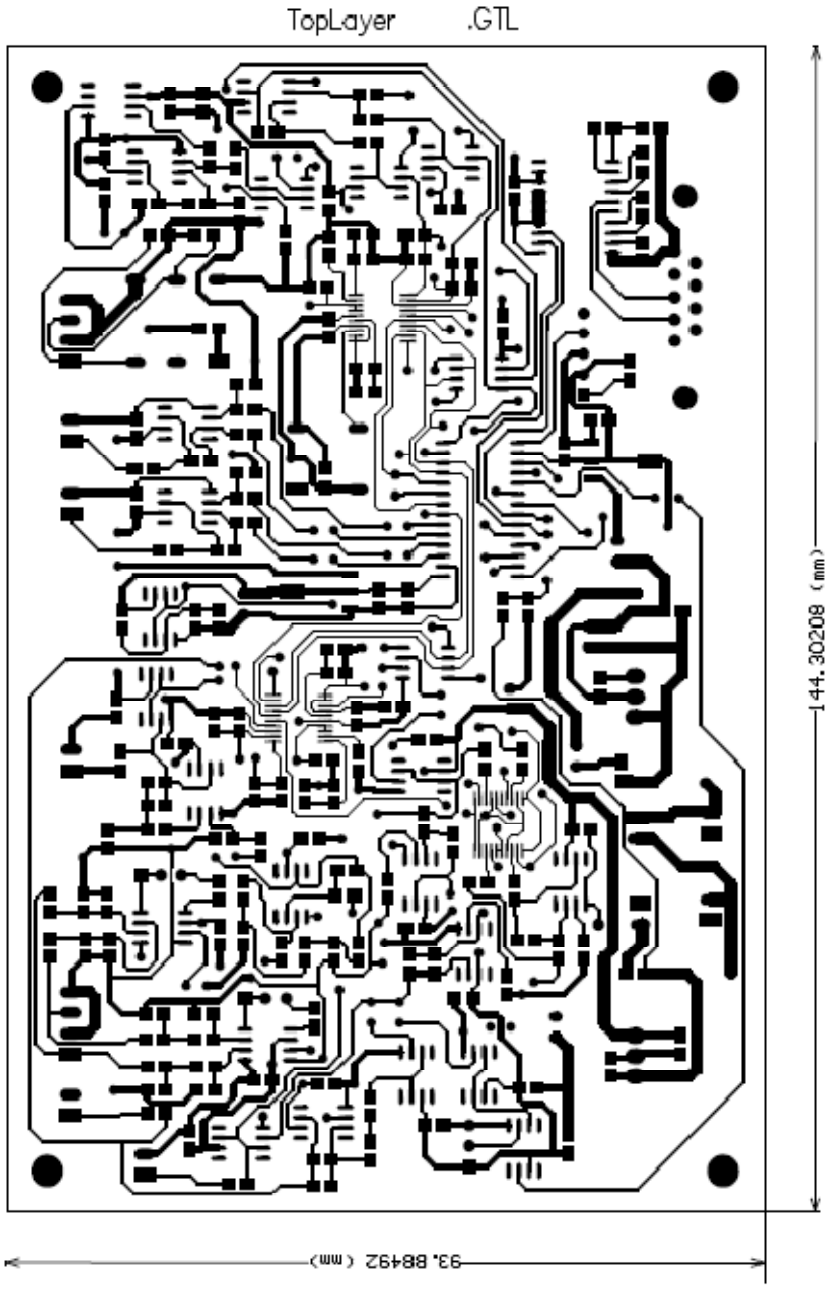

Figure B.2 Top layer of the impedance cardiograph PCB.

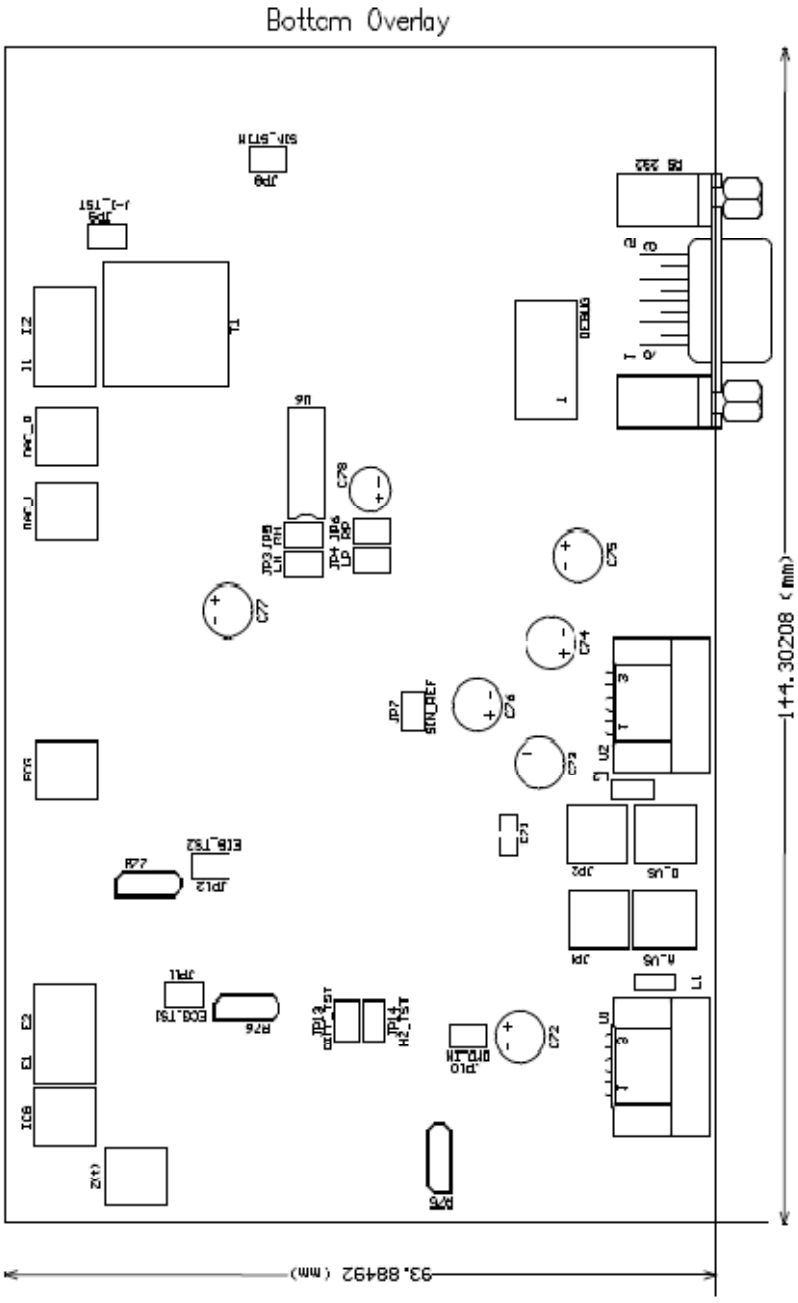

Figure B.3 Bottom overlay of the impedance cardiograph PCB.

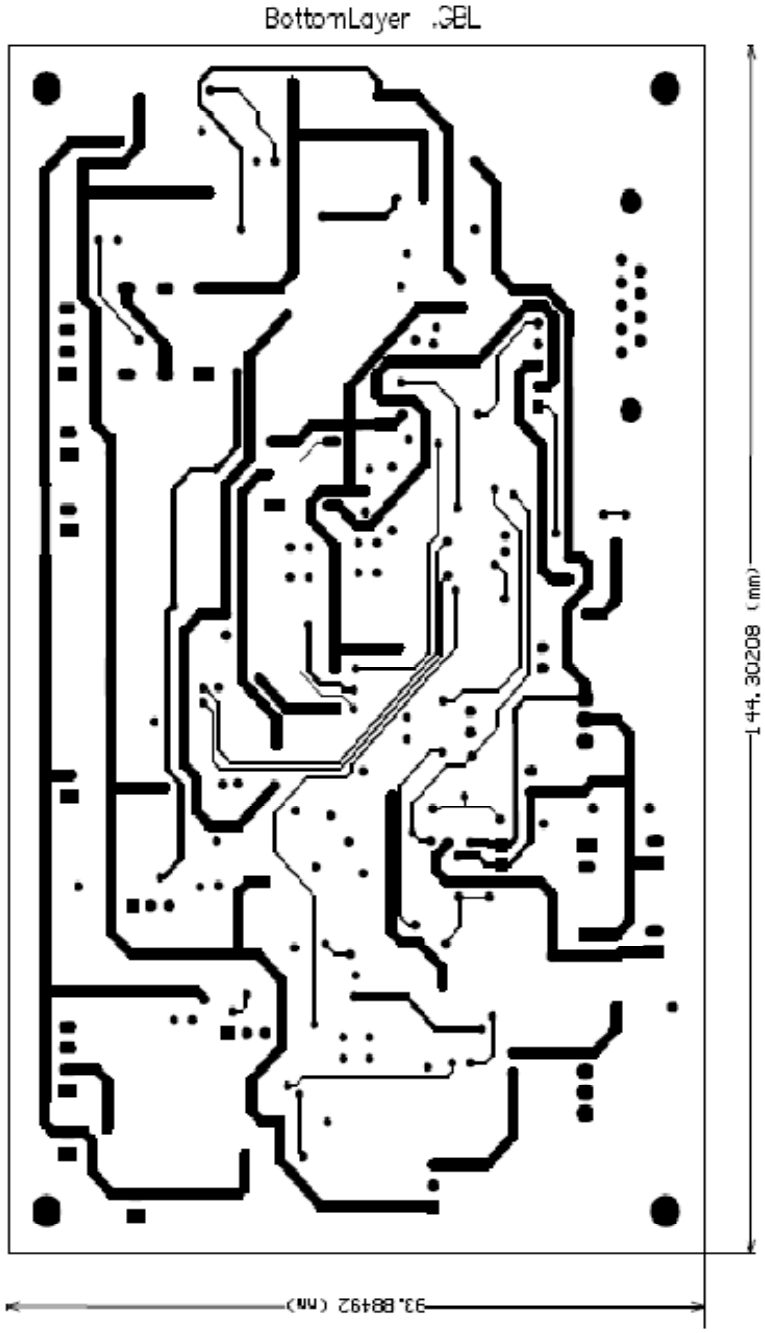

Figure B.3 Bottom layer of the impedance cardiograph PCB.

Appendix C

COMPONENT LIST

Designator	Part Number/Value	Component description	Package	Quantity
C56	100 pF	Capacitor	0805	1
C68	270 pF	Capacitor	0805	1
C49	2.2 nF	Capacitor	0805	1
C16, C18, C35, C45, C53, C54, C57	33 nF	Capacitor	0805	7
C31	47 nF	Capacitor	0805	1
C2, C3, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C17, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C32, C33, C34, C36, C38, C39, C40, C41, C42, C43, C44, C46, C47, C48, C50, C51, C52, C55, C58, C59, C63, C64, C65, C66, C67, C69, C70, C71, C60, C61, C62	0.1 µF	Capacitor	0805	56
C1, C4, C19, C37	1 µF	Capacitor	0805	4
C72, C73, C74, C75, C76, C77	100 µF	Capacitor, Electrolytic	Through hole-TH	6
C78	10 µF	Capacitor, Electrolytic	TH	1
L1, L2	-	Ferrite Bead	TH	2
R20, R29, R36, R46, R47	50 Ω	Resistor	0805	5
R16	100 Ω	Resistor	0805	1
R3, R8, R33, R52	220 Ω	Resistor	0805	4
R56, R58, R74	1 kΩ	Resistor	0805	3
R67, R68, R69, R70	2.2 kΩ	Resistor	0805	4
R50	2.7 kΩ	Resistor	0805	1
R63	3.9 kΩ	Resistor	0805	1
R55, R71	5.7 kΩ	Resistor	0805	1
R9, R53	6.8 kΩ	Resistor	0805	2
R2, R4, R5, R14, R15, R17, R21, R22, R23, R24, R25, R26. R27, R28, R43, R44, R61, Rp	10 kΩ	Resistor	0805	18
R57, R65, R66, R72, R73	12 kΩ	Resistor	0805	5
R54	15 kΩ	Resistor	0805	1
R6, R7	20 kΩ	Resistor	0805	2
R60	33 kΩ	Resistor	0805	1

R39, R40	39 kΩ	Resistor	0805	2
R59	82 kΩ	Resistor	0805	1
R1, R10, R11, R12, R13, R31, R32, R48, R49	100 kΩ	Resistor	0805	9
R37	220 kΩ	Resistor	0805	1
R35, R38, R41, R42, R51, R41, R42, R45, R62, R64	1 MΩ	Resistor	0805	10
R34	3.3 MΩ	Resistor	0805	1
R76, R77	5 kΩ	Potentiometer	TH	1
R75	100 kΩ	Potentiometer	TH	1
T1	PT6E, 1:1+1	Transformer	TH	1
U1, U2	LM7805C	5 V Regulator	TO220H, TH	2
U8, U9, U10, U12, U13, U14, U16, U17, U18, U19, U20, U23, U24, U26, U27, U28, U29, U30, U31, U32, U34	MCP601	Op amp	SOIC-8	2
U11, U22	MCP 4151-502	Digital Potentiometer	SOIC-8	2
U7, U21	AD9834CRUZ	DDS	TSSOP-20	2
U25	ADG734	Quad SPDT switch	TSSOP-20	1
U3, U4	LM1117	3.3 V Regulator	SOT-223	2
U33, U35	INA128	Instrumentation amplifier	SOIC-8	2
U36	ADM3251E	Isolator	SOIC(W)-20	1
U5	dsPIC33FJ128GP802	Microcontroller	SOIC-28	2
U6	SG531H	40 MHz Oscillator	TH	1
RS232		DB9 female connector		1
A_VS, D_VS, DAC_L, DAC_R, ECG, ICG, Z(t)		2-pin connector		7
I1_I2, E1_E2		4-pin connector		2
DEBUG		5-pin connector		1

REFERENCES

[1] L. E. Baker, "Principles of impedance technique", *IEEE Eng. Med. Biol. Mag.,* vol. 8 no. 1, pp. 11 - 15, 1989.

[2] R. P. Patterson, "Fundamentals of impedance cardiography", *IEEE Eng. Med. Biol. Mag.,* vol. 8 no. 1, pp. 35 - 38, 1989.

[3] R. Belardinelli, N. Ciampani, C. Costantini, A. Blandini, and A. Purcaro, "Comparison of impedance cardiography with Thermodilution and Direct Fick methods for noninvasive measurement of stroke volume and cardiac output during incremental exercise in patients with ischemic cardiomyopathy", *The American Journal of Cardiology*, vol. 77 no. 15, pp. 1293-1301, 1996.

[4] P. E. Aust, G. G. Belz, G. Belz, and W. Koch, "Comparison of impedance cardiography and echocardiography for measurement of stroke volume", *European Journal of Clinical Pharmacology*, vol. 23 no. 6, pp. 475-477, 1982.

[5] S. Grimnes, O. G. Martinsen, *Bioimpedance and Bioelectricity Basics*, 2nd ed., Academic Press, London, 2008.

[6] M. Qu, Y. Zhang, J. G. Webster, and W. J. Tompkins, "Motion artifact from spot and band electrodes during impedance cardiography", *IEEE Trans. Biomed. Eng.,* vol. 33 no. 11, pp. 1029 - 1036, 1986.

[7] N. S. Manigandan / P. C. Pandey (Supervisor), "Development of hardware for impedance cardiography", *M. Tech. Dissertation*, Biomedical Engineering Group, School of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2004.

[8] N. K. S. Naidu / P. C. Pandey (Supervisor), "Hardware for impedance cardiography", *M.Tech. Dissertation*, Biomedical Engineering Group, School of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2005.

[9] L. Venkatachalam /P. C. Pandey (Supervisor), "Development of hardware for impedance cardiography", *M. Tech. Dissertation*, Biomedical Engineering Group, School of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2006.

[10] B. B. Patil / Prof. P. C. Pandey (Supervisor), "Instrumentation for impedance cardiography", *M. Tech. dissertation*, Biomedical Engineering Group, School of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2009.

[11] Analog Devices, "20 mW power, 2.3 V to 5.5 V, 75 MHz complete DDS AD9834", Available online, www.analog.com/static/importedfiles/Data_Sheets/AD9834.pdf, downloaded on 10th Dec. 2010.

[12] A. C. Guyton, *Textbook of Medical Physiology*, 7th ed., Saunders, Philadelphia, 1986.

[13] G. J. Tortora, S. R. Grabowski, *Principles of Anatomy and Physiology*, 10th ed., Wiley, New York, 2003.

[14] "How heart works", National Heart Foundation of New Zealand, http://www.heartfoundation.org.nz/images/Heart%20diagram.jpg., downloaded on 15th Jun. 2011.

[15] H. H. Woltjer, H. J. Bogaard and P. M. J. M. de Vries, "The technique of impedance cardiography", *European Heart Journal,* vol. 18 no. 9, pp. 1396-1403, 1997.

[16] Z. Lababidi, D. A. Ehmke, R. E. Durnin, P. E. Leavetton, and R. M. Lauer, "The first derivative thoracic impedance cardiogram", *Circulation*, vol. 41 no. 4, pp. 651-658, 1970.

[17] L. Jensen, J. Yakimets, and K. K. Teo, "A review of impedance cardiography" *Heart & Lung*, vol. 24 no. 3, pp. 183-193, 1995.

[18] L. E. Baker, "Applications of impedance technique to the respiratory system", *IEEE Eng. Med. Biol. Mag.,* vol. 8 no. 1, pp. 50 - 52, 1989.

[19] T. Palko, "New generation impedance rheographs and examples of their clinical applications", *Biocybernetics and Biomedical Eng.,* vol. 27 no. 1/2, pp. 185-196, 2007.

[20] D. Tsunami, J. McNames, A. Colbert, S.Pearson, and R. Hammerschlag, "Variable frequency bioimpedance instrumentation", in *Proc. 26th Ann. Int. Conf. IEEE EMBS,* San Fransisco, 2004, pp. 2386-2389.

[21] J. N. Sarvaiya, P. C. Pandey, and V. K. Pandey, "An impedance detector for glottography", *IETE J.Research*, vol. 55 no. 3, pp 100-105, 2009.

[22] J. W. Lee, T. I. Oh, S. M. Paek, J. S. Lee, and E. J. Woo, "Precision constant current source for electrical impedance tomography", in *Proc. 25th Ann. Int. Conf. IEEE EMBS*, Mexico, 2003, pp.1066-1069.

[23] A. J. Fourcin, "Apparatus for speech pattern derivation", U. S. Patent No. 4,139,732, Feb. 13, 1979.

[24] M. S. Toth "Method for reducing baseline drift in a biological signal", U. S. Patent No. US20100076329, Mar. 25, 2010.

[25] S. Lee and W. Chou, "Baseline drift cancelling method and device", U. S. Patent No. US20100168595, Jul. 1, 2010.

[26] A. Cohen and R. L. Longini, "Self-balancing system for medical and physiological instrumentation," *IEEE Trans. Biomed. Eng.*, vol. 18, pp. 66–69, Jan. 1971.

[27] T. M. R. Shankar and J. G. Webster, "Design of an automatically balancing electrical impedance plethysmograph," *J. Clin. Eng.*, vol. 9 no. 2, pp. 129–134, Apr. - Jun. 1984.

[28] V. K. Pandey, N. K. S. Naidu, and P. C. Pandey, "Tracking based baseline restoration for acquisition of impedance cardiogram and other biosignals", in *Proc. 27th Annu. Int. Conf. IEEE Eng. Med. Biol.*, 2005, pp. 3486- 3489.

[29] V. K. Pandey and P. C. Pandey, "Tracking based baseline restoration circuit for acquisition of bio signals", *Electron. Letters,* vol.43 no. 9, pp. 13 - 14, Mar. 2007.

[30] Microchip, "High performance 16-bit digital signal controllers", Available online, http://ww1.microchip.com/downloads/en/DeviceDoc/70292E.pdf, downloaded on 30th Jul. 2010.

[31] B. B. Patil, P. C. Pandey, V. K. Pandey, and S. M. M. Naidu, "A high sensitivity bioimpedance detector", *Proc. Nat. Conf. on Virtual and Intelligent Instr.*, 13-14 Nov. 2009 (NCVII -09), BITS Pilani, India, Paper 9B.1.

[32] S. M. M. Naidu / Prof. P. C. Pandey (Supervisor), "Hardware for impedance cardiography", *R & D Project Report*, Electronic Systems Group, Department of Electrical Engineering, Indian Institute of Technology Bombay, Nov. 2009.

[33] H. Taub, D. Schilling, *Digital Integrated Electronics*, Intl. stud. ed., McGraw-Hill, Auckland, 1977.

[34] Microchip, "7/8-bit single/dual SPI digital POT with volatile memory", Available online, ww1.microchip.com/downloads/en/DeviceDoc/22060b.pdf,downloaded on 27th Dec. 2010.

[35] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd ed., McGraw-Hill, New Delhi, 2002.

[36] Microchip, "Rail-to-rail input/output, 10 MHz op-amps", Available online, ww1.microchip.com/downloads/en/DeviceDoc/21685d.pdf, downloaded on 27th Dec. 2010.

[37] Oxford Electrical Products, "PT6E", Available online, http:// www.oep.co.uk / pdf / PT6e.pdf, downloaded on 10th Jan. 2011.

[38] Texas Instruments, "Single-supply, rail-to-rail output, CMOS instrumentation amplifier", Available online, http://www.ti.com/lit/gpn/ina155, downloaded on 25th Dec. 2010.

[39] Fairchild semiconductors, "Triple 2-channel analog multiplexer/demultiplexer", Available online, http://www.fairchildsemi.com/ds/CD/CD4053BC.pdf, downloaded on 5th Dec. 2010.

[40] Analog Devices, "CMOS, 2.5 Ω low-voltage, quad SPDT switches", Available online, www.analog.com/static/importedfiles/Data_Sheets/ADG733_734.pdf, downloaded on 15th Jan. 2011.

[41] Analog Devices, "Isolated, single-channel, RS232 line driver/receiver", Available online, www.analog.com/static/importedfiles/Data_Sheets/ADM3215E.pdf, downloaded on 15th Jan. 2011.

[42] N. Mandloi / Prof. P. C. Pandey (Supervisor), “Development of an impedance glottograph”, *M. Tech. dissertation*, Biomedical Engineering Group, Department of Biosciences and Bioengineering, Indian Institute of Technology Bombay, 2011.

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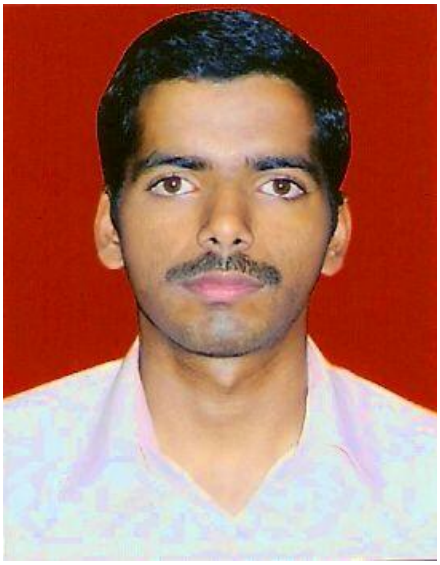
Author's Resume



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