A Bioimpedance Simulator for Impedance Cardiography

A dissertation submitted in
partial fulfilment of the requirements for the degree of

Master of Technology
in Biomedical Engineering

by

Rani Holani
(123300002)

under the supervision of

Prof. P. C. Pandey

Department of Biosciences and Bioengineering
Indian Institute of Technology Bombay
June 2014

Indian Institute of Technology Bombay

M. Tech. Dissertation Approval

This dissertation entitled "**A bioimpedance simulator for impedance cardiography**" by **Rani Holani** (Roll No. **123300002**) is approved, after the successful completion of *viva voce* examination, for the award of the degree of **Master of Technology** in **Biomedical Engineering**.

Supervisor	.....	(Prof. P. C. Pandey)
Examiners	.....	(Prof. S. Mukherji)
	.....	(Prof. L. R. Subramanyan)
Chairperson	.....	(Prof. D. K. Sharma)

Date: July 4, 2014

Place: Mumbai

Declaration

I declare that this dissertation represents my own ideas and words. I have adequately cited and referenced the original sources wherever other's ideas or words have been included. I also declare that I have adhered to all the principles of academic honesty and integrity and have not misrepresented, fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the institute and can also evoke penal action from sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

(Rani Holani)

Date: July 4, 2014

Place: Mumbai

Rani Holani/ Prof. P. C. Pandey (supervisor), "A bioimpedance simulator for impedance cardiography", M.Tech. Dissertation, Biomedical Engineering, Indian Institute of Technology Bombay, June 2014.

ABSTRACT

Impedance cardiography is a non-invasive plethysmographic technique for assessing the haemodynamic parameters which may be useful in the diagnosis of cardiac disorders. It involves monitoring of the variation in the thoracic bioimpedance during a cardiac cycle. A bioimpedance simulator is needed for simulating the thoracic impedance to test and calibrate the impedance cardiograph instrument. A bioimpedance simulator is developed for providing a continuously time-varying resistance with settable basal resistance, frequency, waveform, and peak-to-peak variation. It is designed as an interconnection of four blocks: resistance variation circuit, controller circuit, serial interface, and power supply circuit. The resistance variation circuit consists of a parallel combination of a voltage-controlled resistor (VCR) circuit for the time-varying component of the resistance and a digitally controlled resistance for the basal resistance. Novel circuits for realizing a VCR using JFETs and MOSFETs are investigated to generate resistance variation in accordance with the desired test waveforms. The VCR circuit used in the bioimpedance simulator is implemented using matched-pair n-channel JFETs, with SD-bootstrapped gate for eliminating nonlinearities occurring due to quadratic term of the drain current of JFET and self-tracking for stabilizing the channel resistance of JFET against variations due to device parameters. The voltages for controlling the channel resistance of JFET are generated by the controller circuit using a microcontroller with on-chip DAC. The switch-resistance network is implemented using a parallel combination of digitally controlled analog switches and fixed-value resistors. An isolated serial interface is provided for setting the simulation parameters of the control voltages from a PC to the microcontroller.

CONTENTS

LIST OF ABBREVIATIONS

Abbreviation	Explanation
DAC	digital-to-analog converter
ECG	electrocardiogram
GUI	graphical user interface
ICG	impedance cardiogram
ISR	interrupt service routine
JFET	junction field-effect transistor
MOSFET	metal-oxide-semiconductor field-effect transistor
SV	stroke volume
UART	universal asynchronous receiver/transmitter
VCR	voltage-controlled resistor

LIST OF SYMBOLS

Symbol	Explanation
i_D	drain current
I_{DSS}	drain saturation current
R_{DS}	drain-source channel resistance
R_o	fixed resistance in the 2-channel model of thorax
R_v	variable resistance in the 2-channel model of thorax
R_{E1E2}	resistance across the terminals E1 and E2
v_B	substrate voltage
v_{BS}	substrate-source voltage
v_C	control voltage
v_{DS}	drain-source voltage
v_G	gate voltage
v_{GS}	gate-source voltage
V_P	pinch-off voltage
V_T	threshold voltage
v_X	X-terminal voltage
v_Y	Y-terminal voltage
V_{BB}	substrate bias voltage
ΔV_T	threshold voltage shift

LIST OF FIGURES

LIST OF TABLES

Chapter 1
INTRODUCTION

1.1 Background

The electrical impedance offered by biological materials like blood, tissues, etc. is known as bioimpedance [1]. There are many applications involving bioimpedance measurements for diagnosis of abnormality in human body, such as detection of breast cancers, assessment of fluid volumes in limbs, and assessment of skin hydration [1], [2]. Blood has the highest conductivity as compared to other tissues [1], [3] and the variation in the impedance offered by the thoracic region is mainly due to change in volume of the blood during the cardiac cycle. Impedance cardiography involves non-invasive monitoring of thoracic impedance [1], [4]. It is a low-cost technique for estimating several cardiovascular indices, e.g. blood ejection time, maximum velocity of blood ejection, stroke volume, cardiac output, etc., which can be used for assessing the hemodynamic functions. For cardiac output monitoring, it is considered to be a good alternative to the established methods like thermodilution and indicator dilution, particularly because it is possible to obtain only one measurement of cardiac output per injection in dilution methods [1],[4].

The impedance measurement is carried out by injecting a high-frequency (20 – 100 kHz) and low-amplitude (< 5 mA) current in the thorax region through an electrode pair. The resulting amplitude-modulated voltage developed across the thorax is picked up by the same or another electrode pair. The sensed voltage is demodulated to extract the variation in the thoracic impedance, which is primarily caused by the change in blood volume in the thorax during the cardiac cycle. These variations are used to estimate the stroke volume, cardiac output, and other cardiovascular indices which may be useful in the diagnosis of the cardiac disorders such as mitral stenosis [4], [5].

1.2 Project objective

The project objective is to develop a bioimpedance simulator for comprehensive testing and calibration of impedance cardiograph instruments. The bioimpedance simulator consists of four modules: resistance variation circuit, controller circuit, serial interface, and power supply. The project involves designing novel circuits to generate resistance variation in accordance with the desired test waveforms (sine, square, and thoracic impedance waveform). In addition, the simulator has to simulate differential and common mode ECG and other

external pickups in order to test ECG extraction and interference rejection features of the impedance cardiograph instrument. A voltage-controlled resistor circuit is developed for realizing time varying impedance. The controller circuit is devised using a microcontroller for generation of various control waveforms. The circuit is battery powered. A serial interface is provided for setting the measurement parameters in the microcontroller using a user interface program on a PC.

1.3 Report outline

Chapter 2 deals with the basics of impedance cardiography. A voltage-controlled resistor circuit is presented in Chapter 3. Chapter 4 describes thoracic impedance simulator used for objective testing of the impedance cardiograph circuit. Chapter 5 describes the test procedures along with the results. The last chapter summarizes the work carried out with conclusions and future work.

Chapter 2
IMPEDANCE CARDIOGRAPHY BASICS

2.1 Introduction

Impedance cardiography is a non-invasive technique for assessment of cardiovascular functioning by measurement of variations in thoracic bioimpedance [1], [4]. The change in impedance can be due to several reasons such as volumetric variations of blood in the arteries, change in the specific resistivity of blood as a function of blood velocity and variation in amount of air in the lungs due to ventilation [1]. The impedance changes due to ventilation represent an unwanted signal in determination of cardiovascular parameters [6]. The thoracic impedance consists of two components: the basal impedance due to the organs, muscle, bone etc. present in the thorax, which stays relatively constant with time and other is the time-varying impedance superimposed on the basal impedance, and it varies with the cardiac cycle. The normal range of basal impedance is 20 – 200 Ω and the variations in the impedance lie in the range of about 0.1 – 2% of the basal impedance [4].

In this technique, a high-frequency low-amplitude current is injected into the thorax of the subject through an electrode pair and the resulting amplitude-modulated voltage developed across the thorax is picked up using the same or another electrode pair as shown in Figure 2.1. This voltage is fed to a difference amplifier for amplification. The amplified signal is then fed to demodulator for extraction of bioimpedance signal which is further differentiated to get the impedance cardiogram (ICG). As thoracic impedance variation over the basal impedance is in the range of 0.1−2% of the basal impedance, the sensed voltage has the modulation index in this range. The impedance measurement is carried out using excitation current in frequency range of 20 – 100 kHz and of amplitude less than 5 mA to avoid any possibility of physiological effects and sensations. In this frequency range, the reactance of cell membrane capacitance is very low allowing the injected current to penetrate though the cell membranes and the impedance offered by thorax region is almost resistive in nature [7]. Further, use of high frequency reduces the effect of variation in tissue-electrode contact impedance [4]. The use of higher frequency also helps in suppressing the carrier ripple from the demodulated impedance signal.

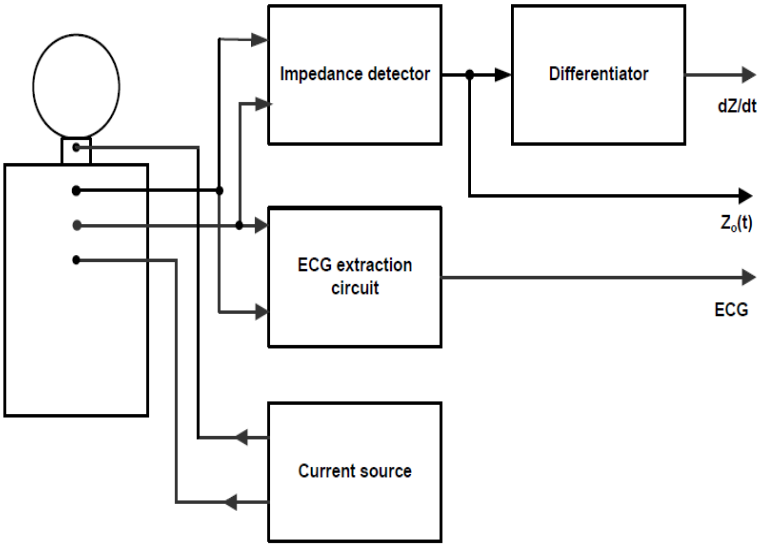


Figure 2.1: Block diagram of Impedance Cardiography [8].

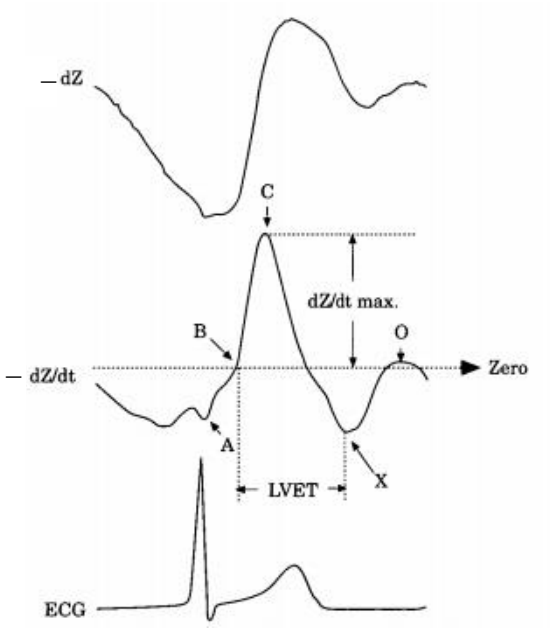


Figure 2.2: Typical dZ, -dZ/dt and ECG waveform [6].

2.2 Significance of ICG waveform

Bioimpedance is an effective measure for identifying changes of many different conditions in the patient's body, such as pulmonary edema [7]. For example, in the patient suffering from pulmonary edema, the accumulation of fluids in the lung-region occurs resulting in variation in thoracic impedance, since the resistivity of the lung changes in accordance with the change of the ratio of fluid to air. So, it is possible to detect pulmonary edema at an early stage, by means of transthoracic impedance measurement. Figure 2.2 shows typical impedance and ECG waveform obtained from electrodes. In dZ/dt curve, the A-point signifies atrial contraction, the B-point is correlated with aortic valve opening, the C-point is the peak of the

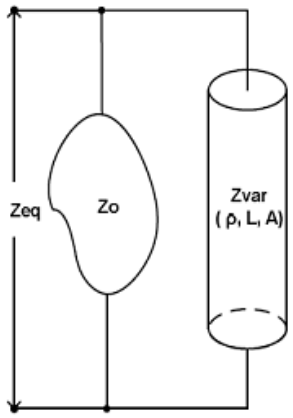


Figure 2.3: Parallel-column model [4].

waveform occurring during systole due to the increased blood flow into the aorta, the X-point coincides with aortic valve closure, and the O-point indicates diastolic upward deflection [11]. As the maximum point of the O-wave coincides with the mitral valve opening snap, elevation in the same can be noticed in patients suffering from mitral stenosis [4], [5]. Thus, analysis of the ICG waveform leads to detection of various heart abnormalities.

The model developed to quantify impedance variations is known as parallel-column model [4], as shown in Figure 2.3. The assumption made in the model is that constant impedance Z_0 is connected in parallel with a cylindrical column with variable impedance having a uniform variable cross-sectional area *A*, fixed length *L*, and fixed resistivity ρ. The model assumes that the electric current distribution in the cylinder is homogenous. The maximum change in the impedance ΔZ and the maximum change in the volume ΔV can be related as [4]

$$\Delta V = \left(\frac{\rho L^2}{Z_0^2} \right) \Delta Z \tag{2.1}$$

This model assumes that there is no outflow of the blood from the thorax during systole and just before systole, the volume of the variable impedance column is zero. According to the Kubicek equation, [4], the stroke volume is directly proportional to $\left(-dZ/dt\right)_{\max}$ and T_{LVET} .

$$\text{SV} = \left(\frac{\rho L^2}{Z_0^2} \right) \left(-dZ/dt\right)_{\max} T_{LVET} \tag{2.2}$$

One of the limitations of this equation is that the thorax is modelled as a cylinder. Also determining the values of ρ and *L* is difficult. Impedance Z_0 is directly proportional to the length *L*, and the blood resistivity ρ but inversely proportional to the cross-sectional area *A* as given in the following equation [9].

$$Z_0 = \rho L / A \tag{2.3}$$

Rearranging equations (2.2) and (2.3) we obtain

$$\text{SV} = V \frac{(-dZ/dt)_{\max}}{Z_0} T_{LVET} \tag{2.4}$$

where V is the volume of thorax participating in electrical activity. Sramek considered the thorax to be a truncated cone and proposed an equation assuming that L equals about 17% of a person's height H and volume V as $L^3/4.25$ [6].

$$\text{SV} = \left(\frac{(0.17H)^3}{4.25Z_0} \right) (-dZ/dt)_{\max} T_{LVET} \tag{2.5}$$

A weight correction factor δ was introduced by Bernstein giving rise to Sramek-Bernstein equation [6].

$$\text{SV} = \delta \left(\frac{(0.17H)^3}{4.25Z_0} \right) (-dZ/dt)_{\max} T_{LVET} \tag{2.6}$$

It may be noted that two parameters common to all these equations are

i. $(-dZ/dt)_{\max}$, the ICG peak which occurs during systole

ii. T_{LVET} , the left ventricular ejection time

Therefore these ICG parameters should be accurately estimated.

2.3 Electrode configuration

There are two electrode configurations commonly used for injecting excitation current into the body and sensing amplitude modulated voltage: bipolar and tetra-polar. In the bipolar or two-electrode configuration, injection of current and sensing of voltage is done using the same pair of electrodes. In the tetra-polar or four-electrode configuration, current is injected by a pair of electrodes and voltage is sensed by another pair of electrodes. The advantage of using the tetra-polar electrode configuration over the bipolar electrode configuration is that the measured voltage does not get affected by the contact impedance of the electrodes as a high input impedance amplifier is used for voltage sensing [7]. The two types of electrodes commonly used in both of the configurations are spot and band electrodes. Placement of the spot electrodes is easy but the non-uniform current density due to them may lead to errors in measurement. Band electrodes provide a more uniform current density but placing them may cause inconvenience to the patients [7]. In addition, the band electrodes are more expensive than spot electrodes [10]. Therefore, an array of spot electrodes is preferred over band electrodes for long-term monitoring.

Several electrode placements using the spot-electrode arrays have been reported in the literature to achieve homogeneous electrical field across the thorax and to improve the impedance measurement. Figure 2.4 shows some of these placements. LL in Figure 2.4 signifies left lateral spot electrode array, commonly known as tetra-polar electrode

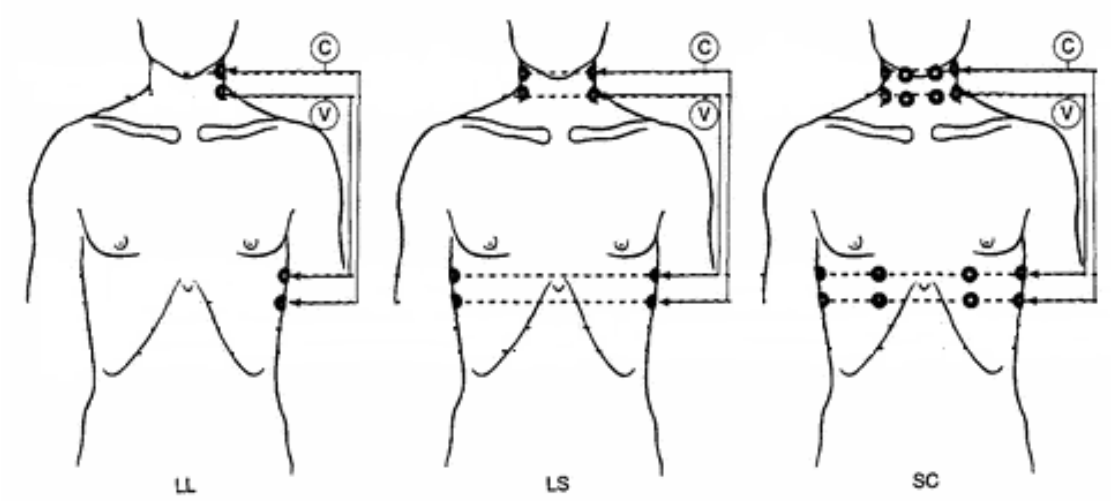


Figure 2.4: Electrode configurations using spot electrode array [11].

configuration. LS refer to the eight laterally placed spot electrodes as used by Bernstein [12] for obtaining ICG signal. Woltjer et al. [11] developed a 16-electrode array, commonly known as semi-circular (SC) spot electrode array. The electrodes placed at the same level are shorted together. Electrodes marked as C are used for current injection while the electrodes marked as V are used for voltage sensing (marked as V).

2.4 Thoracic impedance simulator

For testing the linearity, sensitivity, and dynamic response of the impedance cardiograph measuring instrument, a bioimpedance simulator is needed for simulating the thoracic impedance. Many circuits have been reported earlier which simulate square wave resistance variation with settable frequency and resistance [8], [13] – [16]. Using analog switches, it is possible to devise resistance variation with arbitrary waveform in discrete steps. However, use of analog switches may introduce glitches in the resulting waveform at the points which involve status change of multiple analog switches. Discrete changes in resistance and possibility of glitches pose a problem for the differentiator used in the ICG instrument. Therefore, it is desirable to develop a circuit for providing a continuous variation in the resistance. The proposed circuit permits variation in resistance in accordance with a continuously varying voltage control voltage with frequency of 0.1 Hz – 100 Hz and with any waveform which may be selected to be sine, square, or a typical thoracic impedance waveform. A sinusoidal waveform can be used for obtaining the frequency response of the impedance sensor of the instrument. Quick assessments of its dynamic response can be made using a square wave or a triangular wave. The overall operation of the instrument can be tested using the thoracic impedance waveform.

Chapter 3
VOLTAGE-CONTROLLED RESISTOR CIRCUIT

3.1 Introduction

As described in the last section of the previous chapter, the key component of thoracic impedance simulator is a circuit for producing a continuous resistance variation in accordance with a time-varying control voltage. A JFET or MOSFET can be used as a voltage-controlled resistor (VCR), but it acts as a linear resistor for a small range of drain-source voltage. The relationship between the gate-source voltage and the drain-source resistance is dependent on device parameters which may vary with temperature and also may have a significant piece-to-piece variation. A feedback circuit using a matched pair of devices is presented to decrease the effect of device parameters on the resistance and to increase the range of drain-source voltage for linear behavior. This circuit is devised such that neither of the terminals of the resistance needs to be grounded and therefore it can be used in applications requiring a floating VCR or resistance mirror. The circuit is devised using JFETs as well as MOSFETs. In addition to its use in realizing a thoracic impedance simulator, the circuit has several other applications such as analog multipliers, modulators, demodulators, volume controllers, and programmable circuits.

3.2 JFET and MOSFET as a VCR

A JFET can act as a VCR for a small range of drain-source voltage. It is a three-terminal device with source (S), gate (G), and drain (D) terminals [17], [18]. Figure 3.1 shows an n-channel JFET with typical drain characteristics. During its normal operation, drain-source voltage should be positive and gate-source junction should be reversed biased, i.e. $v_{DS} \geq 0$ and $v_{GS} \leq 0$. With $v_{GS} = 0$, the drain current i_D increases as v_{DS} is increased until it reaches the saturation current I_{DSS}. The current decreases as the reverse bias on the gate-source junction is increased and the current becomes zero for $v_{GS} = V_P$, which is known as the pinch-off voltage and its value is negative for n-channel devices. The region with $v_{GS} \leq V_P$ is known as the cut-off region. For $V_P \leq v_{GS} < 0$, and $v_{DS} < v_{GS} - V_P$, i_D increases with v_{DS} and this region is known as the triode or ohmic region. For $V_P \leq v_{GS} < 0$ and $v_{DS} > v_{GS} - V_P$, i_D reaches a saturation level, becoming almost independent of v_{DS}.

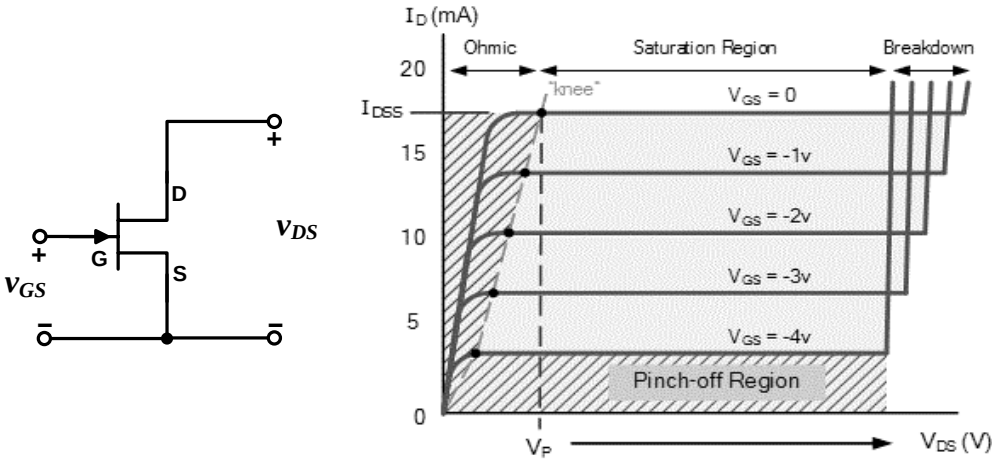


Figure 3.1:.A n-channel JFET and its drain characteristics (adapted from Figure 14.2 in [17]).

This region is known as the saturation region. As v_{DS} is further increased, the channel breakdown occurs and results in a large current, marked as the breakdown region in the figure. The relationship between drain current i_D and drain-source voltage $v_{DS}(>0)$ is approximately modeled as the following:

$$i_D = \begin{cases} 0, & v_{GS} \le V_P \\ I_{DSS}\left(\dfrac{2(v_{GS}-V_P)v_{DS}-v_{DS}^2}{V_P^2}\right), & V_P \le v_{GS} < 0 \quad \text{and} \quad v_{GD} > V_P \\ I_{DSS}\left(1-\dfrac{v_{GS}}{V_P}\right)^2, & V_P \le v_{GS} < 0 \quad \text{and} \quad v_{GD} < V_P \end{cases} \tag{3.1}$$

The channel resistance $R_{DS} = v_{DS}/i_D$ is given as the following:

$$R_{DS} = V_P^2/[2I_{DSS}(v_{GS}-V_P-v_{DS}/2)] \tag{3.2}$$

For small values of v_{DS}, the channel resistance R_{DS} can be approximated as a linear resistance with the value given as the following:

$$R_{DS} = V_P^2/[2I_{DSS}(v_{GS}-V_P)], \quad v_{DS} << v_{GS}-V_P \tag{3.3}$$

This has the smallest value for $v_{GS} = 0$ and is given as

$$R_{DS,ON} = |V_P|/(2I_{DSS}) \tag{3.4}$$

The expression for i_D in (3.1) can also be written as the following:

$$i_D = \begin{cases} 0, & v_{GS} \le V_P \\ k[(v_{GS}-V_P)v_{DS}-{v_{DS}}^2/2], & V_P \le v_{GS} < 0 \quad and \quad v_{GD} > V_P \\ k[(v_{GS}-V_P)^2/2], & V_P \le v_{GS} < 0 \quad and \quad v_{GD} < V_P \end{cases} \tag{3.5}$$

where the value of *k* is given as

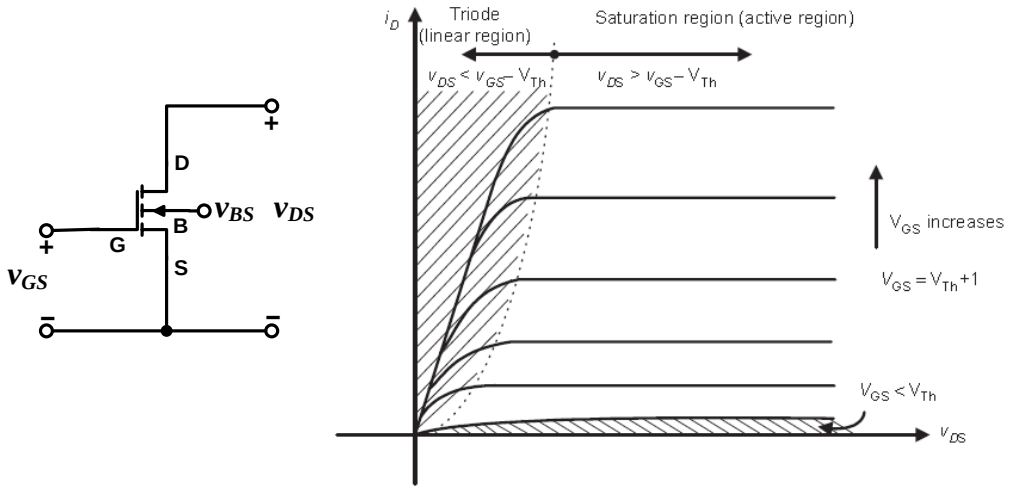


Figure 3.2: An enhancement-type NMOS transistor and its drain characteristics (adapted from Figure 4.11 in [19]).

$$k = 2I_{DSS} / V_P^2 \tag{3.6}$$

The value of the pinch-off voltage V_P and that of $R_{DS,ON}$ are given as

$$|V_P| = qN_D a^2 / 2\varepsilon \tag{3.7}$$

$$R_{DS,ON} = l/(2awqN_D\mu) \tag{3.8}$$

where l = channel length, w = channel width, a = channel thickness, q = electronic charge, N_D = concentration of donor ions, μ = carrier mobility in the device channel, and ε = dielectric constant of material of the channel [17]. Using (3.4), (3.7), and (3.8), the value of k in (3.6) can be given as the following:

$$k = 4\mu\varepsilon w/(al) \tag{3.9}$$

The values of V_P and k have device-to-device spread and also vary with temperature.

A MOSFET also can act as a voltage-controlled linear resistor for a limited range of drain-source voltage. Figure 3.2 shows an enhancement-type NMOS transistor as a four-terminal device with source (S), gate (G), drain (D), and substrate (B) terminals [17], [19], [20]. Figure 3.2 also shows the typical drain characteristics of such a device. The relation between drain current i_D and drain-source voltage $v_{DS}(>0)$ can be approximated by the following equation

$$i_D = \begin{cases} 0, & v_{GS} \le V_T \\ k[(v_{GS} - V_T)v_{DS} - {v_{DS}}^2/2], & v_{GS} > V_T \quad \text{and} \quad v_{GD} > V_T \\ k[(v_{GS} - V_T)^2/2], & v_{GS} > V_T \quad \text{and} \quad v_{GD} < V_T \end{cases} \tag{3.10}$$

where k is a constant dependent on the gate oxide layer and the channel geometry and V_T is the turn-on threshold voltage which has a positive value for n-channel enhancement-mode devices. This equation resembles to (3.5) which signifies the similarity in the operating

principles and electrical characteristics of JFET and MOSFET. The relationship assumes that the substrate-channel junction is reverse-biased and the effect of channel modulation due to variation in the channel-substrate voltage is ignored. The current i_D is zero for $v_{GS} \le V_T$ and this region is known as the cut-off. For supra-threshold gate-source voltage and $v_{DS} < v_{GS} - V_T$, the current i_D has a dependence on drain-source voltage v_{DS} and this region is known as the triode region. For $v_{DS} \ge v_{GS} - V_T$, the current i_D does not depend on drain-source voltage v_{DS} and this region is known as the saturation region.

The value of *k* for a MOSFET is given as

$$k = \mu C_{OX} w / l \tag{3.11}$$

where μ is the carrier mobility in the device channel, C_{OX} is the gate oxide layer capacitance per unit area, and *l* and *w* are channel length and width, respectively [19]. The value of *k* can also be written as

$$k = \mu \varepsilon w / (bl) \tag{3.12}$$

where b is the oxide layer thickness.

The carrier mobility μ decreases with temperature and is often approximated as a function of absolute temperature T as the following:

$$\mu(T) = \mu_0 (T_0 / T)^m \tag{3.13}$$

where μ_0 is the mobility at the reference temperature T_0 and m is a constant with a value of $1.2 - 2$ [20], [21]. The threshold voltage V_T depends on temperature, device parameters, and substrate-source bias [29]. The temperature dependence of threshold voltage V_T can be approximated by the following equation:

$$V_T(T) = V_T(T_0) - K(T - T_0) \tag{3.14}$$

where T is the absolute temperature, T_0 is the reference temperature (usually 25 ˚C), and K is the temperature drift coefficient for the threshold voltage [20]. With v_{BS} = 0 V, the threshold voltage V_T is given by the following equation

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_{Si} q N_A (2\psi_B)}}{C_{OX}} \tag{3.15}$$

where ψ_B is the body Fermi potential, ε_{Si} is the relative permittivity of silicon, N_A is the doping concentration of the body, V_{FB} is the flat-band voltage, and q is charge on electron [20]. The effect of v_{BS} on i_D can be modeled as a threshold voltage shift ΔV_T and can be given as the following:

$$V_T(v_{BS}) = V_T(v_{BS} = 0) + \Delta V_T \tag{3.16}$$

The shift ΔV_T is given as the following:

$$\Delta V_T = \frac{\sqrt{2\varepsilon_{Si} q N_A}}{C_{OX}} \left(\sqrt{|2\psi_B + v_{BS}|} - \sqrt{|2\psi_B|} \right) \tag{3.17}$$

In the triode region, the channel resistance $R_{DS} = v_{DS} / i_D$ can be controlled by the gate voltage v_{GS} and is given as

$$R_{DS} = \frac{1}{k(v_{GS} - V_T - v_{DS}/2)}, \quad v_{DS} < v_{GS} - V_T \tag{3.18}$$

For very small drain-source voltage v_{DS}, the channel resistance R_{DS} can be approximated as a linear resistance as given in the following equation:

$$R_{DS} = \frac{1}{k(v_{GS} - V_T)}, \quad v_{DS} << v_{GS} - V_T \tag{3.19}$$

As the resistance depends on device parameters *k* and V_T, it may have a significant piece-to-piece variation. It changes with operating temperature and also due to changes in substrate-channel bias. For low values of v_{DS}, the substrate may be connected to the source or another voltage to maintain a constant reverse bias across the substrate-channel junction. However, for a larger v_{DS}, different points of the channel have a different bias with respect to the substrate and therefore, a dependence on v_{DS} gets introduced due to modulation of the channel by the substrate-channel bias.

3.3 Circuits for improving VCR operation

In many applications, there is need for a VCR working as a linear resistance for a large voltage range. The device and temperature dependent variations in the resistance also need to be reduced. In some applications, it is desirable that neither terminal of the VCR is grounded, i.e. it can act as a floating resistor. Some applications require a resistance mirror, i.e., a resistance whose value is proportional to another variable resistance. Many circuits [22] − [31], [45] have been reported which satisfy one or more of the above mentioned criteria but not all.

Some of the circuits for extending the range of linearity have used combination of transistors operating in the triode and saturation regions in order to eliminate the nonlinearity due to the quadratic term in the expression for drain current [24], [28], [29]. In one such circuit, Moon et al. [24] reported a voltage-controlled resistor using enhancement-type MOSFETs. The circuit, as shown in Figure 3.3, has two matched transistors. The transistor M1 with its drain-gate shorted operates in the saturation region. A voltage source E_1 is introduced at the source terminal of M1 so that its gate-source voltage remains above the threshold voltage for the applied range of drain-source voltage. The drain current i_1 flowing through M1 is given as the following:

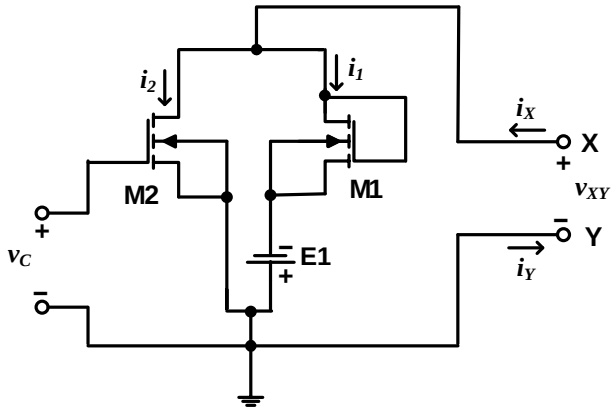


Figure 3.3: Enhancement-type MOSFET-based circuit for voltage-controlled linear resistor as proposed by Moon et.al. [24].

$$i_1 = k_1(v_X + E_1 - V_{T1})^2/2, \quad v_X + E_1 \geq V_{T1} \tag{3.20}$$

The control voltage v_C is applied at the gate terminal of the transistor M2. Assuming that v_C and v_{XY} are such that M2 is in the triode region, its drain current i_2 is given as the following:

$$i_2 = k_2[(v_C - V_{T2})v_X - v_X^2/2], \quad v_C > V_{T2},\ v_C \geq v_X + V_{T2} \geq 0 \text{ and } v_X > 0 \tag{3.21}$$

The total current i_X $(= i_Y)$ flowing in the circuit is the sum of i_1 and i_2 and it can be given as

$$i_X = k_1(v_X + E_1 - V_{T1})^2/2 + k_2[(v_C - V_{T2})v_X - v_X^2/2], \quad v_C > V_{T2} \text{ and } v_C - V_{T2} \geq v_X \geq V_{T1} - E_1 \tag{3.22}$$

For matched pair of transistors, $k_1 = k_2 = k$ and $V_{T1} = V_{T2} = V_T$. Under these conditions, the two quadratic terms involving v_X cancel out and we get

$$i_X = k[(v_C + E_1 - 2V_T)v_X + (E_1 - V_T)^2/2], \quad v_C > V_T \text{ and } v_C - V_T \geq v_X \geq V_T - E_1 \tag{3.23}$$

The offset term involving $(V_T - E_1)^2$ is eliminated by selecting $E_1 = V_T$. Under this condition, the resistance $R_X = v_X / i_X$ can be expressed by the following equation:

$$R_X = \frac{1}{k(v_C - V_T)}, \quad v_C > V_T \text{ and } v_C - V_T \geq v_X \geq 0 \tag{3.24}$$

It may be noted that a MOSFET acts as a linear resistor for $v_{XY} << v_C - V_T$. In the circuit proposed by Moon et al. [24], the range is extended to $v_X \leq v_C - V_T$. This circuit does not eliminate dependence of the resistance on the device parameters *k* and V_T and it does not provide a floating resistance. Further, insertion of the voltage source E_1 matched to V_T poses a practical difficulty in use of this circuit.

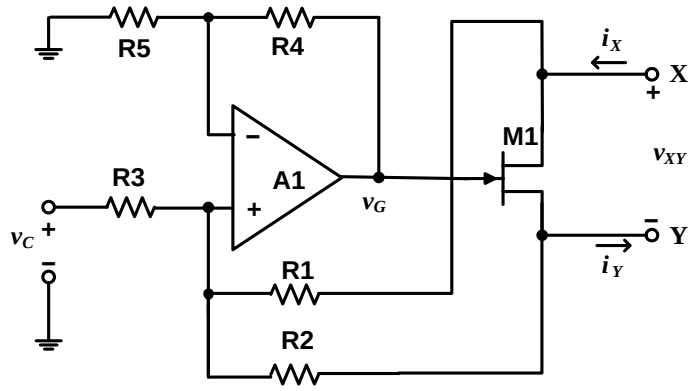


Figure 3.4: Floating VCR circuit as proposed by Senani [22].

Another way to cancel the nonlinearity in a grounded VCR is to provide a feedback from drain to gate in which sum of half of the drain and control voltage is applied to the gate terminal of the transistor [22], [30], [31]. Extending this approach, Senani [22] realized a JFET-based floating VCR circuit in which the drain voltage v_X and source voltage v_Y are superimposed on the control voltage v_C to obtain the gate voltage v_G. The circuit is realized with an op amp, a JFET and five resistors as shown in Figure 3.4. The resistances R_1, R_2, and R_3 are selected to be 1 MΩ, so that the currents drawn from the drain and source terminals are negligibly small and $i_X \approx i_Y$. The gate voltage v_G is given as

$$v_G = (v_C + v_X + v_Y)/2 \tag{3.25}$$

Assuming $v_X > v_Y$ and M1 to be in the triode region, its drain current is given as the following:

$$i_X = k[(v_G - v_Y - V_P)(v_X - v_Y) - (v_X - v_Y)^2/2], \quad 0 \geq v_G - v_Y \geq V_P \text{ and } 0 \geq v_G - v_X \geq V_P \tag{3.26}$$

Using the gate voltage v_G as given in (3.25), the drain current is given as

$$i_X = k(v_C/2 - V_P)(v_X - v_Y) \tag{3.27}$$

showing cancellation of the quadratic term. The condition for the triode region operation of M1 as in (3.25) can be rewritten as the following:

$$0 \geq (v_C + v_X + v_Y)/2 - v_Y \geq V_P \text{ and } 0 \geq (v_C + v_X + v_Y)/2 - v_X \geq V_P$$

which can be simplified as

$$0 \geq (v_C + v_X - v_Y)$$

$$(v_C + v_X - v_Y) \geq 2V_P$$

$$0 \geq (v_C - v_X + v_Y)$$

$$(v_C - v_X + v_Y) \geq 2V_P$$

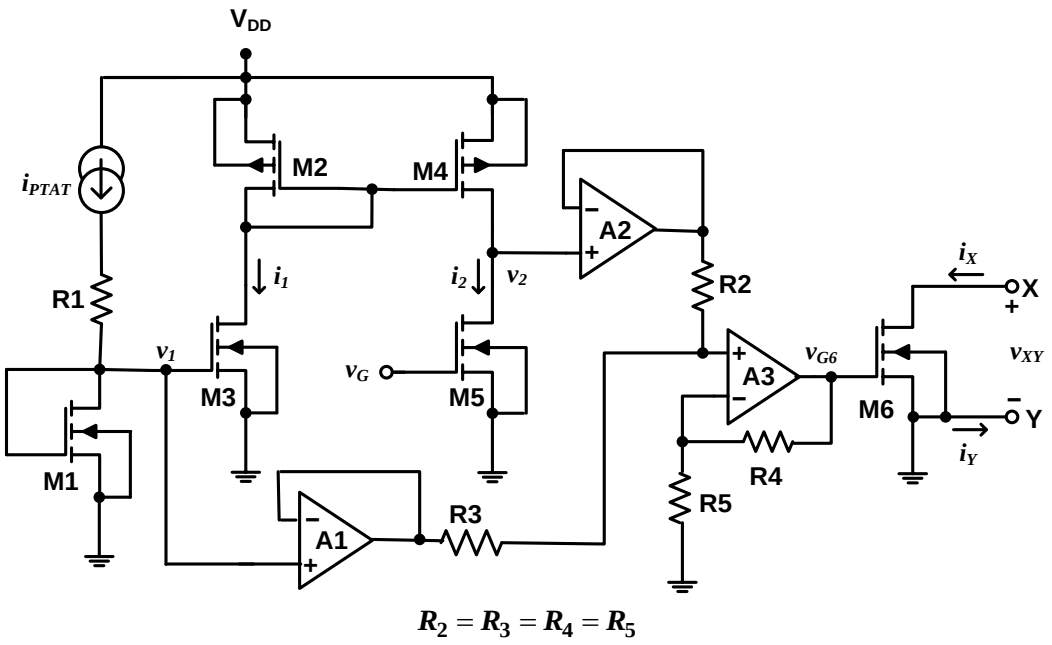


Figure 3.5: MOS resistor as proposed by Fort [26].

For $v_X = v_Y$, we get $0 \geq v_C \geq 2V_P$. The constraints on v_X and v_Y can be written as the following:

$$v_X - v_Y \leq -v_C$$

$$v_X - v_Y \leq v_C - 2V_P$$

$$v_Y - v_X \leq v_C - 2V_P$$

$$v_Y - v_X \leq -v_C$$

These can be combined as $|v_X - v_Y| \leq \min(-v_C, v_C - 2V_P)$. Therefore, the channel resistance $R_{XY} = (v_X - v_Y)/i_{XY}$ can be written as the following:

$$R_{XY} = \frac{1}{k(v_C/2 - V_P)}, \quad 0 \geq v_C \geq 2V_P \quad \text{and} \quad |v_X - v_Y| \leq \min(-v_C, v_C - 2V_P) \qquad (3.28)$$

Senani [22] reported that in the circuit using BFW10 as M1 with pinch-off voltage of −4 V, the range of linearity got extended to ± 1 V from ± 0.1 V. Thus, the circuit realizes a floating VCR with an extended range of linearity with respect to the voltage across the resistance. However, the resistance value is dependent on device parameters I_{DSS} and V_P.

Fort [26] reported a MOSFET-based resistor as shown in Figure 3.5, with compensation to reduce the variations occurring due to the device parameters and temperature. A current i_{PTAT} is used to generate the compensation voltage v_C based on a second order approximation of variation in mobility of a MOS resistor due to change in temperature. The current i_{PTAT} is generated from a current source such that it is proportional to the absolute temperature *T*. This current is received by a voltage generation module,

consisting of NMOS transistors M1, M3 and M5 with matched threshold voltage V_T and two matched PMOS transistors M2 and M4, which generates two outputs v_1 and v_2 such that

$$v_1 = V_T + k_1 T \text{ and } v_2 = k_2 T^2$$

These voltages are summed using op amps A1, A2, and A3 to provide the gate control voltage as the following:

$$v_{G6} = V_T + k_1 T + k_2 T^2 \tag{3.29}$$

Therefore, the resistance across the transistor M6 for small values of drain-source voltage can be given as

$$R_X = 1/k(v_{G6} - V_{T6}) \tag{3.30}$$

With the threshold voltage of M6 being matched to V_T, the resistance can be written as

$$R_X = 1/k(k_1 T + k_2 T^2) \tag{3.31}$$

Values of k_1 and k_2 are selected to compensate for variation in μ with temperature and the value of resistance is stabilized with respect to temperature variation. The circuit does not provide a floating VCR and does not compensate for variation in the resistance values due to change in v_X.

Clarke [27] proposed a set of four VCR circuits using two matched JFETs and an op amp to realize a grounded resistor whose resistance value is compensated against variations in device parameters using negative feedback. To illustrate the operation, one of the circuits is shown in Figure 3.6. It consists of an op amp A1 and two matched n-channel JFETs M1 and M2 working in the triode region. For the feedback through A1 and M1 to be negative, the drain and source terminals of M1 should be as shown in the figure and therefore $v_{REF} \geq 0$, $i_1 > 0$, and $v_C < 0$. The feedback loop through A1 and M1 maintains the inverting terminal of op amp A1 at ground. The current i_1 is controlled by voltage v_C and can be given as

$$i_1 = -v_C / R_1 \tag{3.32}$$

The voltage source v_{REF} is selected to keep M1 in the triode region. Assuming that v_{REF} is very small and that the gate voltage v_G gets controlled through the feedback loop for maintaining the current i_1 through M1, we get

$$i_1 = k_1(v_G - V_{P1} - v_{REF}/2)v_{REF}, \quad 0 \geq v_G \geq V_{P1} \text{ and } 0 \geq v_G - v_{REF} \geq V_{P1} \tag{3.33}$$

From (3.32) and (3.33), we get

$$-v_C / R_1 = k_1(v_G - V_{P1} - v_{REF}/2)v_{REF}, \quad 0 \geq v_G \geq V_{P1} \text{ and } v_G - V_{P1} \geq v_{REF} \geq v_G \tag{3.34}$$

From this equation, we get the value of v_G as the following:

$$v_G = \frac{-v_C}{k_1 R_1 v_{REF}} + V_{P1} + \frac{v_{REF}}{2} \tag{3.35}$$

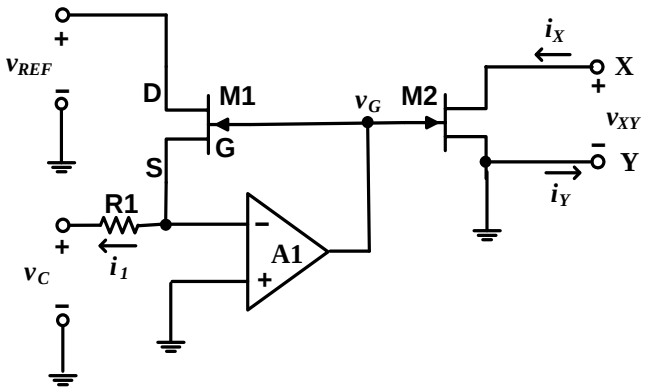


Figure 3.6: VCR circuit as proposed by Clarke [27].

The voltage v_G is also applied as the gate voltage of M2. Assuming M2 to be in the triode region, the current i_X flowing through M2 can be given as

$$i_X = k_2(v_G - V_{P2} - v_X/2)v_X, \quad 0 \geq v_G \geq V_{P2} \text{ and } 0 \geq v_G - v_X \geq V_{P2} \tag{3.36}$$

and $i_Y = i_X$. This equation using the expression for v_G in (3.35) can be rewritten as

$$i_X = \left[k_2 \left(\frac{-v_C}{k_1 R_1 v_{REF}} + V_{P1} + \frac{v_{REF}}{2} - V_{P2} - \frac{v_X}{2} \right) \right] v_X \tag{3.37}$$

Therefore, the resistance $R_X = v_X / i_X$ can be expressed as

$$R_X = \left[k_2 \left(\frac{-v_C}{k_1 R_1 v_{REF}} + V_{P1} - V_{P2} + \frac{v_{REF} - v_X}{2} \right) \right]^{-1} \tag{3.38}$$

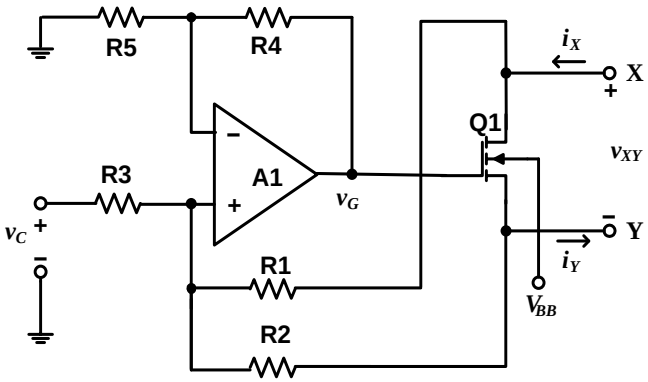
For VCR operation, v_{REF} can be kept constant and $-v_C$ can be applied as a control voltage. Assuming M1 and M2 to be matched pair of transistors, i.e. $k_1 = k_2 = k$ and $V_{P1} = V_{P2} = V_P$, the resistance $R_X = v_X / i_X$ can be expressed as

$$R_X = \left[\left(-\frac{v_C}{R_1 v_{REF}} + k_2 (v_{REF} - v_X)/2 \right) \right]^{-1} \tag{3.39}$$

Assuming v_{REF} and v_X to be small, the resistance R_X can be given approximately as the following:

$$R_X = \frac{v_{REF}}{-v_C} R_1 \tag{3.40}$$

The most important feature of the circuit is that if the two JFETs are matched and are operating in the triode region, the resistance R_X does not depend on the device parameters I_{DSS} and V_P. Another feature of the circuit is that it can be used as a resistance mirror, because R_X is proportional to R_1. However, it does not provide compensation to increase the range of linearity and does not realize a floating resistor.



$$R_1 = R_2 = R_3 \qquad R_5 = 2\,R_4$$

Figure 3.7: MOSFET-based floating VCR circuit with SD-bootstrapped gate and fixed-bias substrate.

3.4 Proposed VCR circuits

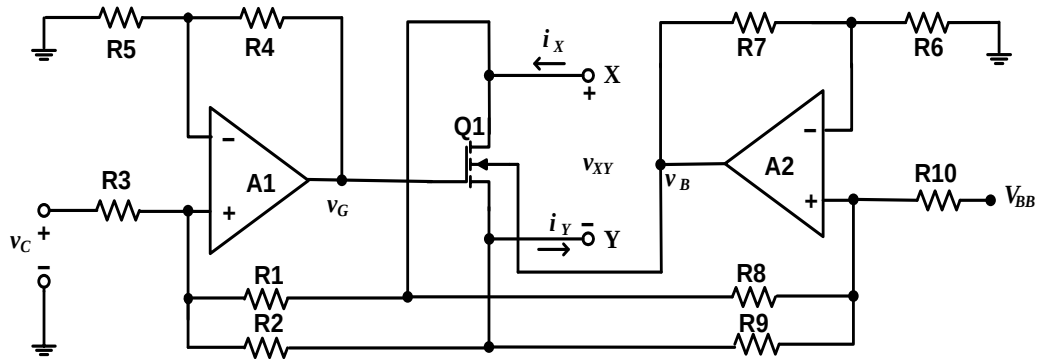
The VCR circuit proposed by Senani [22] and shown in Figure 3.4 can be realized using a MOSFET as shown in Figure 3.7. In a MOSFET-based circuit, the substrate-channel junction should remain reverse biased despite variations in the voltages at the source and drain terminals. The circuit in the figure uses a fixed substrate voltage V_B. It has to be lower than the lowest possible voltage at the X and Y terminals. Assuming that the source-substrate voltage does not change the channel resistance, analysis of the circuit operation is similar to that of the JFET-based circuit. The corresponding equations using MOSFET related parameters are as the following:

$$v_G = (v_C + v_X + v_Y)/2 \tag{3.41}$$

$$i_X = k(v_C/2 - V_T)(v_X - v_Y) \tag{3.42}$$

$$R_{XY} = \frac{1}{k(v_C/2 - V_T)}, \quad v_C \geq 2V_T \quad \text{and} \quad |v_X - v_Y| \leq v_C - 2V_T \tag{3.43}$$

Addition of the mean of the source and drain terminal voltages to the external control voltage to obtain the gate voltage for reducing the dependence of the channel resistance on source-drain voltage to realize a floating linear resistor can be considered as "SD-bootstrapped" gate. Variation in v_X and v_Y may dynamically change the role of X and Y terminals as source and drain, causing a variation in the substrate-source voltage which is likely to cause channel modulation and hence result in a nonlinear channel resistance. To reduce the channel modulation, mean value of v_X and v_Y may be added on a fixed negative voltage V_{BB} to generate the substrate bias as shown in Figure 3.8. In this circuit, $v_B = V_{BB} + (v_X + v_Y)/2$ and it can be considered as having "SD-bootstrapped" substrate in addition to having SD-bootstrapped gate.



$$R_1 = R_2 = R_3 \qquad R_6 = R_7 \qquad R_8 = R_9 = 2R_{10} \qquad R_5 = 2R_4$$

Figure 3.8: MOSFET-based floating VCR with SD-bootstrapped gate and SD-bootstrapped substrate.

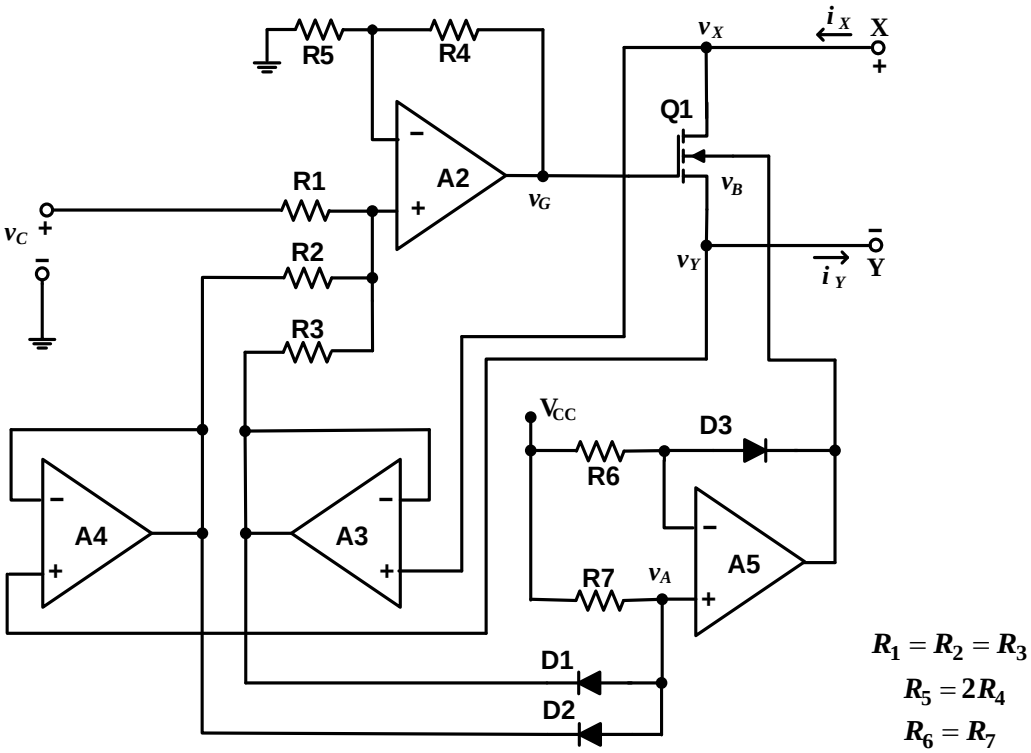


Figure 3.9: MOSFET-based floating VCR with SD-bootstrapped gate and S-bootstrapped substrate.

The effect of channel modulation can be minimized by connecting the substrate to the source. In a floating VCR, either of the X and Y terminals can act as source, therefore the source terminal needs to be detected for providing the source voltage to the substrate. This can be considered as "S-bootstrapped" substrate. Figure 3.9 shows the circuit with SD-bootstrapped gate and S-bootstrapped substrate. In this circuit, v_X and v_Y are buffered to ensure $i_X \approx i_Y$. The resistance R_7 connected to V_{CC} ensures that either D_1 or D_2 conducts.

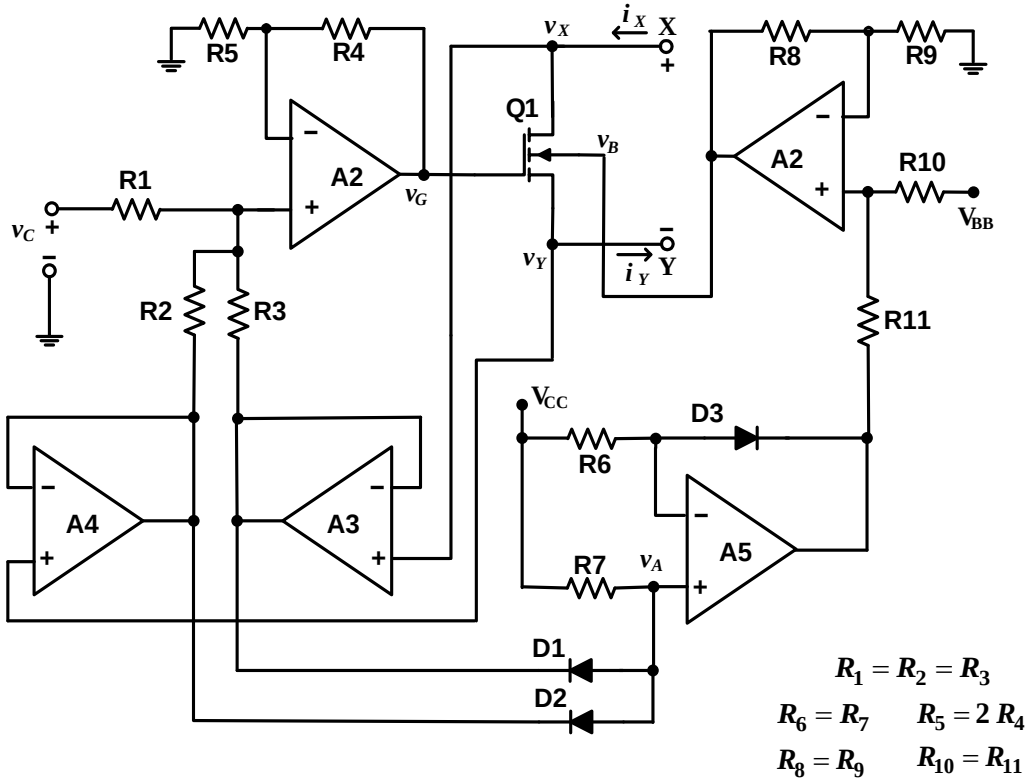


Figure 3.10: MOSFET-based floating VCR with SD-bootstrapped gate and S-bootstrapped-bias substrate.

If $v_X < v_Y$, then D_1 conducts and $v_A = v_X + v_{D1}$ else D_2 conducts and $v_A = v_Y + v_{D2}$. Thus $v_A = \min(v_X + v_{D1}, v_Y + v_{D2})$. Op amp A5 provides a unity buffer for v_A with a compensation for the diode drop. Assuming $v_{D1} \approx v_{D2} \approx v_{D3}$, output of op amp A5 provides $v_B = \min(v_X, v_Y)$. For maintaining a significant reverse bias at substrate-channel junction, the source voltage should be superimposed on a negative bias V_{BB}. Figure 3.10 shows the circuit using MOSFET with SD-bootstrapped gate and S-bootstrapped substrate with a fixed negative bias V_{BB}. In this circuit, $v_B = V_{BB} + \min(v_X, v_Y)$ and it can be considered as a circuit with "S-bootstrapped-bias" substrate.

The VCR circuit proposed by Clarke [27] and shown in Figure 3.6 uses a matched pair of JFETs to stabilize the resistance value against variation in device parameters. This can be considered as a "self-tracking circuit". Its realization using a matched pair of MOSFETs is shown in Figure 3.11. Since this circuit realizes a grounded resistance and is meant for small values of v_X, its substrate is provided a fixed negative bias V_{BB}.

Tiwari [25] investigated a circuit using two matched transistors and feedback to realize a floating linear VCR whose resistance value is independent of the device parameters. The circuit can be realized using JFETs or MOSFETs. In this circuit, the gate voltage is obtained by superimposing the drain and source voltages on the control voltage to realize a floating linear resistor and to eliminate the nonlinearity occurring due to the quadratic term in

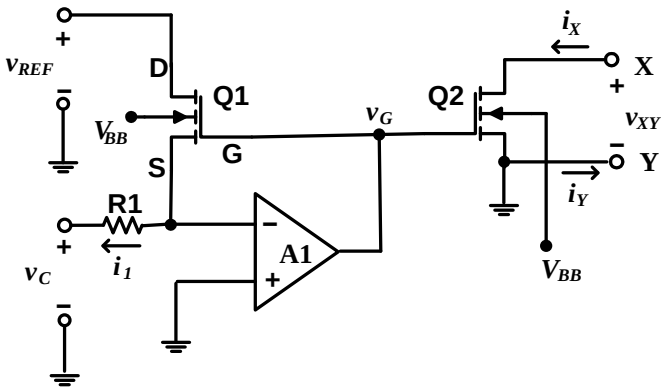


Figure 3.11: Matched-pair MOSFET-based grounded VCR with self-tracking and fixed-bias substrate.

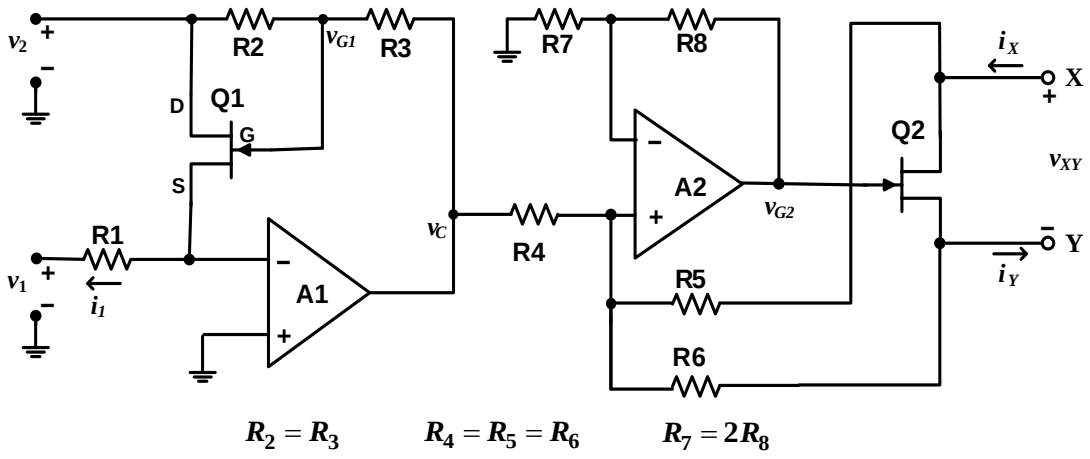


Figure 3.12: Matched-pair JFET-based floating VCR circuit with SD-bootstrapped gate, fixed-bias substrate and self-tracking.

the drain current as in the "bootstrapped-gate voltage" circuit reported by Senani [22]. The control voltage is derived using a feedback arrangement and matched pair of transistors as in the "self-tracking circuit" by Clarke [27] for eliminating the effect of variation in device parameters.

The proposed "bootstrapped-gate self-tracking" circuit using matched-pair JFET is shown in Figure 3.12. The n-channel JFETs Q1 and Q2 are matched transistors. Q2 serves as a floating resistor with terminals X and Y. The two transistors are assumed to be operating in the triode region. The control voltage v_C is generated through the negative feedback loop consisting of A1 and Q1 which maintains the inverting input terminal of A1 at ground. For loop feedback to be negative, the drain and source terminals of Q1 must be as shown in the figure, and therefore $v_2 \geq 0$. The external input v_1 has to be negative and the current i_1 through Q1 is given as

$$i_1 = -v_1 / R_1 \tag{3.44}$$

The gate terminals of both the transistors are obtained by summing half of the respective drain and source voltages on v_C. The gate voltage of Q1 be given as

$$v_{G1} = (v_C + v_2)/2 \tag{3.45}$$

and the gate voltage of Q2 is given as

$$v_{G2} = (v_C + v_X + v_Y)/2 \tag{3.46}$$

The resistances R_5 and R_6 are selected to be large enough to not cause any loading on the terminals X and Y. In this circuit the gate bootstrapping has been used to make the channel resistance dependent only on the control voltage v_C. The channel resistance of Q1 is controlled by v_1, v_2, and R_1, and it is independent of the device parameters. As the transistors are matched, the channel resistance of Q2 tracks that of Q1.

Assuming that the voltage v_2 is such that Q1 operates in the triode region, the current i_1 is given as

$$i_1 = k_1[(v_{G1} - V_{P1})v_2 - {v_2}^2/2], \quad 0 \geq v_{G1} \geq V_{P1} \text{ and } v_{G1} - v_2 \geq V_{P1} \tag{3.47}$$

Using (3.44), (3.45) and (3.47), the value of control voltage v_C comes out to be

$$v_C = 2\left[\frac{-v_1}{k_1 R_1 v_2} + V_{P1}\right], \quad 0 \leq v_2 \leq v_C - 2V_{P1} \tag{3.48}$$

Assuming v_X and v_Y to be such that Q2 is in the triode region, the current $i_X\,(= i_Y)$ through Q2 can be given as

$$\begin{aligned} i_X &= k_2[(v_{G2} - v_Y - V_{P2})(v_X - v_Y) - (v_X - v_Y)^2/2], \\ &\qquad 0 \geq v_{G2} - v_Y \geq V_{P2} \text{ and } 0 \geq v_{G2} - v_X \geq V_{P2} \end{aligned} \tag{3.49}$$

Using v_{G2} as given in (3.46), the current i_X can be rewritten as

$$i_X = k_2[(v_C/2 - V_{P2})(v_X - v_Y)], \quad 0 \geq v_C > 2V_{P2} \text{ and } |v_X - v_Y| \leq \min(-v_C, v_C - 2V_{P2}) \tag{3.50}$$

Using the control voltage v_C as given in (3.48), we can write

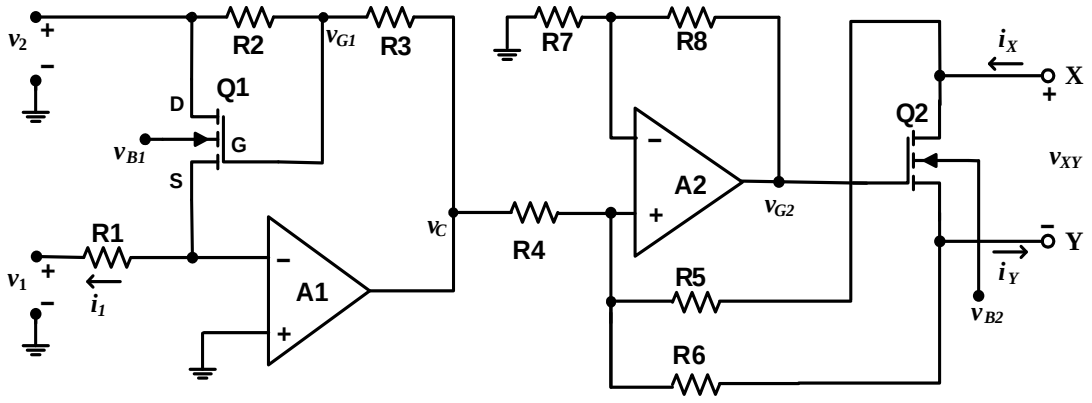
$$i_X = k_2\left[\frac{-v_1}{R_1 k_1 v_2} + V_{P1} - V_{P2}\right](v_X - v_Y) \tag{3.51}$$

For the matched pair of transistors Q1 and Q2, $k_1 = k_2 = k$ and $V_{P1} = V_{P2} = V_P$. Therefore, we can rewrite (3.51) as the following:

$$i_X = (-v_1/v_2 R_1)(v_X - v_Y), \quad 0 \geq v_C > 2V_P \text{ and } |v_X - v_Y| \leq \min(-v_C, v_C - 2V_P) \tag{3.52}$$

Therefore the circuit serves as a floating linear VCR with $R_{XY} = (v_X - v_Y)/i_X$ and the resistance value along with the constraints on the voltages is given as the following:

$$R_{XY} = \frac{v_2}{-v_1} R_1, \quad 0 \geq v_C > 2V_P \text{ and } |v_X - v_Y| \leq \min(-v_C, v_C - 2V_P) \tag{3.53}$$



$$R_2 = R_3 \qquad R_4 = R_5 = R_6 \qquad R_7 = 2R_8$$

Figure 3.13: Matched-pair MOSFET-based floating VCR circuit with SD-bootstrapped gate, fixed-bias substrate, and self-tracking.

The control can be exercised by a combination of v_1, v_2, and R_1, with the constraints on their values so that $v_C = 2\left[V_P - v_1/(kR_1v_2)\right]$ satisfies the condition $0 \geq v_C > 2V_P$ over the range of values of the device parameters V_P and k.

The proposed SD-bootstrapped gate, fixed-bias substrate, and self-tracking circuit can also be realized using a matched-pair of MOSFETs. The circuit using matched n-channel MOSFET pair is shown in Figure 3.13. It uses fixed substrate voltages, selected to keep the substrate-channel junctions reverse biased. The resistances R_5 and R_6 are kept large so that $i_Y \approx i_X$. Assuming that change in the source and drain voltages with reference to the substrate voltage do not result in channel modulation, analysis of the circuit operation is similar to that of the matched-pair JFET based circuit. The corresponding equations using MOSFET related parameters are as the following:

$$v_{G1} = (v_C + v_2)/2 \tag{3.54}$$

$$i_1 = -v_1/R_1 \tag{3.55}$$

$$i_1 = k_1[(v_{G1} - V_{T1})v_2 - {v_2}^2/2], \quad v_{G1} \geq V_{T1} \text{ and } v_{G1} - v_2 \geq V_{T1} \tag{3.56}$$

$$v_C = 2\left[\frac{-v_1}{k_1R_1v_2} + V_{T1}\right], \quad 0 \leq v_2 \leq v_C - 2V_{T1} \tag{3.57}$$

$$v_{G2} = (v_C + v_X + v_Y)/2 \tag{3.58}$$

$$i_X = k_2\left[\frac{-v_1}{R_1k_1v_2} + V_{T1} - V_{T2}\right](v_X - v_Y) \tag{3.59}$$

For matched pair of transistors, $k_1 = k_2 = k$ and $V_{T1} = V_{T2} = V_T$. Therefore, we can rewrite (3.59) as the following:

$$i_X = (-v_1/v_2R_1)(v_X - v_Y) \tag{3.60}$$

The constraints for triode region operation of Q2 are given as $v_{G2} - v_Y \geq V_T$ and $v_{G2} - v_X \geq V_T$. This can be expressed, using the value of v_{G2} in (3.58), as $v_C > 2V_T$ and $|v_X - v_Y| \leq v_C - 2V_T$. Thus, for the circuits in Figure 3.12 and Figure 3.13, the drain-source resistance $R_{XY} = (v_X - v_Y)/i_X$ is given as

$$R_{XY} = \frac{v_2}{-v_1} R_1, \quad v_C > 2V_T \text{ and } |v_X - v_Y| \leq v_C - 2V_T \tag{3.61}$$

The control can be exercised by a combination of v_1, v_2, and R_1, with the constraints on their values so that $v_C = 2[V_T - v_1/(kR_1v_2)]$ satisfies the condition $v_C > 2V_T$ for full range of values of the device parameters V_T and k.

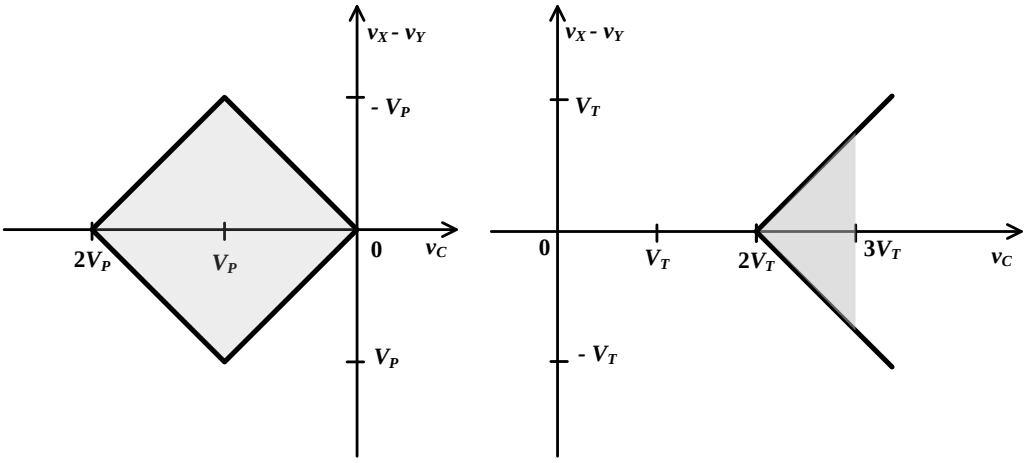
The constraints on v_C and $v_X - v_Y$ for linear operation of the circuit for the JFET based circuit as given in (3.53) and for the MOSFET-based circuit as given in (3.61) are shown graphically by the shaded region in Figure 3.14. It may be noted that although the resistance value is independent of the device parameters, range of $v_X - v_Y$ over which the resistance remains constant depends on v_C and consequently on the device parameters.

The circuits in Figure 3.12 and Figure 3.13 realize a floating linear VCR and the value of resistor R_{XY} is proportional to the resistance R_1 and the ratio of voltages v_2 and $-v_1$. Therefore, the resistance can be varied for realizing a resistor in proportion to v_2 or inversely proportional to $-v_1$. In addition, either circuit can be used to realize a floating resistance mirror by varying R_1.

In the description of the MOSFET-based circuit of Figure 3.13 and derivation of the equations, it is assumed that the substrate-channel junctions of Q1 and Q2 are reverse biased and the effects of channel modulation due to the variation in channel-substrate voltage is negligible. This can be realized by connecting the two substrate voltages v_{B1} and v_{B2} to a large negative voltage V_{BB} such that

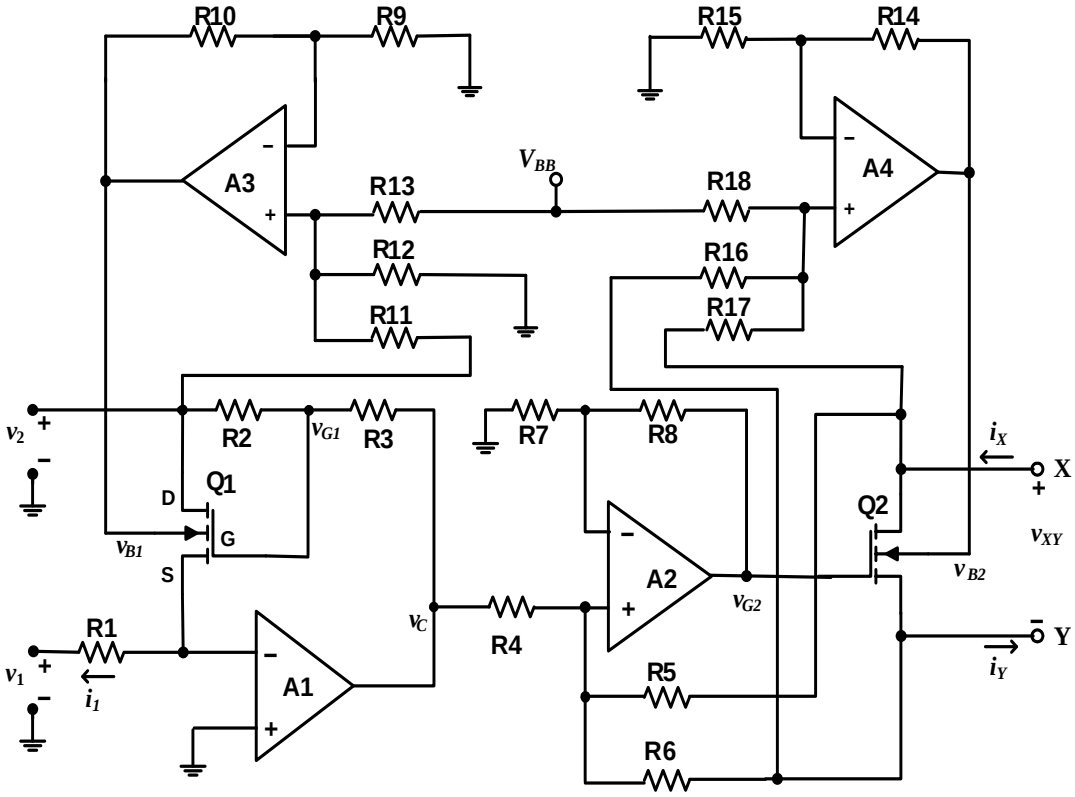
$$-V_{BB} >> \max(v_2, |v_X|, |v_Y|)$$

to ensure that variation in v_2, v_X, or v_Y do not introduce any significant modulation of the channels in the two transistors. It may be noted that larger negative V_{BB} results in larger channel resistance for a given control voltage. An alternate solution for reducing the channel modulation is to connect each substrate to a voltage which is sum of half of the corresponding drain and source voltages and a fixed negative voltage V_{BB}, as shown in Figure 3.15. In this circuit, the substrate voltages are given as



(a) JFET based circuit of Figure 3.12 (b) MOSFET-based circuit of Figure 3.13

Figure 3.14: Constraints on v_C and $v_{X-}v_Y$ for linear operation of the proposed floating VCR circuits with SD-bootstrapped gate and self-tracking.



$$R_2 = R_3 \qquad R_4 = R_5 = R_6 \qquad R_7 = 2R_8$$
$$R_9 = 2R_{10} \qquad R_{11} = R_{12} = R_{13} \qquad R_{14} = 2R_{15} \qquad R_{16} = R_{17} = R_{18}$$

Figure 3.15: Matched-pair MOSFET-based floating VCR with self-tracking, SD-bootstrapped gate, and SD-bootstrapped substrate.

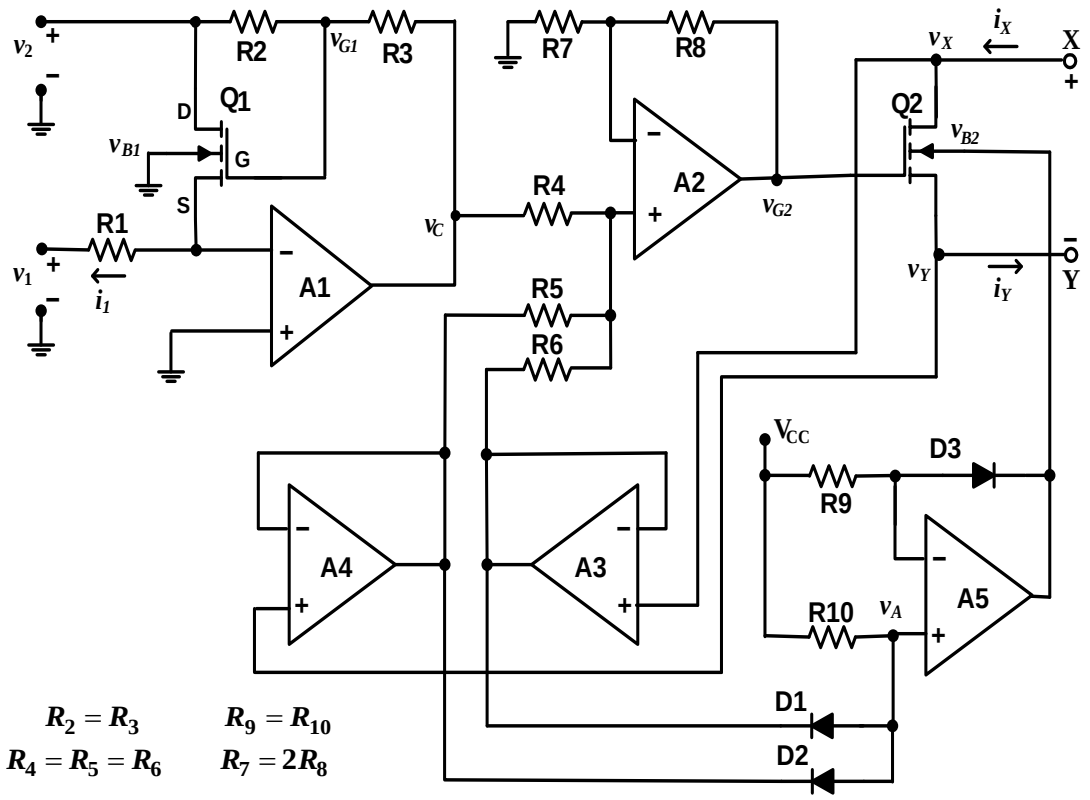


Figure 3.16: Matched-pair MOSFET-based floating VCR self-tracking, SD- bootstrapped gate, and S-bootstrapped substrate.

$$v_{B1} = V_{BB} + v_2/2 \tag{3.62}$$

$$v_{B2} = V_{BB} + (v_X + v_Y)/2 \tag{3.63}$$

This circuit can be called as having "SD-bootstrapped" substrate as in Figure 3.8. The voltage V_{BB} is selected to ensure that the substrate-channel junction remains reverse biased. The conditions of $v_{BS} < 0$ and $v_{BD} < 0$ are met for Q1 because $v_2 > 0$ and $V_{BB} < 0$. For Q2, the conditions $v_{BY} < 0$ and $v_{BX} < 0$ result in the conditions $V_{BB} + (v_X + v_Y)/2 - v_X < 0$ and $V_{BB} + (v_X + v_Y)/2 - v_Y < 0$.These can be simplified as $|v_X - v_Y| \le -2V_{BB}$.

The most common solution to minimize the channel modulation is to connect the substrate to the source of MOSFET. In a floating VCR, either of the X and Y terminals can act as source, and therefore the source terminal needs to be detected for providing the source voltage to the substrate. This can be considered as "S-bootstrapped" substrate as in Figure 3.8. In this circuit, $v_{B1} = 0$ and $v_{B2} = \min(v_X, v_Y)$ and therefore $v_{BS2} = 0$. Figure 3.16 shows matched-pair MOSFET-based self-tracking circuit with SD-bootstrapped gate and S-bootstrapped substrate. For maintaining a significant reverse bias at substrate-channel junction, the source voltage is superimposed on a large negative voltage V_{BB}. Figure 3.17

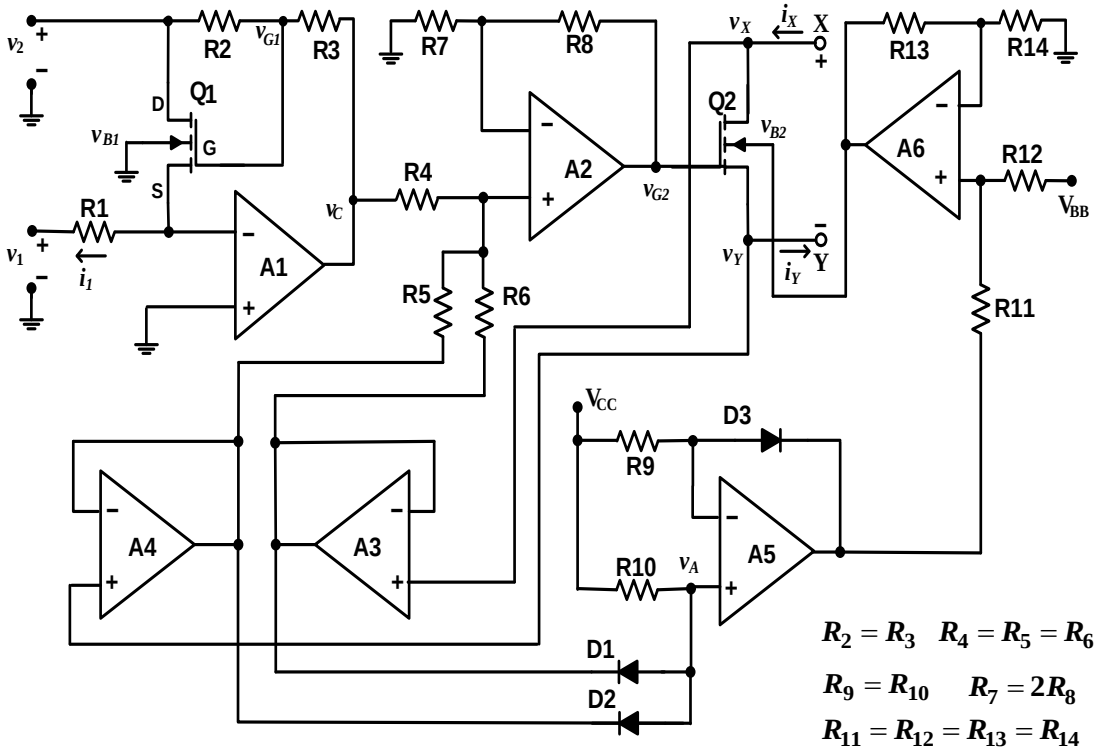


Figure 3.17: Matched-pair MOSFET-based floating VCR with self-tracking, SD-bootstrapped-gate, and S-bootstrapped-bias substrate.

shows matched-pair MOSFET-based self-tracking circuit with SD-bootstrapped gate and S-bootstrapped-bias substrate. In this circuit, $v_{B1} = 0$ and $v_{B2} = V_{BB} + \min(v_X, v_Y)$ and therefore $v_{BS2} = V_{BB}$.

3.5 Simulation results for VCR circuits using JFET

Circuit simulation was carried out to study the operation of JFET-based VCR circuits for examining the linearity and effect of variation in device parameters on the value of controlled resistance. The simulations were carried out for the following three circuits:

i) Grounded VCR using a JFET,
ii) JFET-based floating VCR circuit with SD-bootstrapped gate as shown in Figure 3.4,
iii) JFET-based floating VCR circuit with SD-bootstrapped gate and self-tracking as shown in Figure 3.12.

A description of the simulation is given below and the results are presented in the following subsections.

For investigating the operation of the proposed VCR circuit, we need a matched-pair of JFETs. For this purpose, we have used U441 from Siliconix. It is an IC with two matched n-channel JFETs [32]. For this device, the relationship between drain-source voltage and drain current may be considered to be linear for drain-source voltage of up to ± 0.1 V. Some

of the device parameters, specifically relevant for using the device as a VCR, are given in Table 3.1. The parameters may vary from piece-to-piece and are temperature dependent. V_P has a typical value of −3.5 V with device-to-device spread from −1 to −6 V, while I_{DSS} has a typical value of 15 mA with a spread from 6 to 30 mA. The device-to-device spread in values of V_P and I_{DSS} correspond to a spread in $R_{DS,ON}$ by a factor of 6 and 5, respectively. It is seen that temperature variation of ±10 ºC has relatively insignificant effect.

Simulation using "LTspice IV" was carried out using the model for JFET on U441 available in [33]. Parameters related to the device simulation are as the following: transconductance coefficient BETA, threshold voltage VTO, and channel modulation parameter LAMBDA. BETA is calculated as the following:

$$\text{BETA} = I_{DSS} / V_P^2 \tag{3.64}$$

For these calculations, three values of I_{DSS} were used: $I_{DSS\min}$ = 6 mA, $I_{DSS_{typ}}$ = 15 mA, and $I_{DSS\max}$ = 30 mA. Three values of V_P were used as VTO values: $V_{P\min}$ = −1.0 V, $V_{P_{typ}}$ = −3.5 V, and $V_{P\max}$ = −6.0 V. The default value of LAMBDA in the simulator is zero, and it was set as 0.012 [33] to simulate effect of mild channel modulation. The temperature coefficients for VTO and BETA are VTOTC and BETATCE with values of −1.7 mV/℃ and −1.7 mA/V^2℃, respectively, given in Table 3.1.

3.5.1 Simulation results for grounded VCR using a JFET

Simulation was used to obtain the drain characteristics for v_{DS} variation from −0.5 V to 2 V and different combinations of the following values of V_P, I_{DSS}, and v_{GS}:

V_P : −1.0, −3.5, and −6.0 V

I_{DSS} : 6, 15, and 30 mA

v_{GS} : 0, −0.5, and −1 V

The results of simulation are shown in Figure 3.18 as $i_D - v_{DS}$ plots are for (a) I_{DSS} = 3.0 mA and three values of V_P and (b) V_P = −2.0 V and three values of I_{DSS}, both for three values of v_{GS}. The plots show that V_P and I_{DSS} have a large effect on the drain characteristics.

For using JFET as a VCR, the terminal marked as D and S in Figure 3.1 are considered as the terminals X and Y, respectively, of the VCR. The control voltage v_C is applied as the gate voltage. Table 3.2 shows the channel resistance R_{XY} for different combinations of V_P and I_{DSS} and three v_C values of 0, −0.5, and −1 V. To avoid computational difficulties associated with v_X = 0, the simulation reported for this voltage

Table 3.1: JFET parameters of U441 for use as a VCR [32].

Parameter	Min.	Typ.	Max.	Test conditions
Device-dependence of V_P (from datasheet)	−1.0 V	−3.5 V	−6.0 V	T = 25 ˚C, I_{DS} = 1 nA, V_{DS} = 10 V
Device-dependence of I_{DSS} (from datasheet)	6 mA	15 mA	30 mA	T = 25 ˚C, V_{GS} = 0 V, V_{DS} = 10 V
Differential gate-source voltage (from datasheet)		6 mV	20 mV	I_D = 5 mA, V_{DG} = 10 V
Saturation drain current ratio (from datasheet)		0.97		V_{GS} = 0 V, V_{DS} = 10 V
Dependence of I_{DSS} on temperature (calc. using temperature coefficient of −0.17% / ºC, as obtained from the transfer characteristics in datasheet)	14.7 mA	15.0 mA	15.3 mA	I_{DSS} (25 ºC) = 15 mA, $T_{\min}$ = 15 ˚C, T_{typ} = 25 ˚C, $T_{\max}$ = 35 ˚C
Dependence of V_P on temperature (calc. using temperature coefficient of −1.7 mV / ºC, as obtained from the transfer characteristics in datasheet)	−3.48 V	−3.50 V	−3.52 V	$V_{GS,OFF}$ (25 ˚C) = 2.0 V, $T_{\min}$ = 15 ˚C, T_{typ} = 25 ˚C, $T_{\max}$ = 35 ˚C
Dependence of $R_{DS,ON}$ on V_P (calc. (3.4))	33 Ω	117 Ω	200 Ω	I_{DSS} = 15 mA, $V_{P\min}$ = −1.0 V, $V_{P typ}$ = −3.5 V, $V_{P\max}$ = −6.0 V, V_{DS} = 0.1 V, V_{GS} = 0 V
Dependence of R_{DS} on I_{DSS} (calc. (3.4))	58 Ω	117 Ω	292 Ω	V_P = −3.5 V, $I_{DSS\min}$ = 6 mA, $I_{DSS typ}$ = 15 mA, $I_{DSS\max}$ = 30 mA, V_{DS} = 0.1 V, V_{GS} = 0 V

was carried out with v_X = 10 mV. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.3). The values for $v_X \geq 0$ are shown in bold.

It is seen that the resistance can be controlled by changing v_C and the values obtained by simulation for small v_X are close to the corresponding calculated values. The resistance is highly nonlinear as exhibited by increase in its value with increase in v_X. It seen that for V_P = −3.5 V, I_{DSS} = 15 mA and v_C = −1 V, R_{XY} variation is 17.4% as v_X is varied over 0 to 1 V. Most importantly, piece-to-piece variations in device parameters may lead to a significant change in R_{XY}.

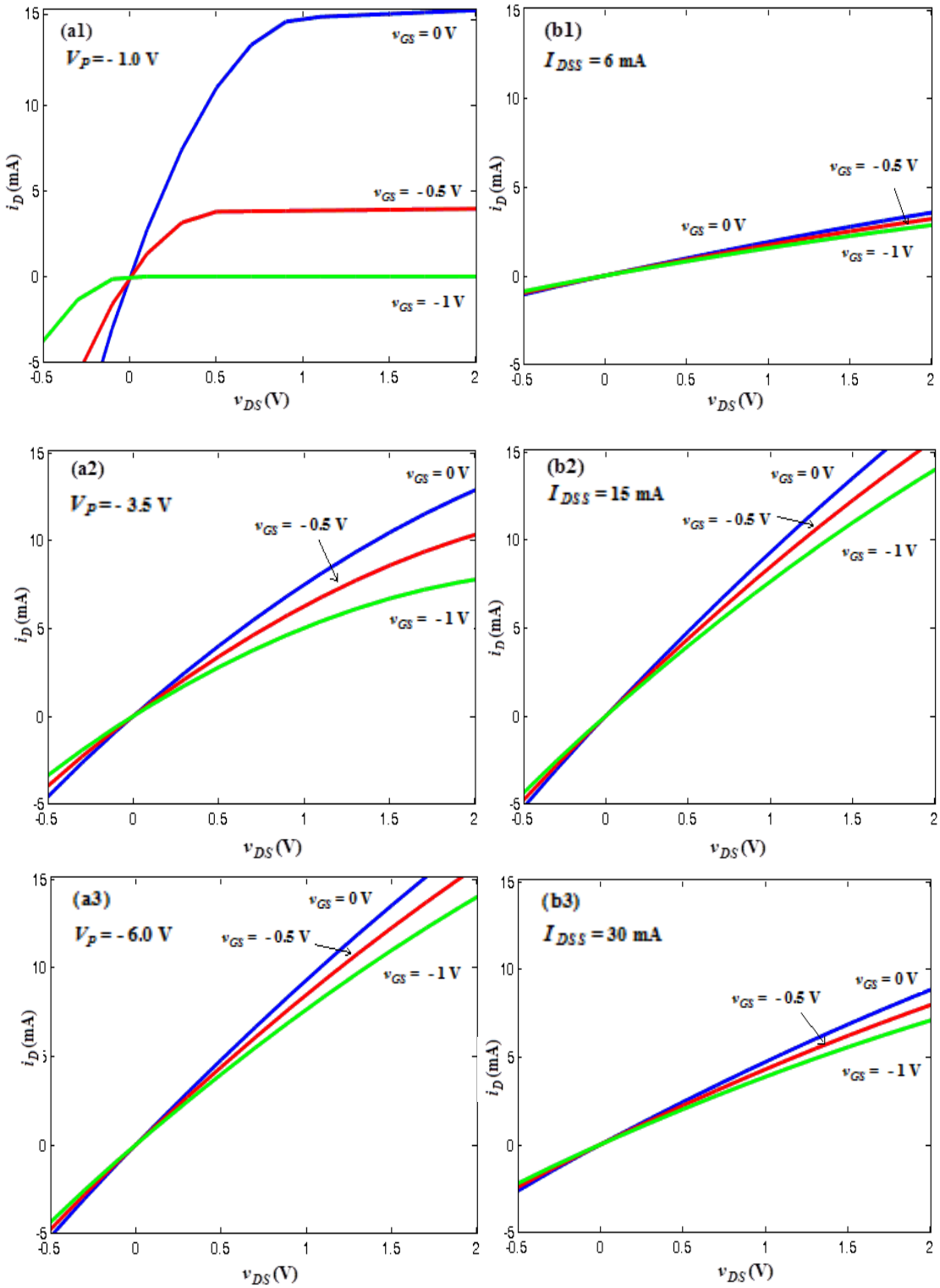


Figure 3.18: Drain characteristics of JFET on U441, obtained using the simulator LTspice IV for (a) I_{DSS} = 15 mA and three values of V_P ; (b) $V_P = -6$ V and three values of I_{DSS} .

Table 3.2: Simulation results for VCR operation of a single JFET device on U441 for observing the effect of V_P and I_{DSS} on R_{XY} at v_C of 0, −0.5, and −1 V.

a) v_C = 0 V

v_X (V)	R_{XY} (Ω)			
	V_P = −3.5 V, I_{DSS} = 15 mA ($R_{XY,CAL}$ = 116.6 Ω)	V_P = −6.0 V, I_{DSS} = 15 mA ($R_{XY,CAL}$ = 200.0 Ω)	V_P = −6.0 V, I_{DSS} = 6 mA ($R_{XY,CAL}$ = 500.0 Ω)	V_P = −6.0 V, I_{DSS} = 30 mA ($R_{XY,CAL}$ = 100.0 Ω)
−0.5	109.5	190.4	470.1	96.8
−0.2	115.1	197.4	489.9	100.2
−0.1	117.1	199.6	495.4	101.3
0.0	**118.8**	**201.9**	**501.3**	**102.4**
0.1	**120.4**	**202.9**	**503.7**	**102.9**
0.2	**121.8**	**204.0**	**506.4**	**103.5**
0.5	**126.3**	**207.5**	**515.0**	**105.2**
1.0	**134.7**	**213.7**	**530.6**	**108.4**
2.0	**156.7**	**228.3**	**567.0**	**115.8**

b) v_C = −0.5 V

v_X (V)	R_{XY} (Ω)			
	V_P = −3.5 V, I_{DSS} = 15 mA ($R_{XY,CAL}$ = 136.0 Ω)	V_P = −6.0 V, I_{DSS} = 15 mA ($R_{XY,CAL}$ = 219.0 Ω)	V_P = −6.0 V, I_{DSS} = 6 mA ($R_{XY,CAL}$ = 550.9 Ω)	V_P = −6.0 V, I_{DSS} = 30 mA ($R_{XY,CAL}$ = 108.9 Ω)
−0.5	126.7	207.5	515.0	105.2
−0.2	133.4	212.8	533.5	108.9
−0.1	135.9	217.4	539.8	110.2
0.0	**138.3**	**220.1**	**546.7**	**111.4**
0.1	**140.5**	**221.3**	**549.7**	**112.2**
0.2	**142.5**	**222.7**	**553.1**	**112.9**
0.5	**148.8**	**227.0**	**563.9**	**115.1**
1.0	**161.2**	**234.8**	**583.4**	**119.0**
2.0	**195.4**	**253.5**	**629.8**	**128.4**

c) v_C = −1 V

v_X (V)	R_{XY} (Ω)			
	V_P = −3.5 V, I_{DSS} = 15 mA ($R_{XY,CAL}$ = 163.3 Ω)	V_P = −6.0 V, I_{DSS} = 15 mA ($R_{XY,CAL}$ = 240.9 Ω)	V_P = −6.0 V, I_{DSS} = 6 mA ($R_{XY,CAL}$ = 606.1 Ω)	V_P = −6.0 V, I_{DSS} = 30 mA ($R_{XY,CAL}$ = 119.7 Ω)
−0.5	148.8	227.0	563.9	115.1
−0.2	158.7	235.7	585.6	119.4
−0.1	162.2	238.7	593.1	120.9
0.0	**166.2**	**241.9**	**601.2**	**122.6**
0.1	**168.8**	**243.5**	**605.0**	**123.3**
0.2	**171.7**	**245.2**	**609.4**	**124.2**
0.5	**181.5**	**250.7**	**623.0**	**126.9**
1.0	**201.0**	**260.7**	**648.0**	**132.0**
2.0	**259.8**	**284.9**	**708.2**	**144.2**

3.5.2 Simulation results for JFET-based floating VCR circuit with SD-bootstrapped gate

The circuit as shown in Figure 3.4 was simulated using a JFET from U441 (Vishay Siliconix) and op amp IC LT1366 (Linear Technology) with supply of ±15 V. LT1366 is dual op amp with rail-to-rail input and output voltages [34]. For simulation, v_Y was kept at 0 and only v_X was varied.

Table 3.3 shows the results of the circuit simulation to observe the effects of v_C and v_X on R_{XY}, with device parameters as $V_P = -3.5$ V and $I_{DSS} = 15$ mA. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.28). To avoid computational difficulties associated with v_X = 0.0 V, the simulation reported for this voltage was carried out with v_X = 10 mV as earlier in the case of JFET. The values corresponding to the condition for v_C and $v_X - v_Y$ as given in (3.28) and in Figure 3.14 are shown in bold. For small values of v_X and different values of v_C, the values of R_{XY} show a good match with the corresponding values of $R_{XY,CAL}$. For v_C = −3.0, −2.0, and −1.0 V, there is a decrease of approximately 2.8% in R_{XY} as v_X is changed from 0 to ±1 V. Thus the nonlinearity related error is within 2.8% for v_X variation over ±1 V.

Table 3.4 shows the simulation results to examine the effect of device parameters V_P and I_{DSS} on R_{XY}. The simulations were carried out for v_C = −1.0 V and the voltage v_X was varied from −1 to 1 V. With I_{DSS} = 15 mA, R_{XY} changes from 138.6 to 219.9 Ω as V_P changes from −3.5 to −6.0 V. With $V_P = -6.0$ V, R_{XY} changes from 70.0 to 342.7 Ω as I_{DSS} changes from 30 to 6 mA. Thus the results show that the device parameters have a large effect on R_{XY}.

3.5.3 Simulation results for matched-pair JFET-based floating VCR circuit with SD-bootstrapped gate and self-tracking

The VCR circuit as shown in Figure 3.10 was simulated using matched-pair JFET from U441 (Vishay Siliconix) and op amp IC LT1366 (Linear Technology). LT1366 is dual op amp with rail-to-rail input and output voltage ranges. The op amps are operated at ±15 V. For this simulation, v_Y was kept at 0 V and only v_X was varied.

Table 3.5 shows the results obtained to observe the effect of v_X and v_1 on R_{XY}. The simulations are carried with V_P = −3.5 V and I_{DSS} = 15 mA. Values of v_2 and R_1 are set as 1.0 V and 500 Ω, respectively. With this value of R_1, the v_1 values of −0.5 V, −1.0, −1.5, and −2 V result in i_1 of 1.0, 2.0, 3.0, and 4.0 mA, respectively. The corresponding values of $R_{XY,SET}$ are 1000.0, 500.0, 333.3, and 250.0 Ω, respectively and are referred to as $R_{XY,SET}$.

Table 3.3: Simulation results for JFET-based floating VCR circuit with SD-bootstrapped gate as shown in Figure 3.4, to observe effect of v_X and v_C on R_{XY}. Device parameters: $V_P = -3.5$ V & $I_{DSS} = 15$ mA.

v_X (V)	$v_C = -3.0$ V ($R_{XY,CAL}$ = 204.1 Ω)		$v_C = -2.0$ V ($R_{XY,CAL}$ = 163.3 Ω)		$v_C = -1.0$ V ($R_{XY,CAL}$ =136.1 Ω)		$v_C = 0.0$ V ($R_{XY,CAL}$ = 116.6 Ω)	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	**−2.49**	**195.4**	**−1.99**	**156.8**	−1.49	130.9	−1.17	21.9
−1.8	**−2.39**	**196.5**	**−1.89**	**157.6**	−1.39	131.7	−0.97	20.0
−1.6	**−2.29**	**197.6**	**−1.79**	**158.5**	−1.29	132.4	−0.80	22.0
−1.4	**−2.19**	**198.7**	**−1.69**	**159.4**	−1.19	133.2	−0.70	66.1
−1.2	**−2.09**	**199.8**	**−1.59**	**160.3**	−1.09	133.9	−0.59	112.1
−1.0	**−1.99**	**201.0**	**−1.49**	**161.2**	**−0.99**	**134.7**	−0.49	115.6
−0.8	**−1.89**	**202.2**	**−1.39**	**162.1**	**−0.89**	**135.4**	−0.39	116.4
−0.6	**−1.79**	**203.3**	**−1.29**	**163.1**	**−0.79**	**136.2**	−0.29	117.1
−0.4	**−1.69**	**204.5**	**−1.19**	**164.0**	**−0.69**	**137.0**	−0.19	117.7
−0.2	**−1.59**	**205.7**	**−1.09**	**164.9**	**−0.59**	**137.8**	−0.09	118.4
0.0	**−1.49**	**206.8**	**−1.00**	**165.8**	**−0.50**	**138.6**	**0.00**	**119.1**
0.2	**−1.39**	**205.7**	**−0.89**	**164.9**	**−0.39**	**137.8**	0.09	118.4
0.4	**−1.29**	**204.5**	**−0.79**	**164.0**	**−0.29**	**137.0**	0.19	117.7
0.6	**−1.19**	**203.3**	**−0.69**	**163.1**	**−0.19**	**136.2**	0.29	117.1
0.8	**−1.09**	**202.2**	**−0.59**	**162.1**	**−0.09**	**135.4**	0.39	116.4
1.0	**−1.00**	**201.0**	**−0.49**	**161.2**	**0.00**	**134.7**	0.49	115.7
1.2	**−0.89**	**199.8**	**−0.39**	**160.3**	0.09	133.9	0.59	115.1
1.4	**−0.79**	**198.7**	**−0.29**	**159.4**	0.19	133.2	0.69	115.4
1.6	**−0.69**	**197.6**	**−0.19**	**158.5**	0.29	132.4	0.79	119.4
1.8	**−0.59**	**196.5**	**−0.09**	**157.6**	0.39	131.7	0.82	122.8
2.0	**−0.49**	**195.4**	**−0.00**	**156.8**	0.49	130.9	0.82	124.6

Table 3.4: Simulation for JFET-based floating VCR circuit with SD-bootstrapped gate, as shown in Figure 3.4, for observing the effect of V_P and I_{DSS} on R_{XY}. $v_C = -1.0$ V.

v_X (V)	$V_P = -3.5$ V, I_{DSS} = 15 mA ($R_{XY,CAL}$ = 136.1 Ω)		$V_P = -6.0$ V, I_{DSS} = 15 mA ($R_{XY,CAL}$ = 218.2 Ω)		$V_P = -3.5$ V, I_{DSS} = 6 mA ($R_{XY,CAL}$ = 340.3 Ω)		$V_P = -3.5$ V, I_{DSS} = 30 mA ($R_{XY,CAL}$ = 68.0 Ω)	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−1.0	−0.99	134.7	−0.99	213.7	−0.99	332.9	−0.99	68.1
−0.8	−0.89	135.4	−0.89	214.9	−0.89	334.8	−0.89	68.4
−0.6	−0.79	136.2	−0.79	216.2	−0.79	336.8	−0.79	68.8
−0.4	−0.69	137.0	−0.69	217.4	−0.69	338.8	−0.69	69.2
−0.2	−0.59	137.8	−0.59	218.7	−0.59	340.8	−0.59	69.6
0.0	−0.50	138.6	−0.50	219.9	−0.50	342.7	−0.50	70.0
0.2	−0.39	137.8	−0.39	218.7	−0.39	340.8	−0.39	69.6
0.4	−0.29	137.0	−0.29	217.4	−0.29	338.8	−0.29	69.2
0.6	−0.19	136.2	−0.19	216.2	−0.19	336.8	−0.19	68.8
0.8	−0.09	135.4	−0.09	214.9	−0.09	334.8	−0.09	68.4
1.0	0.00	134.7	0.00	213.7	0.00	332.9	0.00	68.1

The voltage v_X was varied from −2 to 2 V. The value of $R_{XY,SET}$ obtained by simulation show a good match with the corresponding values of $R_{XY,CAL}$. The table shows that for the values of v_C corresponding to v_1 of −2.0, −1.5, −1.0, and −0.5 V, v_X of ±1 V is within the range of linear operation of the circuit. For v_1 of −2.0, −1.5, and −1.0 V, there is a decrease of approximately 2.5% in R_{XY} as v_X is changed from 0 to ±1 V. Corresponding decrease for v_1 = −0.5 V is approximately 4.3%.

Table 3.6 shows the effect of V_P and I_{DSS}, for v_1 = −1.5 V, v_2 = 1.0 V, R_1 = 500 Ω, i.e. i_1 = 3.0 mA. The voltage v_X was varied from −1 to 1 V. It is seen that as V_P and I_{DSS} are changed, corresponding changes occur in v_{G1}, v_C, and v_{G2} and R_{XY} remains constant for a given v_X. Thus the simulation results show that the self-tracking feature of the circuit stabilizes R_{XY} against variations due to device parameters and SD-bootstrapped gate results in a linear floating VCR. As the set values and simulated values show a very good match, the circuit can be used for realizing a floating resistance mirror.

3.6 Simulation results for VCR circuits using MOSFET

Circuit simulation was carried out to study the operation of MOSFET-based VCR circuits for examining the linearity and effect of variation in device parameters on the value of controlled resistance. The simulations were carried out for the following eight circuits:

i) Grounded VCR using a MOSFET,
ii) MOSFET-based floating VCR circuit with SD-bootstrapped gate and fixed-bias substrate as shown in Figure 3.7,
iii) MOSFET-based floating VCR circuit with SD-bootstrapped gate and SD-bootstrapped substrate as shown in Figure 3.8,
iv) MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped substrate as shown in Figure 3.9,
v) MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped-bias substrate as shown in Figure 3.10,
vi) MOSFET-based floating VCR circuit with SD-bootstrapped gate, fixed-bias substrate, and self-tracking, as shown in Figure 3.13,
vii) MOSFET-based floating VCR circuit with SD-bootstrapped gate, SD-bootstrapped substrate, and self-tracking as shown in Figure 3.15.
viii) MOSFET-based floating VCR circuit with SD-bootstrapped gate, S-bootstrapped substrate, and self-tracking as shown in Figure 3.16.

A description of the simulation is given below and the results for specific circuits are presented in the following subsections. As the results for simulations in (iv) and (v) showed

Table 3.5: Simulation results for the JFET-based floating VCR circuit with SD-bootstrapped gate and self-tracking, as in Figure 3.10 to observe the effects of v_1 and v_X on R_{XY}. Device parameters: $V_P = -3.5$ V & $I_{DSS} = 15$ mA. Circuit parameters: $v_2 = 1.0$ V, and $R_1 = 500.0\ \Omega$.

v_X (V)	$v_1 = -2.0$ V (Calculated: $i_1 = 4.0$ mA, $R_{XY,SET} = 250.0\ \Omega$. Observed: $v_C = -1.89$ V, $v_{G1} = -1.39$ V)		$v_1 = -1.5$ V (Calculated: $i_1 = 3.0$ mA, $R_{XY,SET} = 333.3\ \Omega$. Observed: $v_C = -2.29$ V, $v_{G1} = -1.79$ V)		$v_1 = -1.0$ V (Calculated: $i_1 = 2.0$ mA, $R_{XY,SET} = 500.0\ \Omega$. Observed: $v_C = -3.09$ V, $v_{G1} = -2.20$ V)		$v_1 = -0.5$ V (Calculated: $i_1 = 1.0$ mA, $R_{XY,SET} = 1000.0\ \Omega$. Observed: $v_C = -3.11$ V, $v_{G1} = -2.61$ V)	
	v_{G2} (V)	$R_{XY}(\Omega)$	v_{G2} (V)	$R_{XY}(\Omega)$	v_{G2} (V)	$R_{XY}(\Omega)$	v_{G2} (V)	$R_{XY}(\Omega)$
−2.0	−2.89	243.0	−3.29	324.0	−3.70	480.1	−4.11	799.8
−1.8	−2.79	244.4	−3.19	325.8	−3.60	487.1	−4.01	840.0
−1.6	−2.69	245.7	−3.09	327.7	−3.50	491.5	−3.91	881.8
−1.4	−2.59	247.2	−2.99	329.5	−3.40	494.3	−3.81	924.3
−1.2	−2.49	248.6	−2.89	331.4	−3.30	497.1	−3.71	965.1
−1.0	−2.39	249.9	−2.79	333.3	−3.20	499.9	−3.61	999.9
−0.8	−2.29	251.4	−2.69	335.3	−3.10	502.9	−3.51	1020.1
−0.6	−2.19	252.9	−2.59	337.2	−3.00	505.8	−3.41	1026.2
−0.4	−2.09	254.4	−2.49	339.2	−2.90	508.8	−3.31	1032.2
−0.2	−1.99	255.9	−2.39	341.2	−2.80	511.8	−3.21	1038.4
0.0	−1.89	257.3	−2.29	343.1	−2.70	514.7	−3.11	1044.2
0.2	−1.79	255.9	−2.19	341.2	−2.60	511.8	−3.01	1038.4
0.4	−1.69	254.4	−2.09	339.2	−2.50	508.8	−2.91	1032.2
0.6	−1.59	252.9	−1.99	337.2	−2.40	505.8	−2.81	1026.2
0.8	−1.49	251.4	−1.89	335.3	−2.30	502.9	−2.71	1020.1
1.0	−1.39	249.9	−1.79	333.3	−2.20	499.9	−2.61	999.9
1.2	−1.29	248.6	−1.69	331.4	−2.10	497.1	−2.51	965.1
1.4	−1.19	247.2	−1.59	329.5	−2.00	494.3	−2.41	924.3
1.6	−1.09	245.7	−1.49	327.7	−1.90	491.5	−2.31	881.8
1.8	−0.99	244.4	−1.39	325.8	−1.80	487.1	−2.21	840.0
2.0	−0.89	243.0	−1.29	324.0	−1.70	480.1	−2.11	799.8

Table 3.6: Simulation results for the JFET-based floating VCR circuit with SD-bootstrapped gate and self-tracking, as in Figure 3.10, for observing the effects of V_P and I_{DSS} on R_{XY}. Circuit parameters: $v_1 = -1.5$ V, $v_2 = 1.0$ V, and $R_1 = 500\ \Omega$ (i.e. $i_1 = 3.0$ mA and $R_{XY,SET} = 333.3\ \Omega$).

v_X (V)	$V_P = -3.5$ V, $I_{DSS} = 15$ mA (Observed: $v_C = -2.29$ V, $v_{G1} = -1.79$ V)		$V_P = -6.0$ V, $I_{DSS} = 15$ mA (Observed: $v_C = -2.48$ V, $v_{G1} = -1.98$ V)		$V_P = -3.5$ V, $I_{DSS} = 6$ mA (Observed: $v_C = -3.86$ V, $v_{G1} = -3.36$ V)		$V_P = -3.5$ V, $I_{DSS} = 30$ mA (Observed: $v_C = -2.90$ V, $v_{G1} = -2.40$ V)	
	v_{G2} (V)	$R_{XY}(\Omega)$	v_{G2} (V)	$R_{XY}(\Omega)$	v_{G2} (V)	$R_{XY}(\Omega)$	v_{G2} (V)	$R_{XY}(\Omega)$
−1.0	−2.79	333.3	−2.98	333.3	−1.00	333.3	−3.40	333.3
−0.8	−2.69	335.3	−2.88	335.3	−0.90	335.3	−3.30	335.3
−0.6	−2.59	337.2	−2.78	337.2	−0.80	337.2	−3.20	337.2
−0.4	−2.49	339.2	−2.68	339.2	−0.70	339.2	−3.10	339.2
−0.2	−2.39	341.2	−2.58	341.2	−0.60	341.2	−3.00	341.2
0.0	−2.29	343.1	−2.48	343.1	−0.50	343.1	−2.90	343.1
0.2	−2.19	341.2	−2.38	341.2	−0.40	341.2	−2.80	341.2
0.4	−2.09	339.2	−2.28	339.2	−0.30	339.2	−2.70	339.2
0.6	−1.99	337.2	−2.18	337.2	−0.20	337.2	−2.60	337.2
0.8	−1.89	335.3	−2.08	335.3	−0.10	335.3	−2.50	335.3
1.0	−1.79	333.3	−1.98	333.3	−0.00	333.3	−2.40	333.3

Table 3.7: MOSFET parameters of ALD1116/1106 for use as a VCR [35].

Parameter	Min.	Typ.	Max.	Test conditions
Device-dependence of V_T (datasheet)	0.4 V	0.7 V	1.0 V	T = 25 ˚C, I_{DS} = 1 µA, $V_{DS} = V_{GS}$
Device-dependence of R_{DS} (datasheet)	−	350 Ω	500 Ω	T = 25 ˚C, V_{GS} = 5 V, V_{DS} = 0.1 V
Device-dependence of k (calc. (3.10))	0.28 mA/V^2	0.52 mA/V^2	−	T = 25 ˚C, I_{DS} = 4.8 mA (typ.), 3.0 mA (min.) for $V_{DS} = V_{GS}$ = 5 V, V_T = 0.7 V
Dependence of V_T on temperature (calc. (3.14))	0.688 V	0.700 V	0.712 V	K = −1.2 mV/ ˚C, V_T (25 ˚C) = 0.7 V, $T_{\min}$ = 15 ˚C, T_{typ} = 15 ˚C, $T_{\max}$ = 35 ˚C
Dependence of k on temperature (calc. (3.11) & (3.13))	0.49 mA/V^2	0.52 mA/V^2	0.55 mA/V^2	m = 1.5, k (25 ˚C) = 0.52 mA/V^2, $T_{\min}$ = 15 ˚C, T_{typ} = 15 ˚C, $T_{\max}$ = 35 ˚C
Dependence of R_{DS} on V_T (calc. (3.19))	1201 Ω	1479 Ω	1923 Ω	k = 0.52 mA/V^2, $V_{T\min}$ = 0.4 V, $V_{T typ}$ = 0.7 V, $V_{T\max}$ = 1.0 V, V_{DS} = 0.1 V, V_{GS} = 2 V
Dependence of R_{DS} on k (calc. (3.19))	−	1479 Ω	2747 Ω	$k_{\min}$ = 0.28 mA/V^2, k_{typ} = 0.52 mA/V^2, V_T = 0.7 V, V_{DS} = 0.1 V, V_{GS} = 2 V

that the circuit with S-bootstrapped-bias substrate of Figure 3.10 has no specific advantage over the circuit with S-bootstrapped substrate of Figure 3.9, the self-tracking circuit with S-bootstrapped-bias substrate of Figure 3.17 was not tested by simulation.

ALD1106 and ALD1116 from Advanced Linear Devices are ICs with matched n-channel 4-terminal MOSFETs with their substrate terminals shorted together [35]. ALD1106 has four devices, while ALD1116 has two devices. The relationship between drain-source voltage and drain current may be considered to be linear for drain- source voltage of up to ± 0.16 V. Some of the device parameters, specifically relevant for using the device as a VCR, are given in Table 3.7. The parameters may vary from piece-to-piece and are temperature dependent. It is seen that V_T has a typical value of 0.7 V with a device-to-device spread of 0.4 − 1.0 V which can cause a spread in R_{DS} by a factor of 1.6 for v_{GS} = 2 V. The device-to-device variation in k can vary by a factor of 2 with a corresponding variation in R_{DS}. For a

change of ±10 ˚C from the operating temperature of 25 ˚C, V_T changes by about ±12 mV and k changes from 0.49 to 0.55 mA/V^2.

Simulation using "LTspice IV" was carried out using ALD1106. Most of the parameters for the device model are available in [36]. Parameters related to the device dimensions are as the following:

Channel length l = 7.8 µm, Channel width w = 0.138 mm,

Area of drain diffusion AD = 1.61 nm^2, Area of source diffusion AS = 6.03 nm^2,

Perimeter of drain PD = 0.478 mm, Perimeter of source PS = 0.478 mm.

The other parameters required for simulation are transconductance parameter KP, bulk threshold parameter GAMMA, surface potential PHI, zero-bias threshold voltage VTO, and channel-length modulation parameter LAMBDA. KP is calculated as the following:

$$\mathrm{KP} = kl/w \tag{3.65}$$

For these calculations, values of l and w were as given above. Two values of k were used: $k_{\min}$ = 0.28 mA/V^2 and k_{typ} = 0.52 mA/V^2. Three values of V_T were used VTO values: $V_{T\min}$ = 0.4 V, $V_{T\,typ}$ = 0.7 V, and $V_{T\max}$ = 1.0 V. Simulations were carried out at two values of v_{BS}. In accordance with the typical characteristics given in the device datasheet [35], $V_T(v_B)$ was taken as V_T, V_T + 0.7 V, and V_T + 1.5 V for V_{BB} of 0, −1.65, and −5 V, respectively. GAMMA is calculated as the following:

$$\mathrm{GAMMA} = \frac{V_T(v_{BS}) - V_T}{(|\mathrm{PHI}| + |v_{BS}|)^{1/2} - |\mathrm{PHI}|^{1/2}} \tag{3.66}$$

Value of PHI is not available for ALD1106, therefore it was taken as PHI = 0.7 V as given for ALD1101 in [36]. For V_{BB} of 0 and −5 V, GAMMA comes out to be 0 and 0.97, respectively. The default value of LAMBDA is zero and it was set as 0.01 to simulate effect of mild channel modulation.

3.6.1 Simulation results for grounded VCR using a MOSFET

Simulation was used to obtain the drain characteristics for v_{DS} variation from −0.6 to 2 V and different combinations of the following values of V_T, k, V_{BB}, and v_{GS}:

V_T : 0.4, 0.7, and 1.0 V

k : 0.52 and 0.28 mA/V^2

V_{BB} : 0 and −5 V

v_{GS} : 3, 3.5, and 4 V

The results of simulation are shown in Figure 3.19 as i_D versus v_{DS} plots. The plots are obtained for three values of V_T, two values of k, two values of V_{BB}, and three values of v_{GS}.

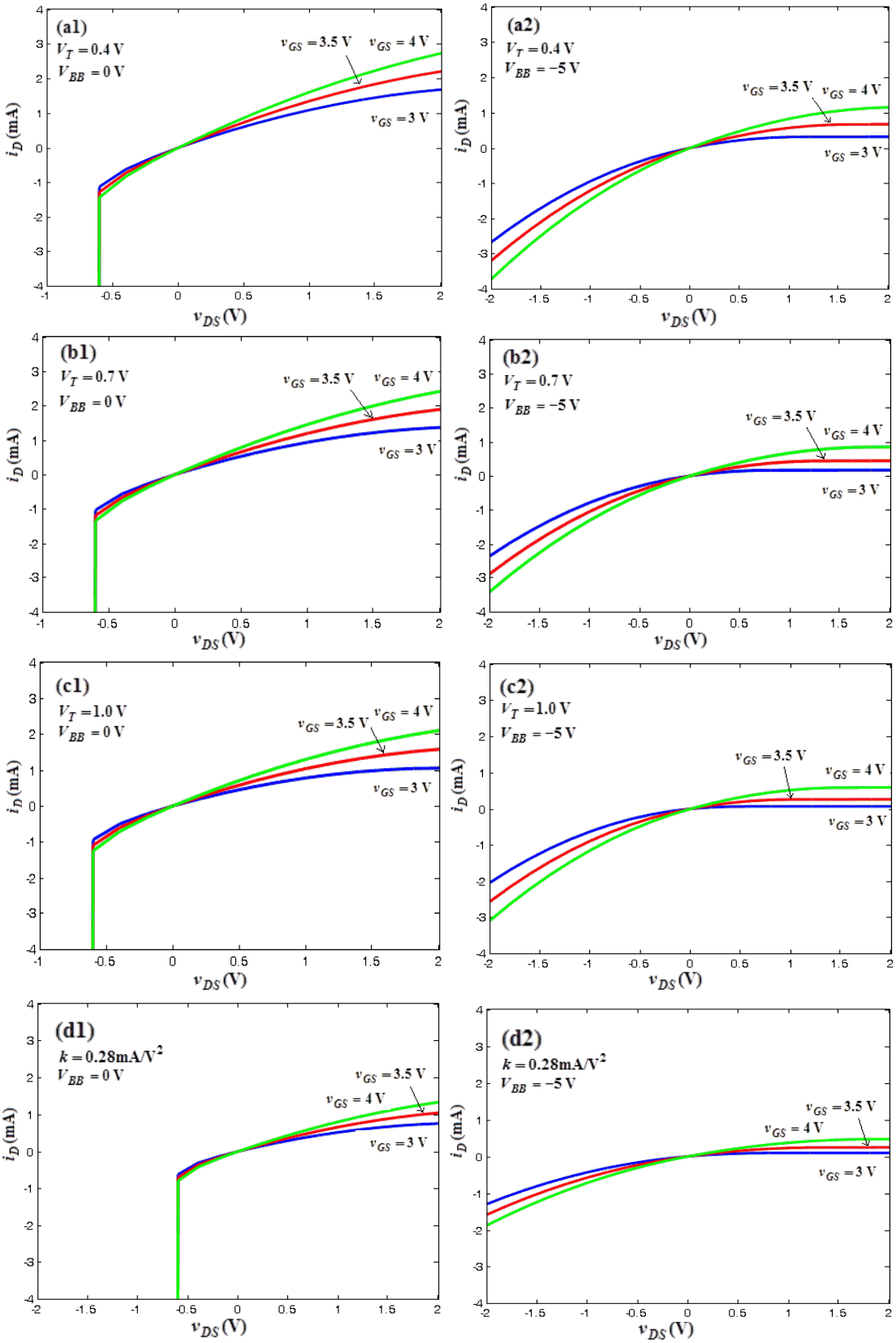


Figure 3.19: Drain characteristics of MOSFET on ALD1106, obtained using the simulator LTspice IV for (a), (b), and (c): k = 0.52 mA/V^2 and different values of V_T (d) V_T = 0.7 V and different values of k = 0.28 mA/V^2.

The plots show that device-to-device variation in V_T and k values can have a large effect on the characteristics. The plots also show that V_{BB} has a significant effect on i_D.

For using MOSFET as a VCR, the terminal marked as D and S in Figure 3.2 are considered as the terminals X and Y, respectively, of the VCR. The control voltage v_C is applied as the gate voltage. Table 3.8 shows the channel resistance R_{XY} for a single device on ALD1106 for different combinations of V_T and k and two values of V_{BB} = 0 and −5 V with three values of v_C = 3, 3.5, and 4 V. The simulation for v_X = 0 V was carried out with v_X = 10 mV to avoid computational difficulties associated with this voltage. The values for $v_C \geq v_X \geq 0$ V for V_{BB} = 0 V are shown in bold. It is seen that the resistance can be controlled by changing v_C and the values obtained by simulation for small v_X are close to the corresponding values as calculated using (3.19). The resistance is highly nonlinear as exhibited by increase in its value with increase in v_X. It seen that for V_T = 0.7 V and k = 0.52 mA/V^2, V_{BB} = −5 V and v_C = 4.0 V, R_{XY} varies by 27% as v_X is varied over 0 to 1 V. The simulation shows that variation in V_T and k leads to significant change in R_{XY}. It also shows a large effect of substrate voltage on R_{XY}.

3.6.2 Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and fixed-bias substrate

The floating VCR circuit with SD-bootstrapped gate and fixed-bias substrate is described in Section 3.4 and shown in Figure 3.7. It was simulated using MOSFET from ALD1106 (Advanced Linear Devices) and op amp IC LT1366 (Linear Technology) with supply of ±15 V. Simulation was carried out to observe the effect of device parameters, substrate voltage and control voltage on R_{XY}. Different combinations of the following values of V_T, k, V_{BB}, and v_C are used:

V_T : 0.4, 0.7, and 1.0 V

k : 0.52 and 0.28 mA/V^2

V_{BB} : −1.65 and −5 V

v_C : 6, 6.5, and 7 V

The voltage v_Y was kept at 0 and only v_X was varied from −2 to 2 V. Op amp supply voltage of ±15 V was used.

Table 3.9(a) shows the results of simulation to observe the effect of v_C and v_X on R_{XY} for V_{BB} = −1.65 V. Device parameters were selected as V_T = 0.7 V and k = 0.52 mA/V^2. To avoid computational difficulties associated with v_X = 0, the simulation reported for this

Table 3.8: Simulation results for a MOSFET on ALD1106 for observing the effect of V_T and k on R_{XY} at v_C of 3, 3.5, and 4 V and V_{BB} of 0 and −5 V.

(a1) v_C = 3 V, V_{BB} = 0 V

	R_{XY} (Ω)			
v_X (V)	V_T = 0.4 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ =739.6 Ω)	V_T = 0.7 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ =836.1 Ω)	V_T = 1.0 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ =961.5 Ω)	V_T = 0.7 V, k = 0.28 mA/V^2 ($R_{XY,CAL}$ =1322.7 Ω)
−0.6	533.5	581.6	639.2	964.0
−0.4	640.2	710.5	798.2	1287.7
−0.2	690.7	773.1	877.8	1401.9
0.0	**750.9**	**849.2**	**976.2**	**1539.1**
0.2	**778.0**	**884.1**	**1023.7**	**1602.5**
0.4	**808.8**	**924.4**	**1078.5**	**1675.5**
0.6	**842.3**	**968.7**	**1139.6**	**1755.8**
0.8	**878.9**	**1017.6**	**1208.5**	**1844.5**
1.0	**918.9**	**1072.1**	**1286.5**	**1943.1**

(a2) v_C = 3 V, V_{BB} = −5 V

	R_{XY} (Ω)			
v_X (V)	V_T = 0.4 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ =1923.1 Ω)	V_T = 0.7 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ =2747.2 Ω)	V_T = 1.0 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ =4807.7 Ω)	V_T = 0.7 V, k = 0.28 mA/V^2 ($R_{XY,CAL}$ = 5102.0 Ω)
−1.0	1066.9	1279.1	1596.6	2318.4
−0.8	1161.7	1417.2	1816.6	2568.6
−0.6	1273.8	1586.7	2103.6	2875.9
−0.4	1408.3	1800.0	2493.7	3262.6
−0.2	1572.8	2076.5	3054.9	3763.7
0.0	1786.7	2464.6	3971.4	4467.1
0.2	1953.5	2795.8	4915.5	5067.5
0.4	2167.3	3258.7	6564.6	5906.3
0.6	2434.8	3908.3	9460.9	7083.7
0.8	2779.2	4886.1	12589.5	8856.0
1.0	3239.3	6095.5	15705.7	11048.1

(b1) v_C = 3.5 V, V_{BB} = 0 V

	R_{XY} (Ω)			
v_X (V)	V_T = 0.4 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 620.3 Ω)	V_T = 0.7 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 686.8 Ω)	V_T = 1.0 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 769.2 Ω)	V_T = 0.7 V, k = 0.28 mA/V^2 ($R_{XY,CAL}$ = 1275.5 Ω)
−0.6	468.9	505.7	548.7	847.6
−0.4	549.0	600.6	662.1	1088.5
−0.2	586.6	644.9	716.2	1168.9
0.0	**629.7**	**697.2**	**781.1**	**1263.8**
0.2	**648.4**	**720.4**	**810.5**	**1305.7**
0.4	**669.4**	**746.6**	**844.0**	**1353.2**
0.6	**691.9**	**774.9**	**880.6**	**1404.6**
0.8	**716.1**	**805.6**	**920.7**	**1460.2**
1.0	**742.2**	**539.0**	**964.9**	**1520.7**

(b2) $v_C = 3.5$ V, $V_{BB} = -5$ V

v_X (V)	R_{XY} (Ω)			
	V_T = 0.4 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 1282.0 Ω)	V_T = 0.7 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 1602.6 Ω)	V_T = 1.0 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 2136.7 Ω)	V_T = 0.7 V, k = 0.28 mA/V^2 ($R_{XY,CAL}$ = 2976.2 Ω)
−1.0	835.9	960.7	1129.4	1741.3
−0.8	893.3	1037.1	1235.9	1879.7
−0.6	958.6	1125.7	1363.4	2040.4
−0.4	1033.4	1229.8	1518.4	2229.1
−0.2	1120.0	1353.9	1711.2	2453.9
0.0	1225.1	1509.9	1967.1	2736.6
0.2	1300.5	1626.7	2171.6	2948.5
0.4	1390.9	1771.7	2439.6	3211.2
0.6	1495.2	1945.7	2784.7	3526.6
0.8	1617.1	2158.7	3245.7	3912.6
1.0	1761.1	2425.1	3892.7	4395.5

(c1) $v_C = 4$ V, $V_{BB} = 0$ V

v_X (V)	R_{XY} (Ω)			
	V_T = 0.4 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 534.2 Ω)	V_T = 0.7 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 582.7 Ω)	V_T = 1.0 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 641.0 Ω)	V_T = 0.7 V, k = 0.28 mA/V^2 ($R_{XY,CAL}$ = 1082.2 Ω)
−0.6	418.3	447.3	480.6	756.4
−0.4	481.4	520.1	565.6	942.7
−0.2	509.7	553.2	604.8	1002.7
0.0	**542.1**	**591.4**	**650.7**	**1072.0**
0.2	**555.7**	**607.8**	**670.1**	**1101.7**
0.4	**570.9**	**626.2**	**693.3**	**1135.0**
0.6	**587.1**	**645.8**	**717.5**	**1170.5**
0.8	**604.2**	**666.7**	**743.7**	**1208.5**
1.0	**622.5**	**678.2**	**771.9**	**1249.1**

(c2) $v_C = 4$ V, $V_{BB} = -5$ V

v_X (V)	R_{XY} (Ω)			
	V_T = 0.4 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 961.5 Ω)	V_T = 0.7 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 1131.2 Ω)	V_T = 1.0 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 1373.6 Ω)	V_T = 0.7 V, k = 0.28 mA/V^2 ($R_{XY,CAL}$ = 2100.8 Ω)
−1.0	687.1	769.2	873.7	1394.2
−0.8	725.7	817.8	936.6	1482.2
−0.6	768.5	872.3	1008.5	1581.1
−0.4	816.2	933.9	1091.5	1692.8
−0.2	869.6	1004.3	1108.8	1820.4
0.0	932.1	1088.3	1307.3	1972.5
0.2	974.6	1147.1	1393.6	2079.1
0.4	1024.0	1216.5	1498.2	2204.9
0.6	1078.9	1295.3	1620.3	2347.7
0.8	1140.2	1385.3	1764.6	2510.9
1.0	1209.3	1489.3	1938.0	2699.4

voltage was carried out with v_X = 10 mV as earlier in Subsection 3.6.1. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.43).

The value of R_{XY} decreases by approximately 1% as v_X is varied from 0 to 1 V. It decreases by 17% as v_X is varied from 0 to −1 V. This behavior can be attributed to the fact that v_X polarity reversal results in change of the role of X and Y terminals and therefore change in substrate-source bias. For $v_X > 0$ and $v_Y = 0$, the terminal Y acts as the source and substrate-source bias remains constant. For $v_X < 0$ and $v_Y = 0$, the terminal X acts as the source and substrate-source bias changes with change in v_X and causes channel modulation. To minimize effect of the substrate-source bias in a floating resistance, the substrate terminal can be connected to a larger negative voltage. Table 3.9(b) shows R_{XY} values with same device parameters and V_{BB} = −5.0 V. The decrease in value of R_{XY} is approximately 1% as v_X is varied from 0 to 1 V and 17% as v_X is varied from 0 to −1 V. These results show that a larger negative voltage at the substrate increases the value of R_{XY} but does not stabilize it against the variation in v_X .Therefore use of the circuits with bootstrapped-substrate as shown in Figures 3.8, 3.9, and 3.10 needs to be examined, as presented later in Subsections 3.6.3, 3.6.4, and 3.6.5.

Table 3.10 shows the simulation results to examine the effect of V_T and k on R_{XY} for V_{BB} = −5 V. The control voltage v_C was set as 6.0 V and the voltage v_X was varied from −1 to 1 V with v_Y = 0. The values show that V_T and k have a significant effect on R_{XY}, and therefore use of the self-tracking circuits needs to be examined, as presented later in Subsections 3.6.6, 3.6.7, and 3.6.8.

3.6.3 Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and SD-bootstrapped substrate

Figure 3.8 shows the MOSFET-based floating VCR with SD-bootstrapped gate and SD-bootstrapped substrate.

Table 3.11 shows simulation results to observe the effect of v_1 and v_X on R_{XY} for bootstrapped substrate voltage v_B. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.43) for v_X = 0.01 V i.e. v_B = −5.0 V. For v_C = 6.0, 6.5, and 7.0 V, there is a decrease of approximately 10% in R_{XY} as v_X is changed from 0 to ±1 V. It may be noted that the SD-bootstrapped gate circuit with fixed-bias substrate resulted in a small decrease of 1% for v_X change from 0 to 1 V, but a large decrease of 17% for v_X change from 0 to -1 V. Thus SD-bootstrapped substrate results in a symmetrical behavior but the nonlinearity related error

Table 3.9: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate and fixed-bias substrate, as shown in Figure 3.7, to observe the effect of v_C and v_X on R_{XY}. Device parameters: V_T = 0.7 V and k = 0.52 mA/V^2.

(a) V_{BB} = −1.65 V

v_X (V)	v_C = 6.0 V ($R_{XY,CAL}$ = 1201.9 Ω)		v_C = 6.5 V ($R_{XY,CAL}$ = 1039.5 Ω)		v_C = 7 V ($R_{XY,CAL}$ = 915.7 Ω)	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	1.99	763.4	2.25	694.1	2.49	636.3
−1.8	2.09	802.1	2.35	726.0	2.59	663.2
−1.6	2.19	844.5	2.45	760.8	2.69	692.2
−1.4	2.29	887.3	2.55	195.5	2.79	720.9
−1.2	2.39	929.8	2.65	829.6	2.89	748.9
−1.0	2.49	972.4	2.75	863.6	2.99	767.7
−0.8	2.59	1015.6	2.85	897.7	3.09	804.3
−0.6	2.69	1059.6	2.95	932.2	3.19	832.1
−0.4	2.79	1104.8	3.05	967.2	3.29	860.1
−0.2	2.89	1151.5	3.15	1003.0	3.39	888.5
0.0	2.99	1199.6	3.25	1039.6	3.49	917.3
0.2	3.09	1197.3	3.35	1037.6	3.59	915.5
0.4	3.19	1194.9	3.45	1035.6	3.69	913.7
0.6	3.29	1192.5	3.55	1033.5	3.79	911.9
0.8	3.39	1190.2	3.65	1031.5	3.89	910.1
1.0	3.49	1187.8	3.75	1029.4	3.99	908.3
1.2	3.59	1185.5	3.85	1027.4	4.09	906.5
1.4	3.69	1183.1	3.95	1025.4	4.19	904.7
1.6	3.79	1180.8	4.05	1023.3	4.29	902.9
1.8	3.89	1178.5	4.15	1021.3	4.39	901.1
2.0	3.99	1176.2	4.25	1019.3	4.49	899.4

(b) V_{BB} = −5 V

v_X (V)	v_C = 6.0 V ($R_{XY,CAL}$ = 2403.8 Ω)		v_C = 6.5 V ($R_{XY,CAL}$ = 1831.5 Ω)		v_C = 7 V ($R_{XY,CAL}$ = 1479.3 Ω)	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	1.99	1533.8	2.25	1277.5	2.49	1094.5
−1.8	2.09	1600.8	2.35	1324.1	2.59	1128.9
−1.6	2.19	1671.8	2.45	1372.7	2.69	1164.4
−1.4	2.29	1747.2	2.55	1423.6	2.79	1201.2
−1.2	2.39	1827.4	2.65	1477.1	2.89	1239.4
−1.0	2.49	1913.2	2.75	1533.1	2.99	1279.1
−0.8	2.59	2004.9	2.85	1592.2	3.09	1320.4
−0.6	2.69	2103.6	2.95	1654.5	3.19	1363.4
−0.4	2.79	2209.8	3.05	1720.3	3.29	1408.3
−0.2	2.89	2324.7	3.15	1789.9	3.39	1455.2
0.0	2.99	2449.1	3.25	1863.6	3.49	1504.0
0.2	3.09	2444.5	3.35	1860.1	3.59	1501.2
0.4	3.19	2439.6	3.45	1856.4	3.69	1498.2
0.6	3.29	2434.7	3.55	1852.7	3.79	1495.2
0.8	3.39	2429.9	3.65	1849.0	3.89	1492.2
1.0	3.49	2425.1	3.75	1845.4	3.99	1489.3
1.2	3.59	2420.4	3.85	1841.7	4.09	1486.4
1.4	3.69	2415.6	3.95	1838.1	4.19	1483.4
1.6	3.79	2410.8	4.05	1834.5	4.29	1480.5
1.8	3.89	2396.9	4.15	1830.8	4.39	1477.6
2.0	3.99	2370.3	4.25	1827.3	4.49	1474.7

Table 3.10: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate and fixed-bias substrate, as shown in Figure 3.7, for observing the effect of V_T and k on R_{XY}. Circuit parameters: v_C = 6.0 V and V_{BB} = −5.0 V.

v_X (V)	V_T = 0.4 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ =1748.2 Ω)		V_T = 0.7 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 2403.8 Ω)		V_T = 1.0 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 3846.1 Ω)		V_T = 0.7 V, k = 0.28 mA/V^2 ($R_{XY,CAL}$ = 4464.3 Ω)	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−1.0	2.49	1474.6	2.49	1913.2	2.49	2723.1	2.49	3467.6
−0.8	2.59	1529.3	2.59	2004.9	2.59	2910.3	2.59	3634.0
−0.6	2.69	1586.7	2.69	2103.6	2.69	3119.8	2.69	3812.7
−0.4	2.79	1647.3	2.79	2209.8	2.79	3355.9	2.79	4005.4
−0.2	2.89	1711.2	2.89	2324.7	2.89	3624.2	2.89	4213.6
0.0	2.99	1778.5	2.99	2449.1	2.99	3931.3	2.99	4439.1
0.2	3.09	1775.2	3.09	2444.5	3.09	3923.9	3.09	4430.7
0.4	3.19	1771.7	3.19	2439.6	3.19	3916.1	3.19	4421.8
0.6	3.29	1768.1	3.29	2434.7	3.29	3908.3	3.29	4413.1
0.8	3.39	1764.6	3.39	2429.9	3.39	3900.5	3.39	4404.3
1.0	3.49	1761.1	3.49	2425.1	3.49	3892.7	3.49	4395.6

is increased, indicating a need for examining circuits with S-bootstrapped substrate as presented later in Subsections 3.6.4 and 3.6.5.

Table 3.12 shows the simulation results to examine the effect of device parameters V_P and I_{DSS} on R_{XY}. With k = 0.52 mA/V^2, R_{XY} changes from 1776.9 to 2446.1 Ω as V_T changes from 0.4 to 1.0 V. With V_P = 0.7 V, R_{XY} changes from 2446.1 to 4433.5 Ω as k changes from 0.28 to 0.52 mA/V^2. Thus the results show that device parameters have a significant effect on R_{XY}.

3.6.4 Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped substrate

The circuit is described in Section 3.4 and shown in Figure 3.9. Table 3.13 shows the simulation results to observe the effect of v_1 and v_X on R_{XY} for S-bootstrapped substrate. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.43) for v_X = 0.01 V i.e. v_B = 0.01 V. For v_C = 6.0, 6.5, and 7.0 V, the value of R_{XY} decreases by approximately 2.7% as v_X is changed from 0 to ±2 V. Figure 3.20 shows the simulation results plotted for MOSFET-based floating VCR circuit with SD-bootstrapped gate and (a) fixed bias substrate, (b) SD-bootstrapped substrate, and (c) S-bootstrapped substrate voltage. It can be seen that for S-bootstrapped substrate the value of R_{XY} shows a relatively much smaller variation with v_X. Figure 3.21 shows R_{XY} versus v_X plot for S-bootstrapped substrate on an enlarged scale. It shows a peak around v_X = 0 which cannot be explained from the circuit model.

Table 3.11: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate and SD-bootstrapped substrate, as shown in Figure 3.8, to observe the effect of v_C and v_X on R_{XY}. Device parameters: V_T = 0.7 V and k = 0.52 mA/V^2.

v_X (V)	v_C = 6.0 V ($R_{XY,CAL}$ = 2403.8 Ω)		v_C = 6.5 V ($R_{XY,CAL}$ = 1831.5 Ω)		v_C = 7 V ($R_{XY,CAL}$ = 1479.3 Ω)	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	1.99	1894.4	2.25	1518.1	2.49	1266.5
−1.8	2.09	1940.9	2.35	1548.5	2.59	1288.1
−1.6	2.19	1989.2	2.45	1579.7	2.69	1310.0
−1.4	2.29	2039.2	2.55	1611.7	2.79	1332.4
−1.2	2.39	2091.1	2.65	1644.7	2.89	1355.3
−1.0	2.49	2145.1	2.75	1678.6	2.99	1378.7
−0.8	2.59	2201.1	2.85	1713.5	3.09	1402.7
−0.6	2.69	2259.4	2.95	1749.4	3.19	1427.2
−0.4	2.79	2320.0	3.05	1786.4	3.29	1452.3
−0.2	2.89	2383.4	3.15	1824.5	3.39	1477.9
0.0	2.99	2446.1	3.25	1861.8	3.49	1502.9
0.2	3.09	2383.4	3.35	1824.5	3.59	1477.9
0.4	3.19	2320.0	3.45	1786.4	3.69	1452.3
0.6	3.29	2259.4	3.55	1749.4	3.79	1427.2
0.8	3.39	2201.1	3.65	1713.5	3.89	1402.7
1.0	3.49	2145.1	3.75	1678.6	3.99	1378.7
1.2	3.59	2091.1	3.85	1644.7	4.09	1355.3
1.4	3.69	2039.2	3.95	1611.7	4.19	1332.4
1.6	3.79	1989.2	4.05	1579.7	4.29	1310.0
1.8	3.89	1940.9	4.15	1548.5	4.39	1288.1
2.0	3.99	1894.4	4.25	1518.1	4.49	1266.5

Table 3.12: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate and SD-bootstrapped substrate, as shown in Figure 3.8, for observing the effect of V_T and k on R_{XY}. v_C = 6.0 V.

v_X (V)	V_T = 0.4 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ =1748.2 Ω)		V_T = 0.7 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 2403.8 Ω)		V_T = 1.0 V, k = 0.52 mA/V^2 ($R_{XY,CAL}$ = 3846.1 Ω)		V_T = 0.7 V, k = 0.28 mA/V^2 ($R_{XY,CAL}$ = 4464.3 Ω)	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−1.0	2.49	1608.6	2.49	2145.1	2.49	3218.3	2.49	3887.9
−0.8	2.59	1640.8	2.59	2201.1	2.59	3342.7	2.59	3989.5
−0.6	2.69	1673.8	2.69	2259.4	2.69	3475.3	2.69	4095.2
−0.4	2.79	1707.8	2.79	2320.0	2.79	3617.0	2.79	4205.3
−0.2	2.89	1742.8	2.89	2383.4	2.89	3768.8	2.89	4319.9
0.0	2.99	1776.9	2.99	2446.1	2.99	3923.4	2.99	4433.5
0.2	3.09	1742.8	3.09	2383.4	3.09	3768.8	3.09	4319.9
0.4	3.19	1707.8	3.19	2320.0	3.19	3617.0	3.19	4205.3
0.6	3.29	1673.8	3.29	2259.4	3.29	3475.3	3.29	4095.2
0.8	3.39	1640.8	3.39	2201.1	3.39	3342.7	3.39	3989.5
1.0	3.49	1608.6	3.49	2145.1	3.49	3218.3	3.49	3887.9

Table 3.13: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped substrate, as shown in Figure 3.9, to observe the effect of v_C and v_X on R_{XY}. Device parameters: V_T = 0.7 V and k = 0.52 mA/V^2.

v_X (V)	v_C = 6.0 V ($R_{XY,CAL}$ = 836.1 Ω)		v_C = 6.5 V ($R_{XY,CAL}$ = 754.1 Ω)		v_C = 7 V ($R_{XY,CAL}$ = 686.8 Ω)	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	1.99	830.7	2.25	749.3	2.49	682.4
−1.8	2.09	832.4	2.35	750.8	2.59	683.8
−1.6	2.19	834.0	2.45	752.3	2.69	685.1
−1.4	2.29	835.7	2.55	753.8	2.79	686.5
−1.2	2.39	837.3	2.65	755.3	2.89	687.8
−1.0	2.49	839.0	2.75	756.7	2.99	689.2
−0.8	2.59	840.6	2.85	758.2	3.09	690.5
−0.6	2.69	842.3	2.95	759.7	3.19	691.9
−0.4	2.79	844.0	3.05	761.3	3.29	693.3
−0.2	2.89	845.8	3.15	762.9	3.39	694.8
0.0	2.99	854.2	3.25	769.9	3.49	700.7
0.2	3.09	845.8	3.35	762.9	3.59	694.8
0.4	3.19	844.0	3.45	761.3	3.69	693.3
0.6	3.29	842.3	3.55	759.7	3.79	691.9
0.8	3.39	840.6	3.65	758.2	3.89	690.5
1.0	3.49	839.0	3.75	756.7	3.99	689.2
1.2	3.59	837.3	3.85	755.3	4.09	687.8
1.4	3.69	835.7	3.95	753.8	4.19	686.5
1.6	3.79	834.0	4.05	752.3	4.29	685.1
1.8	3.89	832.4	4.15	750.8	4.39	683.8
2.0	3.99	830.7	4.25	749.3	4.49	682.4

Ignoring this peaking, the variation in R_{XY} is 1.7% for v_X of ±1 V and 2.8% for v_X of ±2 V. Thus the simulation results show that S-bootstrapping of the substrate has helped in stabilizing the value of R_{XY} and the performance of this circuit is far better than that of SD-bootstrapping of the substrate. It is further seen that the nonlinearity related error is almost comparable to that of the SD-bootstrapped JFET circuit and the circuit operation is possible over a larger range of v_X .

3.6.5 Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped-bias substrate

The proposed circuit is shown in Figure 3.10. Table 3.14 shows the simulation results to observe the effect of v_1 and v_X on R_{XY} for S-bootstrapped substrate voltage superimposed on a fixed negative voltage V_{BB} = −5 V. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.43) for v_X = 0.01 V i.e. v_B = 0.01 V. For v_C = 6.0, 6.5, and 7.0 V, the value of R_{XY} decreases by approximately 1.7% as v_X is changed from 0 to ±1 V. On comparing simulation results of the circuits with S-bootstrapped substrate and S-bootstrapped-bias

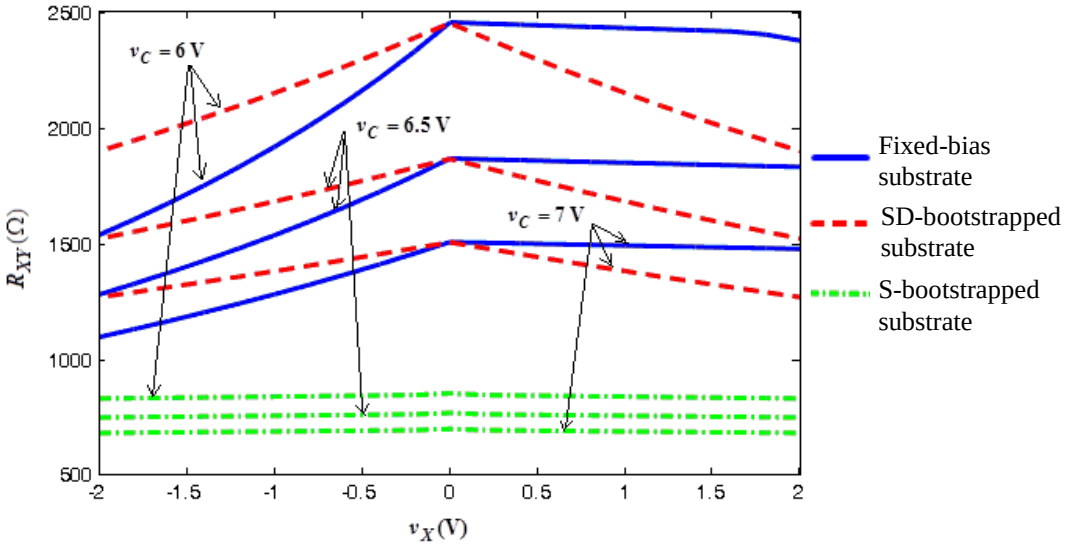


Figure 3.20: Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped-gate and (a) fixed-bias substrate, (b) SD-bootstrapped substrate, and (c) S-bootstrapped substrate.

Table 3.14: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped-bias substrate, as shown in Figure 3.10, to observe the effect of v_C and v_X on R_{XY}. Device parameters: V_T = 0.7 V and k = 0.52 mA/V^2. V_{BB} = −5 V.

v_X (V)	v_C = 6.0 V ($R_{XY,CAL}$ = 836.1 Ω)		v_C = 6.5 V ($R_{XY,CAL}$ = 754.1 Ω)		v_C = 7 V ($R_{XY,CAL}$ = 686.8 Ω)	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	1.99	2370.3	2.25	1827.3	2.49	1474.7
−1.8	2.09	2396.9	2.35	1830.8	2.59	1477.6
−1.6	2.19	2410.8	2.45	1834.4	2.69	1480.5
−1.4	2.29	2415.7	2.55	1838.1	2.79	1483.4
−1.2	2.39	2420.3	2.65	1841.7	2.89	1486.4
−1.0	2.49	2425.1	2.75	1845.3	2.99	1489.3
−0.8	2.59	2429.9	2.85	1849.0	3.09	1492.3
−0.6	2.69	2434.7	2.95	1852.7	3.19	1495.2
−0.4	2.79	2439.6	3.05	1856.4	3.29	1498.2
−0.2	2.89	2444.8	3.15	1860.3	3.39	1501.3
0.0	2.99	2465.9	3.25	1873.3	3.49	1510.4
0.2	3.09	2444.8	3.35	1860.3	3.59	1501.3
0.4	3.19	2439.6	3.45	1856.4	3.69	1498.2
0.6	3.29	2434.7	3.55	1852.7	3.79	1495.2
0.8	3.39	2429.9	3.65	1849.0	3.89	1492.3
1.0	3.49	2425.1	3.75	1845.3	3.99	1489.3
1.2	3.59	2420.3	3.85	1841.7	4.09	1486.4
1.4	3.69	2415.7	3.95	1838.1	4.19	1483.4
1.6	3.79	2410.8	4.05	1834.4	4.29	1480.5
1.8	3.89	2396.9	4.15	1830.8	4.39	1477.6
2.0	3.99	2370.3	4.25	1827.3	4.49	1474.7

substrate, it is seen that addition of the fixed negative bias on bootstrapped substrate increases the value of the resistance but does not decrease the nonlinearity related error.

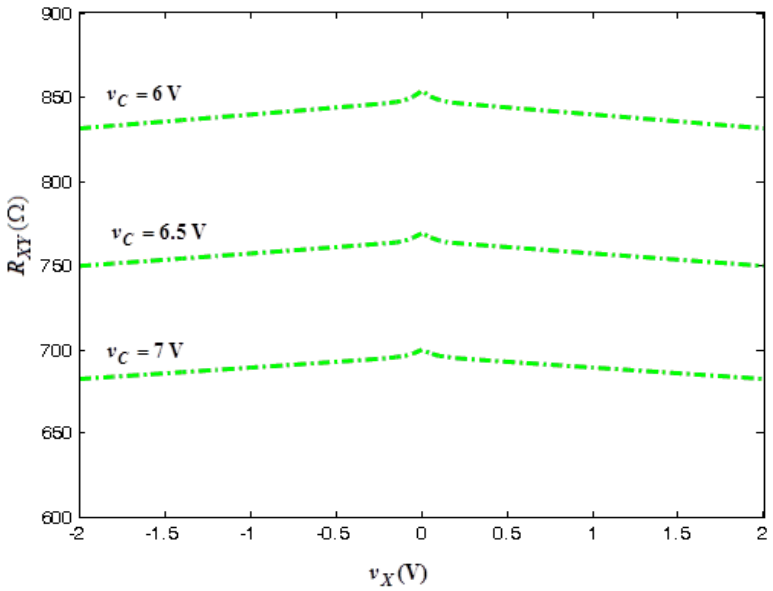


Figure 3.21: Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped substrate.

3.6.6 Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped gate, fixed-bias substrate, and self-tracking

The proposed circuit, as shown in Figure 3.13, was implemented using the matched MOSFET pair on ALD1106. Table 3.15 (a) shows the readings obtained to observe the effect of v_X and v_1 on R_{XY}. The simulations were carried with device parameters selected as V_T = 0.7 V and k = 0.52 mA/V^2. Circuit parameters are selected as v_2 = 1.0 V, R_1 = 1.0 kΩ, and V_{BB} = −1.65 V. For voltages v_1 = −0.5 V, −1.0, −1.5, and −2 V, it results in i_1 of 1.0, 2.0, 3.0, and 4.0 mA, respectively and the corresponding set values of R_{XY} as 1000.0, 500.0, 333.3, and 250.0 Ω, respectively. The voltage v_X was varied from −2 to 2 V. The linearity is not achieved in any of the cases for v_X > 0 V. The value of R_{XY} decreases by 1% as v_X is changed from 0 to 1 V and by 25% as v_X is changed from 0 to −1 V. Table 3.15 (b) shows the results with same parameters and V_{BB} = −5.0 V. The decrease in the value of R_{XY} is 1% for v_X changing from 0 to 1 V and 8% for v_X changing from 0 to −1 V. The results show that a more negative bias to the substrate results in the value of R_{XY} nearer to its set value, but nonlinearity related errors is not significantly decreased for v_X < 0 V.

Table 3.16 shows the results to observe the effect of device parameters for v_1 = −1 V, V_{BB} = −5 V and R_1 = 1.0 kΩ, i.e. i_1 = mA. The voltage v_X was varied from −1 to 1 V. The R_{XY} values for a given v_X are not affected by change in the device parameters k and V_T. Thus the results show that the self-tracking feature of the circuit is effective in stabilizing R_{XY} against variation the circuit parameters.

Table 3.15: Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped gate, fixed-bias substrate, and self-tracking, as shown in Figure 3.13, to observe the effect of v_1 and v_X on R_{XY}. Device parameters: V_T = 0.7 V and k = 0.52 mA/V^2. Circuit parameters: v_2 = 1.0 V and R_1 = 1.0 kΩ.

(a) V_{BB} = −1.65 V

v_X (V)	v_1 = −2.0 V (i_1 = 0.50 mA, $R_{XY,SET}$ = 500.0 Ω, v_C = 10.46 V, v_{G1} = 5.73 V)		v_1 = −1.5 V (i_1 = 0.67 mA, $R_{XY,SET}$ = 666.7 Ω, v_C = 8.54 V, v_{G1} = 4.77 V)		v_1 = −1.0 V (i_1 = 1.0 mA, $R_{XY,SET}$ = 1000.0 Ω, v_C = 6.60 V, v_{G1} = 3.80 V)		v_1 = −0.5 V (i_1 = 2.0 mA, $R_{XY,SET}$ = 2000.0 Ω, v_C = 4.68 V, v_{G1} = 2.84 V)	
	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)
−2.0	4.23	403.3	3.27	506.4	2.30	680.5	1.34	1036.7
−1.8	4.33	414.2	3.37	523.5	2.40	711.2	1.44	1108.5
−1.6	4.43	425.7	3.47	541.7	2.50	744.5	1.54	1190.2
−1.4	4.53	436.7	3.57	559.4	2.60	777.8	1.64	1275.9
−1.2	4.63	447.2	3.67	576.4	2.70	810.4	1.74	1364.3
−1.0	4.73	457.3	3.77	592.9	2.80	842.8	1.84	1456.6
−0.8	4.83	467.2	3.87	609.2	2.90	875.3	1.94	1554.1
−0.6	4.93	476.8	3.97	625.3	3.00	908.1	2.04	1657.8
−0.4	5.03	486.3	4.07	641.3	3.10	941.4	2.24	1769.1
−0.2	5.13	495.7	4.17	657.3	3.20	975.3	2.34	1889.4
0.0	5.23	504.9	4.27	673.3	3.30	1009.9	2.44	2019.9
0.2	5.33	503.9	4.37	672.0	3.40	1008.0	2.54	2016.0
0.4	5.43	502.9	4.47	670.7	3.50	1005.9	2.64	2012.0
0.6	5.53	501.9	4.57	669.3	3.60	1003.9	2.74	2008.0
0.8	5.63	500.9	4.67	668.0	3.70	1002.0	2.84	2004.0
1.0	5.73	500.0	4.77	666.7	3.80	1000.0	2.94	2000.1
1.2	5.83	499.0	4.87	665.3	3.90	998.0	3.04	1996.1
1.4	5.93	498.0	4.97	664.0	4.00	996.1	3.14	1992.2
1.6	6.03	497.0	5.07	662.7	4.10	994.1	3.24	1988.2
1.8	6.13	496.1	5.17	661.4	4.20	992.2	3.34	1984.3
2.0	6.23	495.1	5.27	660.1	4.30	990.2	3.44	1979.8

3.6.7 Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped gate, SD-bootstrapped substrate, and self-tracking

The need for bootstrapped voltage v_B arises as R_{XY} does not track R_1 for $v_X < 0$ V. Therefore, Figure 3.15 was implemented with SD-bootstrapped gate, SD-bootstrapped substrate,and self-tracking. Table 3.17 shows the simulation results with device parameters selected as V_T = 0.7 V and k = 0.52 mA/V^2. Circuit parameters are selected as V_{CC} = ±15 V, v_Y = 0 V, v_2 = 1.0 V, V_{BB} = −5 V, and R_1 = 1.0 kΩ. For different values of v_X and v_1, the values of R_{XY} show a good match with the corresponding set values $R_{XY,SET}$. For v_1 = −2.0 and −1.5 V, the value of R_{XY} decreases by approximately 4% as v_X is changed from 0 to ±1 V. For less negative values of v_1, v_C decreases and the range of v_X for linear operation of the circuit decreases. This behavior is in accordance with the relation as given earlier in (3.61) and shown in Figure 3.14. It may be noted that this circuit has a nonlinearity related error of

(b) V_{BB} = −5 V

v_X (V)	v_1 = −2.0 V (i_1 = 0.50 mA, $R_{XY,SET}$ = 500.0 Ω, v_C = 10.46 V, v_{G1} = 5.73 V)		v_1 = −1.5 V (i_1 = 0.67 mA, $R_{XY,SET}$ = 666.7 Ω, v_C = 8.54 V, v_{G1} = 4.77 V)		v_1 = −1.0 V (i_1 = 1.0 mA, $R_{XY,SET}$ = 1000.0 Ω, v_C = 6.60 V, v_{G1} = 3.80 V)		v_1 = −0.5 V (i_1 = 2.0 mA, $R_{XY,SET}$ = 2000.0 Ω, v_C = 4.68 V, v_{G1} = 2.84 V)	
	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)
−2.0	5.06	443.4	4.09	571.3	3.13	802.9	2.17	1350.5
−1.8	5.16	449.5	4.19	581.1	3.23	821.7	2.27	1402.5
−1.6	5.26	455.5	4.29	590.9	3.33	840.8	2.37	1457.1
−1.4	5.36	461.6	4.39	600.8	3.43	860.3	2.47	1514.4
−1.2	5.46	467.7	4.49	610.9	3.53	880.3	2.57	1574.7
−1.0	5.56	473.8	4.59	620.9	3.63	900.6	2.67	1638.4
−0.8	5.66	480.0	4.69	631.2	3.73	921.5	2.77	1705.8
−0.6	5.76	486.2	4.79	641.5	3.83	942.8	2.87	1777.3
−0.4	5.86	492.4	4.89	652.0	3.93	964.6	2.97	1853.1
−0.2	5.96	498.7	4.99	662.6	4.03	987.0	3.07	1933.8
0.0	6.06	504.9	5.09	673.3	4.13	1009.9	3.17	2019.9
0.2	6.16	504.0	5.19	670.0	4.23	1008.0	3.27	2016.0
0.4	6.26	502.9	5.29	670.6	4.33	1005.9	3.37	2012.0
0.6	6.36	501.9	5.39	669.3	4.43	1003.9	3.47	2008.0
0.8	6.46	501.0	5.49	668.0	4.53	1003.0	3.57	2004.0
1.0	6.56	500.0	5.59	666.7	4.63	1000.0	3.67	2000.0
1.2	6.66	499.0	5.69	665.3	4.73	998.0	3.77	1996.1
1.4	6.76	498.0	5.79	664.0	4.83	996.1	3.87	1992.2
1.6	6.86	497.0	5.89	662.7	4.93	994.1	3.97	1988.3
1.8	6.96	496.1	5.99	661.4	5.03	992.2	4.07	1984.3
2.0	7.06	495.1	6.09	660.1	5.13	990.2	4.17	1979.8

4% which is much lower than the non-tracking circuit. This can be attributed to the fact that the present circuit is using a larger v_C.

The simulation results from Table 3.18 show the effect of device parameters V_T and k for v_1 = −1 V and R_1 = 1.0 kΩ, i.e. i_1 = 1 mA and $R_{XY,SET}$ = 1.0 kΩ. The results show that self-tracking feature of the circuit is able to stabilize the resistance against parameter variations.

3.6.8 Simulation results for MOSFET-based floating VCR circuit with SD-bootstrapped gate, S-bootstrapped substrate, and self-tracking

The circuit is shown in Figure 3.16. Table 3.19 shows the simulation results with device parameters selected as V_T = 0.7 V and k = 0.52 mA/V^2. Circuit parameters are selected as v_2 = 1.0 V and R_1 = 1.0 kΩ. For different values of v_X and v_1, the values of R_{XY} show a good match with the corresponding set values $R_{XY,SET}$. For v_1 = −2.0, −1.5, and −1.0 V, there is a decrease of approximately 1.5% in R_{XY} as v_X is changed from 0 to ±1 V. The corresponding decrease for v_1 = −0.5 V is 2.5%.

Table 3.16: Simulation results for the MOSFET-based floating VCR circuit, as shown in Figure 3.11, for observing the effect of V_T and k on R_{XY}. Circuit parameters: $v_1 = -1.0$ V, $v_2 = 1.0$ V, $V_{BB} = -5.0$ V, and $R_1 = 1.0$ kΩ (i.e. $i_1 = 1.0$ mA and $R_{XY,SET} = 1000.0$ Ω).

v_X (V)	V_T = 0.4 V, k = 0.52 mA/V^2			V_T = 0.7 V, k = 0.52 mA/V^2			V_T = 1.0 V, k = 0.52 mA/V^2			V_T = 0.7 V, k = 0.28 mA/V^2		
	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)
−1.0	4.33	3.33	900.6	4.63	3.63	900.6	4.93	3.93	900.6	6.20	5.20	942.6
−0.8	4.33	3.43	921.5	4.63	3.73	921.5	4.93	4.03	921.5	6.20	5.30	955.9
−0.6	4.33	3.53	942.8	4.63	3.83	942.8	4.93	4.13	942.8	6.20	5.40	969.3
−0.4	4.33	3.63	964.6	4.63	3.93	964.6	4.93	4.23	964.6	6.20	5.50	982.7
−0.2	4.33	3.73	987.0	4.63	4.03	987.0	4.93	4.33	987.0	6.20	5.60	996.3
0.0	4.33	3.83	1009.9	4.63	4.13	1009.9	4.93	4.43	1009.9	6.20	5.70	1009.9
0.2	4.33	3.93	1008.0	4.63	4.23	1008.0	4.93	4.53	1008.0	6.20	5.80	1008.0
0.4	4.33	4.03	1005.9	4.63	4.33	1005.9	4.93	4.63	1005.9	6.20	5.90	1006.0
0.6	4.33	4.13	1003.9	4.63	4.43	1003.9	4.93	4.73	1003.9	6.20	6.00	1004.0
0.8	4.33	4.23	1003.0	4.63	4.53	1003.0	4.93	4.83	1003.0	6.20	6.10	1002.0
1.0	4.33	4.33	1000.0	4.63	4.63	1000.0	4.93	4.93	1000.0	6.20	6.20	1000.0

The simulation results from Table 3.20 show the effect of device parameters V_T and k for $v_1 = -1$ V and $R_1 = 1.0$ kΩ, i.e. $i_1 = 1$ mA and $R_{XY,SET} = 1.0$ kΩ. The results show that self-tracking feature of the circuit is able to stabilize the resistance against parameter variations.

Figure 3.22 shows the simulation results plotted for matched-pair MOSFET-based floating VCR circuits with self-tracking, SD-bootstrapped gate, and different types of substrate biasing: (a) fixed-bias substrate, (b) SD-bootstrapped substrate, and (c) S-bootstrapped substrate. It shows that the S-bootstrapped substrate results in the smallest change in R_{XY} with variation in v_X. As the earlier self-tracking circuits, this circuit was also found to stabilize R_{XY} against device parameter variations. Thus this circuit is able to stabilize R_{XY} and decrease nonlinearity related errors.

3.7 Test results for VCR circuits using JFET

Circuit implementation and testing is carried out to study the operation of the following three JFET-based VCR circuits:

i) Grounded VCR using a JFET,
ii) JFET-based floating VCR circuit with SD-bootstrapped gate as shown in Figure 3.4,
iii) JFET-based floating VCR circuit with SD-bootstrapped gate and self-tracking as shown in Figure 3.12.

Table 3.17: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate, SD-bootstrapped substrate, and self-tracking, as shown in Figure 3.15, to observe the effect of v_1 and v_X on R_{XY}. Device parameters: V_T = 0.7 V and k = 0.52 mA/V^2. Circuit parameters: v_2 = 1.0 V, and R_1 = 1.0 kΩ.

v_X (V)	$v_1 = -2.0$ V (i_1 = 0.50 mA, $R_{XY,SET}$ = 500.0 Ω, v_C = 10.46 V, v_{G1} = 5.73 V)		$v_1 = -1.5$ V (i_1 = 0.67 mA, $R_{XY,SET}$ = 666.7 Ω, v_C = 8.54 V, v_{G1} = 4.77 V)		$v_1 = -1.0$ V (i_1 = 1.0 mA, $R_{XY,SET}$ = 1000.0 Ω, v_C = 6.60 V, v_{G1} = 3.80 V)		$v_1 = -0.5$ V (i_1 = 2.0 mA, $R_{XY,SET}$ = 2000.0 Ω, v_C = 4.68 V, v_{G1} = 2.84 V)	
	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)
−2.0	4.96	481.5	3.99	636.2	3.03	937.3	2.06	1779.4
−1.8	5.06	485.2	4.09	642.2	3.13	949.5	2.16	1820.6
−1.6	5.16	488.8	4.19	648.2	3.23	961.8	2.26	1863.2
−1.4	5.26	492.5	4.29	654.3	3.33	974.4	2.36	1907.3
−1.2	5.36	496.3	4.39	660.5	3.43	987.1	2.46	1952.8
−1.0	5.46	500.0	4.49	666.7	3.53	1000.0	2.56	2000.0
−0.8	5.56	503.7	4.59	672.9	3.63	1013.1	2.66	2048.9
−0.6	5.66	507.5	4.69	679.2	3.73	1026.4	2.76	2099.7
−0.4	5.76	511.3	4.79	685.6	3.83	1039.9	2.86	2142.4
−0.2	5.86	515.1	4.89	691.9	3.93	1053.6	2.96	2207.0
0.0	5.96	518.8	4.99	698.1	4.03	1066.8	3.06	2260.9
0.2	6.06	515.1	5.09	691.9	4.13	1053.9	3.16	2207.0
0.4	6.16	511.3	5.19	685.6	4.23	1039.9	3.26	2142.4
0.6	6.26	507.5	5.29	679.2	4.33	1026.4	3.36	2099.7
0.8	6.36	503.7	5.39	672.9	4.43	1013.1	3.46	2048.9
1.0	6.46	500.0	5.49	666.7	4.53	1000.0	3.56	2000.1
1.2	6.56	496.3	5.59	660.5	4.63	987.1	3.66	1952.8
1.4	6.66	492.5	5.69	654.3	4.73	974.4	3.76	1907.3
1.6	6.76	488.8	5.79	648.2	4.83	961.8	3.86	1863.2
1.8	6.86	485.2	5.89	642.2	4.93	949.5	3.96	1820.6
2.0	6.96	481.5	5.99	636.2	5.03	937.3	4.06	1779.4

Table 3.18: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate, SD-bootstrapped substrate, and self-tracking, as shown in Figure 3.15, for observing the effect of V_T and k on R_{XY}. Circuit parameters: $v_1 = -1.0$ V, v_2 = 1.0 V, and R_1 = 1.0 kΩ (i.e. i_1 = 1.0 mA and $R_{XY,SET}$ = 1000.0 Ω).

v_X (V)	V_T = 0.4 V, k = 0.52 mA/V^2			V_T = 0.7 V, k = 0.52 mA/V^2			V_T = 1.0 V, k = 0.52 mA/V^2			V_T = 0.7 V, k = 0.28 mA/V^2		
	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)
−1.0	4.23	3.23	1000.0	4.53	3.53	1000.0	4.83	3.83	1000.0	6.09	5.09	1000.0
−0.8	4.23	3.33	1013.1	4.53	3.63	1013.1	4.83	3.93	1013.1	6.09	5.19	1008.1
−0.6	4.23	3.43	1026.4	4.53	3.73	1026.4	4.83	4.03	1026.4	6.09	5.29	1016.2
−0.4	4.23	3.53	1039.9	4.53	3.83	1039.9	4.83	4.13	1039.9	6.09	5.39	1024.4
−0.2	4.23	3.63	1053.6	4.53	3.93	1053.6	4.83	4.23	1053.6	6.09	5.49	1032.6
0.0	4.23	3.73	1066.8	4.53	4.03	1066.8	4.83	4.33	1066.8	6.09	5.59	1066.8
0.2	4.23	3.83	1053.9	4.53	4.13	1053.9	4.83	4.43	1053.9	6.09	5.69	1032.6
0.4	4.23	3.93	1039.9	4.53	4.23	1039.9	4.83	4.53	1039.9	6.09	5.79	1024.4
0.6	4.23	4.03	1026.4	4.53	4.33	1026.4	4.83	4.63	1026.4	6.09	5.89	1016.2
0.8	4.23	4.13	1013.1	4.53	4.43	1013.1	4.83	4.73	1013.1	6.09	5.99	1008.1
1.0	4.23	4.23	1000.0	4.53	4.53	1000.0	4.83	4.83	1000.0	6.09	6.09	1000.0

Table 3.19: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate, S-bootstrapped substrate, and self-tracking, as shown in Figure 3.16, to observe the effect of v_1 and v_X on R_{XY}. Device parameters: V_T = 0.7 V and k = 0.52 mA/V^2. Circuit parameters: v_2 = 1.0 V, and R_1 = 1.0 kΩ.

v_X (V)	$v_1 = -2.0$ V (i_1 = 0.50 mA, $R_{XY,SET}$ = 500.0 Ω, v_C = 9.12 V, v_{G1} = 5.06 V)		$v_1 = -1.5$ V (i_1 = 0.67 mA, $R_{XY,SET}$ = 666.7 Ω, v_C = 7.18 V, v_{G1} = 4.09 V)		$v_1 = -1.0$ V (i_1 = 1.0 mA, $R_{XY,SET}$ = 1000.0 Ω, v_C = 5.26 V, v_{G1} = 3.13 V)		$v_1 = -0.5$ V (i_1 = 2.0 mA, $R_{XY,SET}$ = 2000.0 Ω, v_C = 3.32 V, v_{G1} = 2.16 V)	
	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)
−2.0	3.56	510.4	2.59	660.1	1.63	990.2	0.66	1980.4
−1.8	3.66	511.4	2.69	661.4	1.73	992.2	0.76	1984.3
−1.6	3.76	512.4	2.79	662.7	1.83	994.1	0.86	1988.2
−1.4	3.86	513.4	2.89	664.0	1.93	996.1	0.96	1992.2
−1.2	3.96	514.4	2.99	665.4	2.03	998.0	1.06	1996.1
−1.0	4.06	515.4	3.09	666.7	2.13	1000.0	1.16	2000.1
−0.8	4.16	516.4	3.19	668.0	2.23	1002.0	1.26	2004.0
−0.6	4.26	517.4	3.29	669.3	2.33	1003.9	1.36	2008.0
−0.4	4.36	518.4	3.39	670.7	2.43	1005.9	1.46	2012.0
−0.2	4.46	519.5	3.49	672.0	2.53	1008.1	1.56	2016.4
0.0	4.56	520.0	3.59	676.9	2.63	1018.1	1.66	2052.9
0.2	4.66	519.5	3.69	672.0	2.73	1008.1	1.76	2016.4
0.4	4.76	518.4	3.79	670.7	2.83	1005.9	1.86	2012.0
0.6	4.86	517.4	3.89	669.3	2.93	1003.9	1.96	2008.0
0.8	4.96	516.4	3.99	668.0	3.03	1002.0	2.06	2004.0
1.0	5.06	515.4	4.09	666.7	3.13	1000.0	2.16	2000.1
1.2	5.16	514.4	4.19	665.4	3.23	998.0	2.26	1996.1
1.4	5.26	513.4	4.29	664.0	3.33	996.1	2.36	1992.2
1.6	5.36	512.4	4.39	662.7	3.43	994.1	2.46	1988.2
1.8	5.46	511.4	4.49	661.4	3.53	992.2	2.56	1984.3
2.0	5.56	510.4	4.59	660.1	3.63	990.2	2.66	1980.4

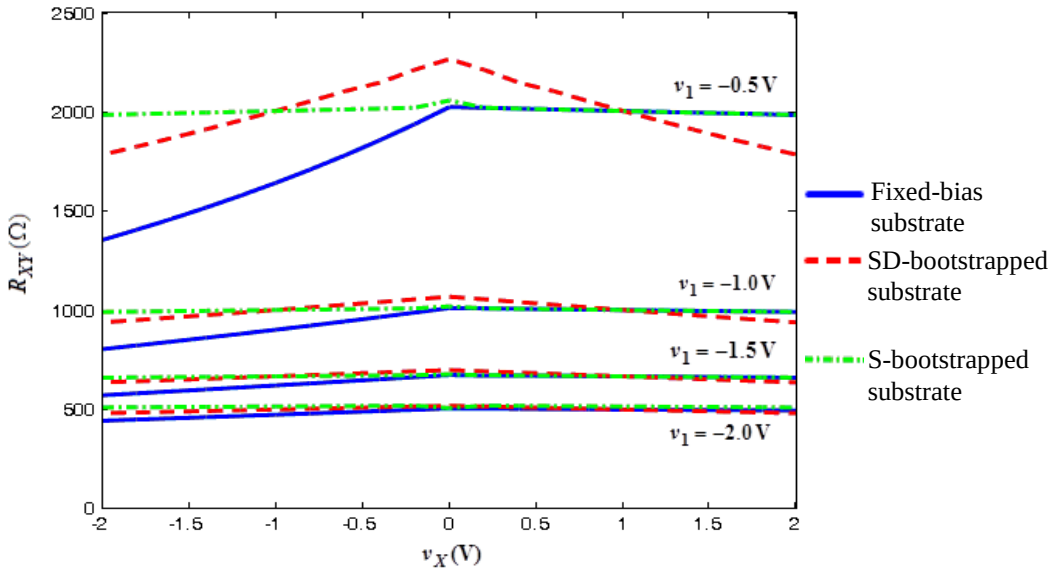


Figure 3.22: Simulation results for matched-pair MOSFET-based floating VCR circuits with self-tracking, SD-bootstrapped gate, and different substrate biases: (a) fixed-bias substrate, (b) SD-bootstrapped substrate, and (c) S-bootstrapped substrate.

Table 3.20: Simulation results for the MOSFET-based floating VCR circuit with SD-bootstrapped gate, S-bootstrapped substrate, and self-tracking, as shown in Figure 3.16, for observing the effect of V_T and k on R_{XY}. Circuit parameters: $v_1 = -1.0$ V, $v_2 = 1.0$ V, and $R_1 = 1.0$ kΩ (i.e. $i_1 = 1.0$ mA and $R_{XY,SET} = 1000.0$ Ω).

v_X	V_T = 0.4 V, k = 0.52 mA/V^2			V_T = 0.7 V, k = 0.52 mA/V^2			V_T = 1.0 V, k = 0.52 mA/V^2			V_T = 0.7 V, k = 0.28 mA/V^2		
(V)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)	v_{G1} (V)	v_{G2} (V)	R_{XY} (Ω)
−1.0	2.83	1.83	1000.0	3.13	2.13	1000.0	3.43	2.43	1000.0	4.69	3.69	1000.0
−0.8	2.83	1.93	1002.0	3.13	2.23	1002.0	3.43	2.53	1002.0	4.69	3.79	1002.0
−0.6	2.83	2.03	1003.9	3.13	2.33	1003.9	3.43	2.63	1003.9	4.69	3.89	1003.9
−0.4	2.83	2.13	1005.9	3.13	2.43	1005.9	3.43	2.73	1005.9	4.69	3.99	1005.9
−0.2	2.83	2.23	1008.1	3.13	2.53	1008.1	3.43	2.83	1008.1	4.69	4.09	1008.1
0.0	2.83	2.33	1018.1	3.13	2.63	1018.1	3.43	2.93	1018.1	4.69	4.19	1018.1
0.2	2.83	2.43	1008.1	3.13	2.73	1008.1	3.43	3.03	1008.1	4.69	4.29	1008.1
0.4	2.83	2.53	1005.9	3.13	2.83	1005.9	3.43	3.13	1005.9	4.69	4.39	1005.9
0.6	2.83	2.63	1003.9	3.13	2.93	1003.9	3.43	3.23	1003.9	4.69	4.49	1003.9
0.8	2.83	2.73	1002.0	3.13	3.03	1002.0	3.43	3.33	1002.0	4.69	4.59	1002.0
1.0	2.83	2.83	1000.0	3.13	3.13	1000.0	3.43	3.43	1000.0	4.69	4.69	1000.0

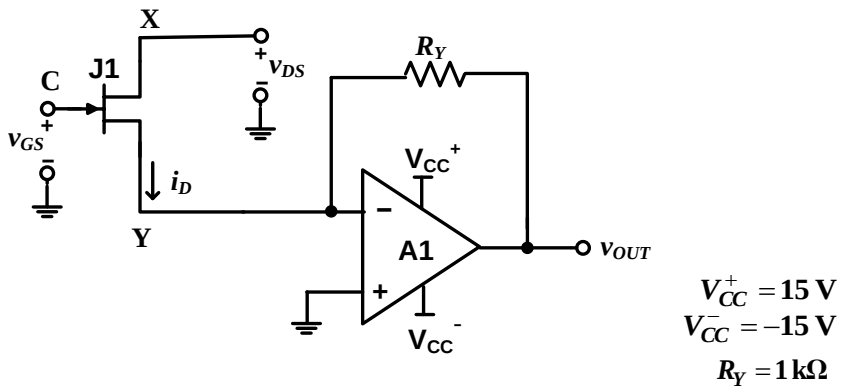


Figure 3.23: Current-to-voltage converter for device characteristics of JFET.

The results are presented in the following subsections. In addition to the results from practical implementation, results from a circuit simulation using the measured parameters of the devices used in implementation are also included.

3.7.1 Test results for grounded VCR using a JFET

The drain characteristics of JFETs are found by measuring i_D as a function of v_{DS}. As shown in Figure 3.23, the drain current i_D of JFET J1 was sensed using current-to-voltage converter realized using op amp LM741 as A1. The current was calculated as $i_D = -v_{OUT}/R_Y$ and it was used for calculating the channel resistance $R_{DS} = v_{DS}/i_D$.

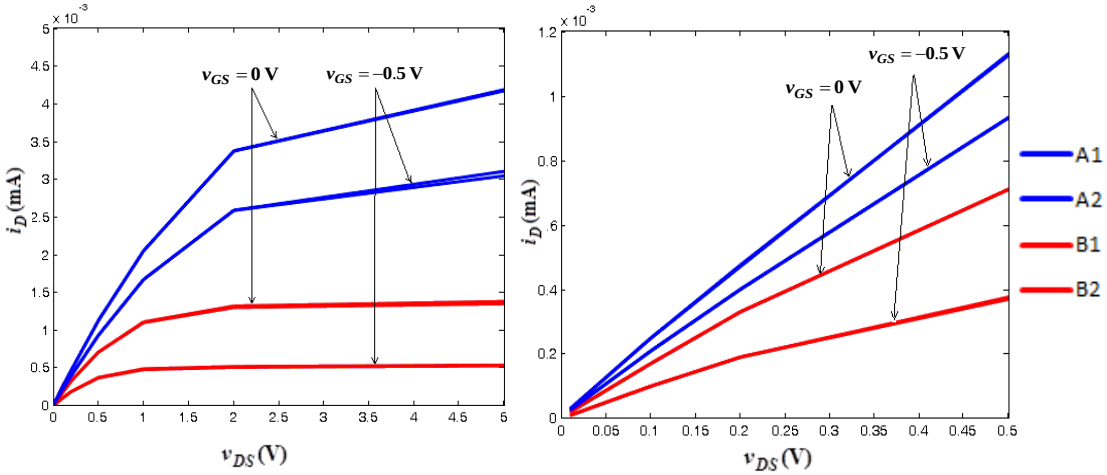


Figure 3.24: Drain characteristics of the JFETs on two pieces of U441 (A1 and A2: two devices on package A, B1 and B2: two devices on package B). Left panel: characteristics for v_{DS} of 0 to 2V, right panel: characteristics for v_{DS} of 0 to 0.5 V.

The drain characteristics of the JFETs on two U441 chips were measured. Each U441 consists of a matched pair of n-channel JFETs. For describing the measurement results, the devices on one package are referred to as A1 and A2 and the devices on the second package are referred to as B1and B2. This testing with two devices on one package and two devices on another package was carried out to get an assessment of the intra-chip and inter-chip variations in the characteristics. The measurements were made for v_{GS} of 0.0 and −0.5 V. The characteristics are plotted in Figure 3.24. For calculating device parameters, the saturation value of i_D for v_{GS} = 0 is taken as I_{DSS} and this value along with the saturation value of i_D at v_{GS} = −0.5 V is used to calculate V_P, in accordance with the expression for saturation current as given in (3.1). The calculated values for the four devices were found to be as the following:

A1: V_P = −2.35 V, I_{DSS} = 4.16 mA; A2: V_P = −2.35 V, I_{DSS} = 4.18 mA

B1: V_P = −1.33 V, I_{DSS} = 1.38 mA; B2: V_P = −1.34 V, I_{DSS} = 1.35 mA

These values and plots show that the characteristics of the JFETs on the same package are almost similar, and there may be large package-to-package differences. From the right panel of the figure, it is seen that the devices work as linear resistor for v_{DS} up to about 0.2 V. Table 3.21 shows the simulation and practical results for the VCR circuit using a single JFET to observe effect of v_X and v_C on R_{XY}. The results are for the circuit using the device A1. The channel resistance of the device for low voltage and calculated in accordance with (3.3) is given in the table as $R_{XY,CAL}$. This circuit provides a grounded resistance and can be used only for $v_X > 0$. It acts as an approximately linear resistor for low values of v_X. The resistance is highly nonlinear as exhibited by increase in its value with increase in v_X.

Table 3.21: Test results for grounded VCR using a JFET to observe effect of v_X and v_C on R_{XY}. Practical results with the device A1 and simulation results using LTspice. Device parameters of A1: V_P = −2.35 V & I_{DSS} = 4.16 mA). $R_{XY,CAL}$(v_C = 0.0 V) = 282.4 Ω, $R_{XY,CAL}$(v_C = −0.5 V) = 358.9 Ω.

v_X (V)	Simulation results		Practical results	
	v_C = 0.0 V	v_C = −0.5 V	v_C = 0.0 V	v_C = −0.5 V
	R_{XY} (Ω)	R_{XY} (Ω)	R_{XY} (Ω)	R_{XY} (Ω)
0.0	285.4	362.3	333.3	384.6
0.1	290.2	370.3	401.6	478.1
0.2	295.7	379.7	421.0	501.2
0.5	301.5	411.4	444.4	536.5
1.0	350.2	480.2	488.3	599.2
2.0	466.7	735.4	594.3	774.6
5.0	1051.4	1694.9	1200.7	1644.7

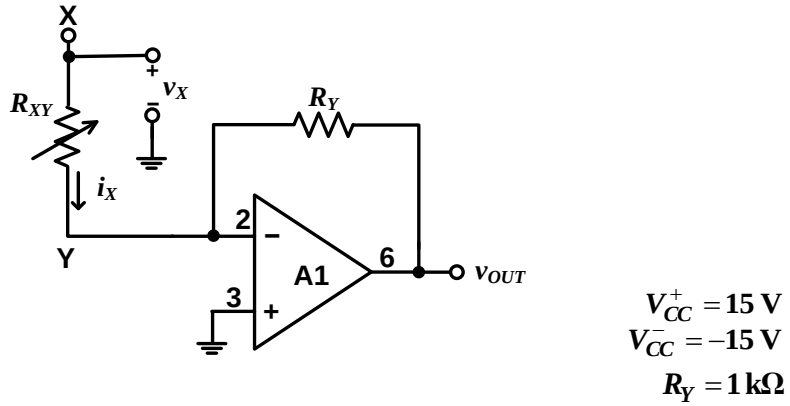


Figure 3.25: Current-to-voltage converter for measuring resistance of the VCR circuit.

3.7.2 Test results for JFET-based floating VCR circuit with SD-bootstrapped gate

The circuit, as shown in Figure 3.4, was implemented using a JFET from U441 (Vishay Siliconix) and op amp IC LM741 (Texas Instruments) with supply of ±12 V. The resistors with the following values were used:

$R_1 = R_2 = R_3 = R_5$= 12 kΩ, R_4= 6 kΩ (two 12 kΩ in parallel). 12 kΩ resistors: well matched resistors selected from a lot of 5% tolerance resistors (measured values: 11.98 − 11.99 kΩ).

The device used was A1 as characterized in the previous subsection and with V_P = −2.35 V and I_{DSS} = 4.16 mA. For the purpose of testing, v_Y was kept at 0 and only v_X was varied. The voltage-to-current converter, as shown in Figure 3.25, was used to measure the drain current i_X. The current was obtained as $i_X = -v_{OUT}/R_Y$ and it was used for calculating $R_{XY} = v_X / i_X$.

Table 3.22: Test results for JFET-based floating VCR circuit with SD-bootstrapped gate, as shown in Figure 3.4, to observe effect of v_X and v_C on R_{XY}. JFET parameters (device A1): $V_P = -2.35$ V & $I_{DSS} = 4.16$ mA. $R_{XY,CAL}$ ($v_C = -2$ V) = 491.8 Ω, $R_{XY,CAL}$ ($v_C = -1$ V) = 358.9 Ω.

v_X (V)	Simulation results				Practical results			
	$v_C = -2.0$ V		$v_C = -1.0$ V		$v_C = -2.0$ V		$v_C = -1.0$ V	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	−1.99	466.7			−2.02	588.6		
−1.8	−1.89	469.4			−1.92	595.0		
−1.6	−1.79	472.0			−1.81	594.7		
−1.4	−1.69	474.7			−1.71	594.7		
−1.2	−1.59	477.4			−1.62	592.3		
−1.0	−1.49	480.2	−0.99	350.9	−1.53	579.4	−1.03	473.3
−0.8	−1.39	483.0	−0.89	353.0	−1.41	603.7	−0.92	485.7
−0.6	−1.29	485.8	−0.79	355.1	−1.31	604.8	−0.82	485.4
−0.4	−1.19	488.7	−0.69	357.2	−1.22	589.1	−0.72	481.9
−0.2	−1.09	491.6	−0.59	359.3	−1.12	579.7	−0.62	472.8
0.2	−0.89	491.6	−0.39	359.3	−0.91	581.1	−0.41	481.9
0.4	−0.79	488.7	−0.29	357.2	−0.81	493.8	−0.31	476.2
0.6	−0.69	485.8	−0.19	355.1	−0.71	486.5	−0.21	481.9
0.8	−0.59	483.0	−0.09	353.0	−0.61	586.5	−0.11	481.0
1.0	−0.49	480.2	0.00	350.9	−0.51	591.1	−0.01	484.3
1.2	−0.39	477.4			−0.40	586.2		
1.4	−0.29	474.7			−0.31	591.5		
1.6	−0.19	472.0			−0.21	600.4		
1.8	−0.09	469.4			−0.11	597.0		
2.0	−0.00	466.7			−0.01	596.8		

Table 3.22 shows the results of the circuit implementation to observe the effects of v_C and v_X on R_{XY}. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.28). For control voltage for $v_C = -2$ V, v_X was varied over −2 to 2 V. For control voltage for $v_C = -1$ V, v_X was restricted over ±1 V to ensure reverse biasing of the gate-channel junction at the source and the drain ends. The results from a circuit simulation using LTspice IV with the device parameters of A1 are also given in the table. The resistance of this circuit is quite linear as compared to that of VCR circuit using single JFET for a relatively wide range of v_X. Simulation shows that as v_X is changed from 0 to ±1 V, R_{XY} decreases by 2.7% and 2.4% for v_C of −1 V and −2 V, respectively. In case of measured results, the changes in R_{XY} are not monotonic. Variation in R_{XY} with reference to its mean value is from −1.5% to 1% for v_C of −1 V and from −14.6% to 6.2% for v_C of −2 V.

Table 3.23: Test results for the JFET-based floating VCR circuit with SD-bootstrapped gate and self-tracking as shown in Figure 3.12, to observe effect of v_X and v_C on R_{XY}. JFET (device A1) parameters: $V_P = -2.35$ V & $I_{DSS} = 4.16$ mA.
$v_1 = -1.0$ V: $R_{XY,SET}$ = 1000.0 Ω, v_C (sim.) = −3.40 V, v_C (pr.) = −3.68 V, v_{G1} (sim.) = −1.20 V, v_{G1} (pr.) = −1.37 V.
$v_1 = -0.5$ V: $R_{XY,SET}$ = 2000.0 Ω, v_C (sim.) = −4.08 V, v_C (pr.) = −4.85 V, v_{G1} (sim.) = −1.54 V, v_{G1} (pr.) = −1.96 V.

v_X (V)	Simulation results				Practical results			
	$v_1 = -1.0$ V		$v_1 = -0.5$ V		$v_1 = -1.0$ V		$v_1 = -0.5$ V	
	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)
−2.0	−2.70	927.6	−3.04	1478.8	−2.84	1000.5	−3.43	1669.4
−1.8	−2.60	951.5	−2.94	1569.8	−2.74	1012.4	−3.33	1630.4
−1.6	−2.50	972.1	−2.84	1668.8	−2.64	1020.4	−3.23	1771.8
−1.4	−2.40	987.1	−2.74	1775.5	−2.54	1047.9	−3.13	1827.6
−1.2	−2.30	994.2	−2.64	1887.7	−2.44	1030.9	−3.03	1892.7
−1.0	−2.20	1000.0	−2.54	2000.0	−2.34	1036.3	−2.93	1953.1
−0.8	−2.10	1005.8	−2.44	2098.7	−2.24	1047.1	−2.83	2020.2
−0.6	−2.00	1011.7	−2.34	2150.8	−2.14	1054.5	−2.73	2047.8
−0.4	−1.90	1017.7	−2.24	2163.5	−2.04	1030.9	−2.63	2072.5
−0.2	−1.80	1023.7	−2.14	2176.4	−1.94	1015.2	−2.53	2083.3
0.2	−1.60	1023.7	−1.94	2176.4	−1.74	1010.1	−2.33	2083.3
0.4	−1.50	1017.7	−1.84	2163.5	−1.64	1041.7	−2.23	2072.5
0.6	−1.40	1011.7	−1.74	2150.8	−1.54	1048.9	−2.13	2061.8
0.8	−1.30	1005.8	−1.64	2098.7	−1.44	1044.4	−2.03	2025.3
1.0	−1.20	1000.0	−1.54	2000.0	−1.34	1005.0	−1.93	1972.4
1.2	−1.10	994.2	−1.44	1887.7	−1.23	1039.8	−1.83	1920.0
1.4	−1.00	987.1	−1.34	1775.5	−1.14	1042.4	−1.73	1871.6
1.6	−0.90	972.1	−1.24	1668.8	−1.03	1034.9	−1.63	1816.1
1.8	−0.80	951.5	−1.14	1569.8	−0.94	1036.8	−1.52	1633.4
2.0	−0.70	927.6	−1.04	1478.8	−0.83	1029.3	−1.42	1715.3

3.7.3 Test results for JFET-based floating VCR circuit with SD-bootstrapped gate and self-tracking

The circuit is shown in Figure 3.12. It was implemented using U441 package for the matched pair of n-channel JFETs and IC LM741 for op amps. The resistors with following values were used:

$R_2 = R_3 = 1$ MΩ, $R_4 = R_5 = R_6 = R_7 = 12$ kΩ, $R_8 = 6$ kΩ (two 12 kΩ in parallel). 12 kΩ resistors: well matched resistors selected from a lot of 5% tolerance resistors (measured values: 11.98 − 11.99 kΩ), 1 MΩ resistors: 5% tolerance.

The circuit was tested with v_Y kept at 0 and varying v_X. The control voltage was applied as v_1 with v_2 = 1.0 V and $R_1 = 998$ Ω. During these measurements, values of v_{G1} and v_{G2} were also recorded. The results are given in Table 3.23. The calculated values of R_{XY} are 2000.0 Ω and 1000.0 Ω for voltages v_1 = −0.5 V and v_1 = −1.0 V, respectively. Simulation results show that R_{XY} decreases by 2.3% as v_X is changed from 0 to ±1 V for v_1

= −1.0 V and by 8.1% for v_1 = −0.5 V. Measurements show that the values of v_C corresponding to v_1 of −1 V and −0.5 V are −3.68 and −4.85 V, respectively. The variation in R_{XY} with reference to its mean value is from −2.7% to 2.0% for v_1 of −1 V and from −4.2% to 2.2% for v_1 of −0.5 V.

3.8 Test results for VCR circuits using MOSFET

Circuit implementation and testing are carried out to study the operation of the following six MOSFET-based VCR circuits:

i) Grounded VCR circuit using a MOSFET,
ii) MOSFET-based floating VCR circuit with SD-bootstrapped gate and fixed-bias substrate as shown in Figure 3.7,
iii) MOSFET-based floating VCR circuit with SD-bootstrapped gate and SD-bootstrapped substrate as shown in Figure 3.8,
iv) MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped substrate as shown in Figure 3.9,
v) MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped-bias substrate as shown in Figure 3.10,
vi) MOSFET-based floating VCR circuit with SD-bootstrapped gate, fixed-bias substrate, and self-tracking, as shown in Figure 3.13.

In addition to the results from practical implementation, results from a circuit simulation using the measured parameters of the devices used in implementation are also included. The circuit shown in Figure 3.15, 3.16, and 3.17 are not implemented for testing due to unavailability of matched pair of MOSFETs with independent substrate terminals.

3.8.1 Test results for grounded VCR using a MOSFET

The drain characteristics of MOSFETs was found by measuring i_D as a function of v_{DS}. As shown in Figure 3.26, the drain current i_D of M1 was sensed using current-to-voltage converter realized using op amp LM741 as A1. The current was calculated as $i_D = -v_{OUT}/R_Y$ and it was used for calculating the resistance $R_{DS} = v_{DS}/i_D$. The drain characteristics of four MOSFETs on each of two ALD1106 ICs were measured. The devices on one IC are referred to as A1, A2, A3, and A4 and the devices on second IC are referred to as B1, B2, B3, and B4. This testing with four devices on one chip and four devices on another chip was carried out for an assessment of the intra-chip and inter-chip variations in the characteristics. The measurements were made for V_{BB} of 0 and −5 V, and v_{GS} of 3, 3.5, and 4 V. The characteristics are plotted in Figure 3.27. Although the characteristics are almost

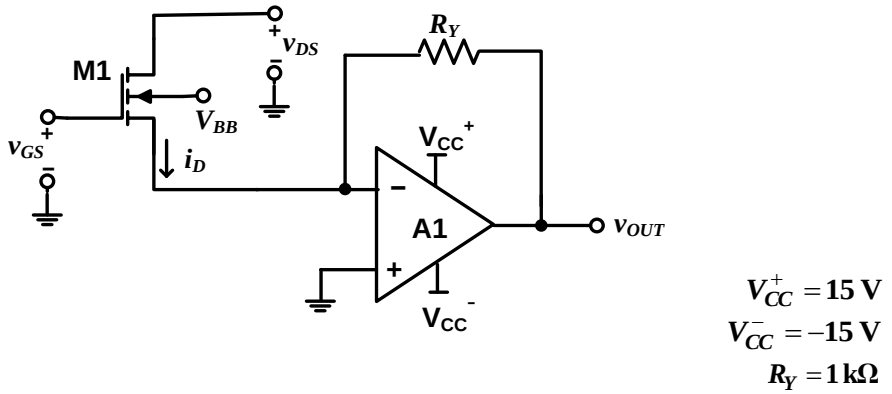


Figure 3.26: Current-to-voltage converter for device characteristics of MOSFET.

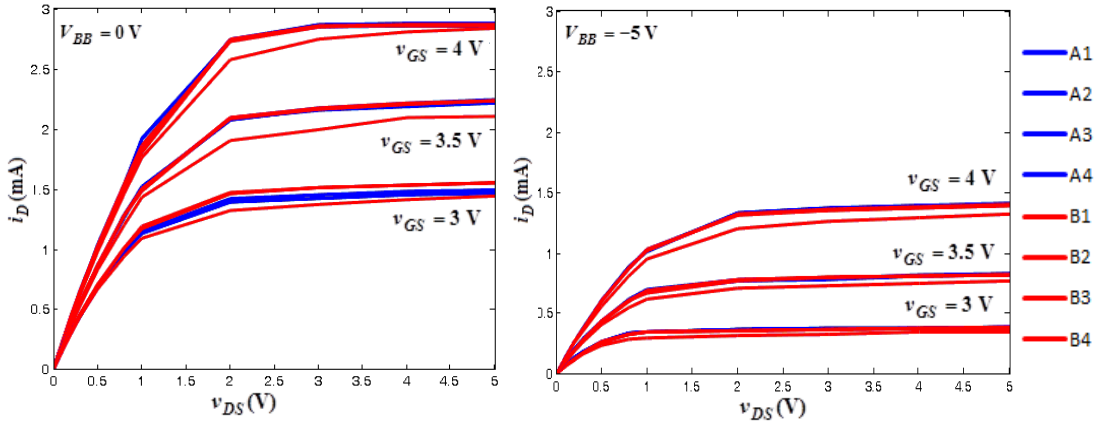


Figure 3.27: Drain characteristics of four devices on two pieces of ALD1106 (A, B: two ICs, A1 − A4: 4 devices on IC-A) for V_{BB} of 0 and −5 V.

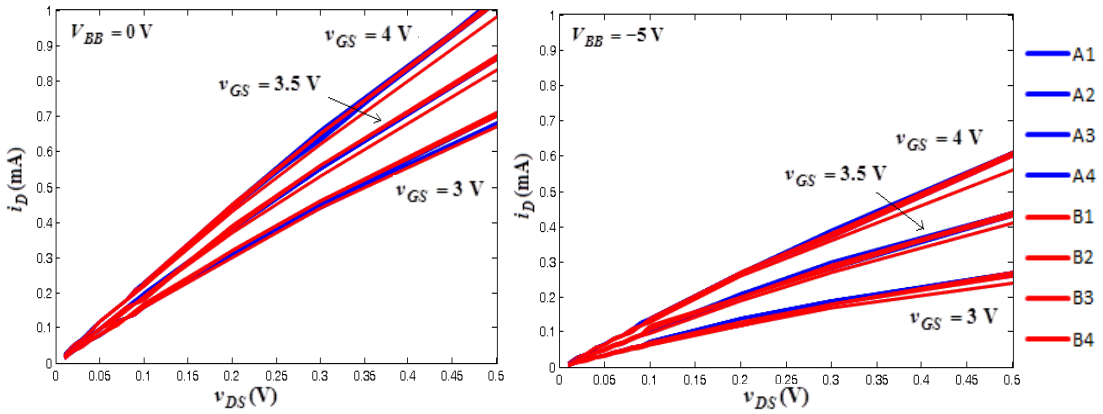


Figure 3.28: Drain characteristics of Figure 3.27 for small v_{DS}.

similar, there are some device-to-device differences, and the difference is more prominent in case of device labeled as B1. A comparison of characteristics of the drain current for the two substrate voltages shows that the substrate-source bias has a significant effect on the drain current. Figure 3.28 shows the drain characteristics of the devices for small v_{DS}. It is seen

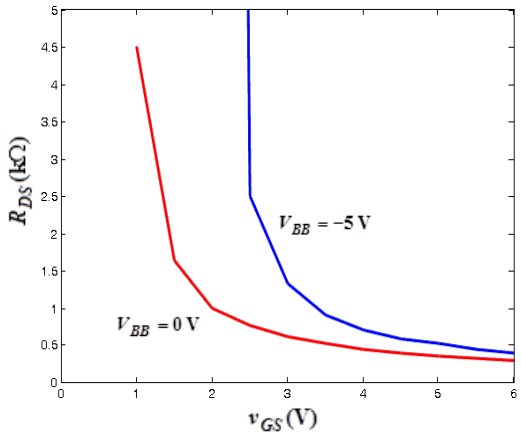


Figure 3.29: R_{DS} versus v_{GS} curve for one of the devices on ALD1106 for V_{BB} of 0 and −5 V.

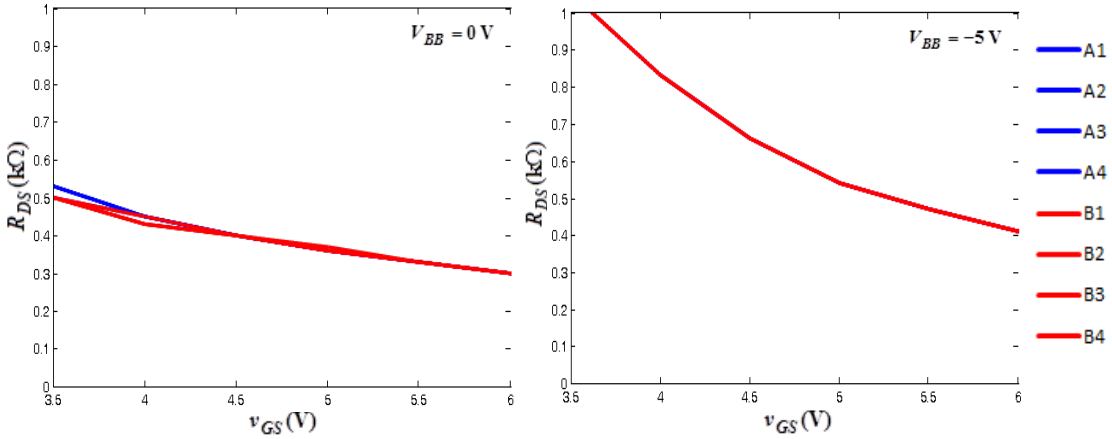


Figure 3.30: R_{DS} versus v_{GS} curves for four devices on two pieces of ALD1106 for V_{BB} of 0 and −5 V.

that the devices work as linear resistor for v_{DS} up to about 0.15 V

Figure 3.29 shows the relationship between R_{DS} and v_{GS} for one of the devices on ALD1106. According to the datasheet of ALD1106 IC, typical value of drain-source resistance at v_{GS} = 5 V and v_{DS} = 0.1 V is 350 Ω. Experimentally observed values show a small spread around it. The plots show that v_{BS} has a large effect on R_{DS}. For V_{BB} = 0 V, R_{DS} gets into kΩ range for v_{GS} < 1 V. For V_{BB} = −5 V, it happens for v_{GS} < 2.5 V. Figure 3.30 shows the resistances for four devices on two pieces of ALD1106. It may be noted that a large value of substrate-source reverse bias increases the channel resistance and masks the device-dependent spread in the values.

The saturation values of i_{DS} at two values of v_{GS} were taken and device parameters V_T and k are calculated in accordance with the expression for saturation current as given in (3.10). The calculated values were found to be as the following:

A1: V_T = 0.7 V and k = 0.69 mA/V^2

Table 3.24: Test results for the grounded VCR using a MOSFET to observe effect of v_X, V_{BB}, and v_C on R_{XY}. MOSFET (A1) parameters: V_T = 0.7 V & k = 0.69 mA/V^2.

(a) V_{BB} = 0 V: $R_{XY,CAL}$(v_C = 3.0 V) = 630.1 Ω, $R_{XY,CAL}$(v_C = 3.5 V) = 517.6 Ω

v_X (V)	Simulation results		Practical results	
	v_C = 3.0 V	v_C = 3.5 V	v_C = 3.0 V	v_C = 3.5 V
	R_{XY} (Ω)	R_{XY} (Ω)	R_{XY} (Ω)	R_{XY} (Ω)
0.1	643.5	526.5	625.0	500.0
0.2	657.4	535.7	645.2	526.3
0.5	703.4	565.5	735.3	574.7
1.0	797.2	623.9	877.2	671.1
2.0	1092.9	789.4	1418.4	956.9
5.0	2609.2	1760.5	3355.7	2232.1

(b) V_{BB} = −5 V: $R_{XY,CAL}$(v_C = 3.0 V) = 1811.6 Ω, $R_{XY,CAL}$(v_C = 3.5 V) = 1114.8 Ω

v_X (V)	Simulation results		Practical results	
	v_C = 3.0 V	v_C = 3.5 V	v_C = 3.0 V	v_C = 3.5 V
	R_{XY} (Ω)	R_{XY} (Ω)	R_{XY} (Ω)	R_{XY} (Ω)
0.1	1941.5	1162.2	1315.7	1000
0.2	2078.9	1209.6	1428.6	1000
0.5	2642.5	1379.0	1851.2	1136.4
1.0	4532.5	1803.3	2857.1	1449.3
2.0	8976.2	3385.2	5405.4	2564.1
5.0	21799.4	8221.3	12820.5	6097.6

Table 3.24 shows the simulation and practical results for the VCR circuit using a single JFET to observe effect of v_X, V_{BB}, and v_C on R_{XY}. The results are for the circuit using the device A1. The channel resistance of the device for low voltage is calculated in accordance with (3.19) and is given in the table as $R_{XY,CAL}$. The resistance is highly nonlinear as exhibited by increase in its value with increase in v_X. The results also show that V_{BB} has a significant effect on R_{XY}.

3.8.2 Test results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and fixed-bias substrate

The floating VCR circuit with bootstrapped gate voltage and fixed-bias substrate is described in Section 3.4 and shown in Figure 3.7. It was implemented using MOSFET from ALD1106 (Advanced Linear Devices) and op amp IC LM741 (Texas Instruments) with supply of ±15 V. The resistors with following values were used:

Table 3.25: Test results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and fixed-bias substrate, as shown in Figure 3.7, to observe effect of v_X and v_C on R_{XY}. MOSFET (A1) parameters: V_T = 0.7 V & k = 0.69 mA/V^2. V_{BB} = −5 V, $R_{XY,CAL}$(v_C = 6.0 V) = 1811.6 Ω, $R_{XY,CAL}$(v_C = 7.0 V) = 1114.8 Ω.

v_X (V)	Simulation results				Practical results			
	v_C = 6.0 V		v_C = 7.0 V		v_C = 6.0 V		v_C = 7.0 V	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	1.99	1140.6	2.49	813.9	1.99	1201.2	2.49	891.3
−1.8	2.09	1190.4	2.59	839.4	2.09	1216.2	2.59	894.6
−1.6	2.19	1243.1	2.69	865.8	2.19	1232.6	2.69	901.4
−1.4	2.29	1299.2	2.79	893.2	2.29	1247.7	2.79	908.5
−1.2	2.39	1358.9	2.89	921.6	2.39	1269.8	2.89	913.2
−1.0	2.49	1422.6	2.99	951.1	2.49	1295.3	2.99	909.1
−0.8	2.59	1490.9	3.09	981.8	2.59	1309.3	3.09	932.4
−0.6	2.69	1564.2	3.19	1013.4	2.69	1330.4	3.19	936.0
−0.4	2.79	1643.2	3.29	1047.2	2.79	1355.9	3.29	956.9
−0.2	2.89	1728.7	3.39	1082.0	2.89	1517.2	3.39	934.6
0.2	3.09	1817.7	3.59	1116.3	3.09	1369.8	3.59	943.4
0.4	3.19	1814.1	3.69	1114.0	3.19	1413.4	3.69	966.2
0.6	3.29	1810.5	3.79	1111.8	3.29	1459.8	3.79	990.1
0.8	3.39	1806.9	3.89	1109.6	3.39	1467.8	3.89	1001.2
1.0	3.49	1803.3	3.99	1107.4	3.49	1497.0	3.99	1012.1
1.2	3.59	1799.7	4.09	1105.2	3.59	1513.2	4.09	1029.1
1.4	3.69	1796.2	4.19	1103.1	3.69	1530.0	4.19	1046.3
1.6	3.79	1792.6	4.29	1100.9	3.79	1544.4	4.29	1057.5
1.8	3.89	1782.4	4.39	1098.7	3.89	1558.4	4.39	1072.7
2.0	3.99	1762.5	4.49	1096.6	3.99	1560.1	4.49	1077.0

$R_1 = R_2 = R_3 = R_5$= 12 kΩ, R_4= 6 kΩ (two 12 kΩ in parallel). 12 kΩ resistors: well matched resistors selected from a lot of 5% tolerance resistors (measured values: 11.98 − 11.99 kΩ).

Table 3.25 shows test results for the implemented circuit. The results are for the circuit using the device A1 with device parameters V_T = 0.7 V and k = 0.69 mA/V^2. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.43).The resistance of this circuit is quite linear as compared to that of the grounded VCR using a MOSFET with V_{BB} = −5 V. The simulation shows that R_{XY} decreases by 0.8 % for v_C of 6.0 V as v_X is changed from 0 to 1 V and it decreases by 17.6% as v_X is varied from 0 to −1 V. The corresponding decreases for v_C of 7 V are 0.8% and 12.1%. In case of measured values for v_C of 6 V, variation in R_{XY} with reference to its mean value is from −4.9% to 3.8% as v_X is varied from 0 to 1 V and from −4.8% to 11.4% as v_X is varied from 0 to −1 V. The corresponding variations for v_C of 7 V are −4.0% to 3.0% and −2.6% to 0.2%.

Table 3.26: Test results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and SD-bootstrapped substrate, as shown in Figure 3.8, to observe effect of v_X and v_C on R_{XY}. MOSFET (A1) parameters: V_T = 0.7 V & k = 0.69 mA/V^2. V_{BB} = −5 V: $R_{XY,CAL}(v_C = 6.0\text{ V})$ = 1811.6 Ω, $R_{XY,CAL}(v_C = 7.0\text{ V})$ = 1114.8 Ω.

v_X (V)	Simulation results				Practical results			
	v_C = 6.0 V		v_C = 7.0 V		v_C = 6.0 V		v_C = 7.0 V	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	1.99	1408.7	2.49	941.8	2.01	1357.8	2.49	993.0
−1.8	2.09	1443.3	2.59	957.8	2.11	1368.8	2.59	997.2
−1.6	2.19	1479.2	2.69	974.1	2.22	1380.5	2.69	994.4
−1.4	2.29	1516.3	2.79	990.8	2.32	1383.5	2.79	993.6
−1.2	2.39	1554.9	2.89	1007.8	2.42	1376.1	2.89	987.6
−1.0	2.49	1595.1	2.99	1025.2	2.51	1364.2	2.99	985.2
−0.8	2.59	1637.3	3.09	1043.0	2.62	1381.7	3.09	981.6
−0.6	2.69	1680.1	3.19	1061.2	2.72	1379.3	3.19	988.5
−0.4	2.79	1725.2	3.29	1079.9	2.82	1388.9	3.29	990.1
−0.2	2.89	1772.3	3.39	1098.9	2.92	1388.9	3.39	961.5
0.2	3.09	1772.3	3.59	1098.9	3.12	1342.3	3.59	966.2
0.4	3.19	1725.2	3.69	1079.9	3.22	1346.8	3.69	968.5
0.6	3.29	1680.1	3.79	1061.2	3.32	1360.5	3.79	975.6
0.8	3.39	1637.3	3.89	1043.0	3.42	1355.9	3.89	965.0
1.0	3.49	1595.1	3.99	1025.2	3.52	1342.3	3.99	978.5
1.2	3.59	1554.9	4.09	1007.8	3.62	1355.9	4.09	977.9
1.4	3.69	1516.3	4.19	990.8	3.72	1352.6	4.19	981.1
1.6	3.79	1479.2	4.29	974.1	3.82	1353.6	4.29	984.0
1.8	3.89	1443.3	4.39	957.8	3.92	1350.3	4.39	984.7
2.0	3.99	1408.7	4.49	941.8	4.02	1331.5	4.49	986.2

3.8.3 Test results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and SD-bootstrapped substrate

The circuit is shown in Figure 3.8. It was implemented using the device A1 with device parameters V_T = 0.7 V and k = 0.69 mA/V^2. The resistors with following values were used:

$R_1 = R_2 = R_3 = R_5 = R_6 = R_7 = R_8 = R_9$ = 12 kΩ, $R_4 = R_{10}$ = 6 kΩ (two 12 kΩ in parallel). 12 kΩ resistors: well matched resistors selected from a lot of 5% tolerance resistors (measured values: 11.98 − 11.99 kΩ).

Table 3.26 shows the results of the circuit implementation to observe the effects of v_C and v_X on R_{XY}. The voltage v_X was varied from −2 to 2 V. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.43). The simulations show that R_{XY} decreases by 10.0% for v_C of 6.0 V as v_X is changed from 0 to ±1 V. The corresponding decreases for v_C of 7 V are 6.7%. In case of measured values for v_C of 6 V, variation in R_{XY} with reference to its mean value is from −1.7% to 1.7% as v_X is varied from 0 to ±1 V. The corresponding variations for v_C of 7 V are −1.5% to 1.4%. The variation is much smaller as compared to the circuit with fixed-bias substrate.

Table 3.27: Test results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped substrate, as shown in Figure 3.9, to observe effect of v_X and v_C on R_{XY}. MOSFET (A1) parameters: as V_T = 0.7 V & k = 0.69 mA/V^2. V_{BB} = 0 V: $R_{XY,CAL}$(v_C = 6.0 V) = 630.1 Ω, $R_{XY,CAL}$(v_C = 7.0 V) = 517.6 Ω.

v_X (V)	Simulation results				Practical results			
	v_C = 6.0 V		v_C = 7.0 V		v_C = 6.0 V		v_C = 7.0 V	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	1.99	617.7	2.49	507.4	2.02	746.3	2.49	638.2
−1.8	2.09	618.9	2.59	508.4	2.12	731.7	2.59	627.2
−1.6	2.19	620.2	2.69	509.4	2.23	717.5	2.69	613.3
−1.4	2.29	621.4	2.79	510.4	2.32	696.5	2.79	602.7
−1.2	2.39	622.6	2.89	511.5	2.43	685.7	2.89	590.5
−1.0	2.49	623.8	2.99	512.5	2.53	671.1	2.99	575.7
−0.8	2.59	625.1	3.09	513.5	2.63	666.7	3.09	568.6
−0.6	2.69	626.4	3.19	514.5	2.73	652.2	3.19	560.2
−0.4	2.79	627.6	3.29	515.5	2.83	625.0	3.29	553.2
−0.2	2.89	628.9	3.39	516.6	2.93	625.0	3.39	530.5
0.2	3.09	628.9	3.59	516.6	3.13	606.1	3.59	522.2
0.4	3.19	627.6	3.69	515.5	3.23	615.4	3.69	538.3
0.6	3.29	626.4	3.79	514.5	3.33	631.6	3.79	555.0
0.8	3.39	625.1	3.89	513.5	3.43	655.7	3.89	568.2
1.0	3.49	623.8	3.99	512.5	3.53	662.2	3.99	573.4
1.2	3.59	622.6	4.09	511.5	3.63	681.8	4.09	586.8
1.4	3.69	621.4	4.19	510.4	3.73	696.5	4.19	597.5
1.6	3.79	620.2	4.29	509.4	3.83	711.1	4.29	610.2
1.8	3.89	618.9	4.39	508.4	3.93	725.8	4.39	622.8
2.0	3.99	617.7	4.49	507.4	4.03	740.7	4.49	633.1

3.8.4 Test results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped substrate

The circuit in Figure 3.9 with SD-bootstrapped gate and S-bootstrapped substrate was implemented. The device used was A1 with V_T = 0.7 V and k = 0.69 mA/V^2. The resistors with the following values were used:

$R_1 = R_2 = R_3 = R_5$ = 12 kΩ, R_4 = 6 kΩ (two 12 kΩ in parallel), $R_6 = R_7$ = 1MΩ. 12 kΩ resistors: well matched resistors selected from a lot of 5% tolerance resistors (measured values: 11.98 − 11.99 kΩ), 1 MΩ resistors: 5% tolerance. Diodes 1N4148 were used as D_1, D_2, and D_3.

Table 3.27 shows the simulation and practical results of the circuit to observe the effects of v_C and v_X on R_{XY}. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.43). The simulation results show that R_{XY} decreases by 0.9% for v_C of 6.0 and 7.0 V as v_X is changed from 0 to ±1 V. In case of measured values for v_C of 6 V, variation in R_{XY} with reference to its mean value is from −5.4% to 4.7% as v_X is varied from 0 to ±1 V. The corresponding variations for v_C of 7 V are −5.8% to 3.8%.

Table 3.28: Test results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped-bias substrate, as shown in Figure 3.10, to observe effect of v_X and v_C on R_{XY}. MOSFET (A1) parameters: V_T = 0.7 V & k = 0.69 mA/V^2. V_{BB} = −5 V: $R_{XY,CAL}$(v_C = 6.0 V) = 1811.6 Ω, $R_{XY,CAL}$(v_C = 7.0 V) = 1114.8 Ω.

v_X (V)	Simulation results				Practical results			
	v_C = 6.0 V		v_C = 7.0 V		v_C = 6.0 V		v_C = 7.0 V	
	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)	v_G (V)	R_{XY} (Ω)
−2.0	1.99	1762.5	2.49	1096.6	2.02	1556.4	2.51	979.4
−1.8	2.09	1782.4	2.59	1098.7	2.12	1550.4	2.62	974.5
−1.6	2.19	1792.6	2.69	1100.9	2.22	1536.9	2.71	975.6
−1.4	2.29	1796.2	2.79	1103.1	2.32	1523.4	2.81	971.5
−1.2	2.39	1799.7	2.89	1105.2	2.42	1501.9	2.91	966.9
−1.0	2.49	1803.3	2.99	1107.4	2.52	1490.3	3.01	963.4
−0.8	2.59	1806.9	3.09	1109.6	2.62	1470.6	3.11	959.2
−0.6	2.69	1810.5	3.19	1111.8	2.72	1438.8	3.21	952.4
−0.4	2.79	1814.1	3.29	1114.0	2.82	1388.9	3.31	968.5
−0.2	2.89	1817.9	3.39	1116.4	2.92	1379.3	3.51	934.6
0.2	3.09	1817.9	3.59	1116.4	3.12	1369.8	3.61	956.9
0.4	3.19	1814.1	3.69	1114.0	3.22	1388.9	3.71	963.8
0.6	3.29	1810.5	3.79	1111.8	3.32	1418.4	3.81	986.8
0.8	3.39	1806.9	3.89	1109.6	3.42	1438.8	3.91	998.7
1.0	3.49	1803.3	3.99	1107.4	3.52	1457.7	4.01	1009.1
1.2	3.59	1799.7	4.09	1105.2	3.62	1494.4	4.11	1019.5
1.4	3.69	1796.2	4.19	1103.1	3.72	1502.1	4.21	1031.7
1.6	3.79	1792.6	4.29	1100.9	3.82	1512.3	4.31	1047.1
1.8	3.89	1782.4	4.39	1098.7	3.92	1522.8	4.41	1058.2
2.0	3.99	1762.5	4.49	1096.6	4.02	1549.2	4.51	1068.4

3.8.5 Test results for MOSFET-based floating VCR circuit with SD-bootstrapped gate and S-bootstrapped-bias substrate

The circuit, as shown in Figure 3.10, was implemented using the device A1 with device parameters V_T = 0.7 V and k = 0.69 mA/V^2. The resistors with the following values were used:

$R_1 = R_2 = R_3 = R_5 = R_8 = R_9 = R_{10} = R_{11}$ = 12 kΩ, R_4 = 6 kΩ (two 12 kΩ in parallel), $R_6 = R_7$ = 1MΩ. 12 kΩ resistors: well matched resistors selected from a lot of 5% tolerance resistors (measured values: 11.98 − 11.99 kΩ), 1 MΩ resistors: 5% tolerance. Diodes 1N4148 diodes were used as D_1, D_2, and D_3.

Table 3.28 shows the results of the circuit implementation to observe the effects of v_C and v_X on R_{XY}. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.43). The simulation results show that R_{XY} decreases by 0.8% for v_C of 6.0 and 7.0 V as v_X is changed from 0 to ±1 V. In case of measured values for v_C of 6 V, variation in R_{XY} with reference to its mean value is from −3.8% to 4.6% as v_X is varied from 0 to ±1 V. The corresponding variations for v_C of 7 V are −3.6% to 3.0%. The results show that the circuit

with S-bootstrapped-bias substrate of Figure 3.10 has no specific advantage over the circuit with S-bootstrapped substrate of Figure 3.9.

3.8.6 Test results for MOSFET-based floating VCR circuit with SD-bootstrapped gate, fixed-bias substrate, and self-tracking

The circuit was shown in Figure 3.13. It was implemented using IC ALD1106 for matched MOSFET pair and IC LM741 for op amp. The devices on 4-device ALD1106 have their substrates shorted as a common terminal on the chip. This common substrate was connected to $V_{BB} = -5$ V. The resistors with the following values were used:

$R_2 = R_3 =$ 1 MΩ, $R_4 = R_5 = R_6 = R_7 =$ 12 kΩ, R_8 = 6 kΩ (two 12 kΩ resistors in parallel). 12 kΩ resistors: well matched resistors selected from a lot of 5% tolerance resistors (measured values: 11.98 − 11.99 kΩ), 1 MΩ resistors: 5% tolerance.

The circuit was tested with v_Y kept at 0 and varying v_X. The control voltage was applied as v_1 with v_2 = 1.0 V and R_1 of 1 kΩ (measured value of 998 Ω). During these measurements, values of v_{G1}, v_C, and v_{G2} were also recorded. The results are given in Table 3.29. $R_{XY,CAL}$ in the table refers to values of R_{XY} calculated using (3.61).The calculated values of R_{XY} are 2000.0 Ω and 1000.0 Ω for v_1 of −0.5 V and −1.0 V, respectively. The simulation shows that R_{XY} decreases by 0.8 % for v_1 of −1.0 V as v_X is changed from 0 to 1 V and it decreases by 11.1% as v_X is varied from 0 to −1 V. The corresponding decreases for v_1 of −0.5 V are 0.8% and 19.1%. In case of measured values for v_1 of −1.0 V, variation in R_{XY} with reference to its mean value is from −3.1% to 2.7% as v_X is varied from 0 to 1 V and from −1.3% to 0.9% as v_X is varied from 0 to −1 V. The corresponding variations for v_1 of −0.5 V are −4.3% to 2.4% and −6.4% to 9.7%.

3.9 Summary

After a review of the VCR circuits, a matched-pair JFET based circuit has been devised for realizing a floating VCR in which the SD-bootstrapping of gate is used to keep the resistance constant against variation in the terminal voltages and a feedback loop based self-tracking is used for stabilizing the resistance against device parameters variations. The value of the VCR is given as $R_{XY} = v_2/(-v_1)R_1$ and thus it can be varied by changing either of the two input control voltages v_1 and v_2 or their combination to realize the desired time-varying resistance. In addition, it can be used as a resistance mirror by varying R_1. The concepts of SD-bootstrapped gate and self-tracking can be extended to realize a bank of parallel-controlled

Table 3.29: Test results for the MOSFET-based VCR circuit with SD-bootstrapped gate, fixed-bias substrate, and self-tracking as shown in Figure 3.13, to observe effect of v_X and v_1 on R_{XY} . MOSFET (device A1) parameters: V_T = 0.7 V & k = 0.69 mA/V^2.
v_1 = −1.0 V: $R_{XY,SET}$ = 1000.0 Ω, v_C (sim.) = 7.28 V, v_C (pr.) = 7.06 V, v_{G1} (sim.) = 4.14 V, v_{G1} (pr.) = 4.00 V.
v_1 = −0.5 V: $R_{XY,SET}$ = 2000.0 Ω, v_C (sim.) = 5.84 V, v_C (pr.) = 5.51 V, v_{G1} (sim.) = 3.42 V, v_{G1} (pr.) = 3.24 V.

v_X (V)	Simulation results				Practical results			
	v_1 = −1.0 V		v_1 = −0.5 V		v_1 = −1.0 V		v_1 = −0.5 V	
	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)
−2.0	2.64	753.8	1.92	1217.1	2.53	867.3	1.75	1433.7
−1.8	2.74	775.7	2.02	1273.7	2.63	893.3	1.85	1480.3
−1.6	2.84	798.4	2.12	1334.1	2.73	883.5	1.95	1513.7
−1.4	2.94	821.7	2.22	1398.7	2.83	888.3	2.05	1553.8
−1.2	3.04	845.8	2.32	1467.9	2.93	898.2	2.15	1589.4
−1.0	3.14	870.8	2.42	1542.3	3.03	899.3	2.25	1631.3
−0.8	3.24	896.6	2.52	1622.6	3.13	912.2	2.35	1913.9
−0.6	3.34	923.4	2.62	1709.5	3.23	916.0	2.45	1694.9
−0.4	3.44	951.5	2.72	1803.9	3.33	919.5	2.55	1724.1
−0.2	3.54	980.0	2.82	1907.1	3.43	909.1	2.65	1754.4
0.2	3.74	1008.0	3.02	2016.0	3.63	930.2	2.85	1832.9
0.4	3.84	1005.9	3.12	2012.0	3.73	947.8	2.95	1877.9
0.6	3.94	1003.9	3.22	2008.0	3.83	969.3	3.05	1923.1
0.8	4.04	1002.0	3.32	2004.0	3.93	979.2	3.15	1960.8
1.0	4.14	1000.0	3.42	2000.0	4.03	989.1	3.25	1980.2
1.2	4.24	998.0	3.52	1996.1	4.13	1004.2	3.35	1990.1
1.4	4.34	996.1	3.62	1992.2	4.23	1017.4	3.45	2002.8
1.6	4.44	994.1	3.72	1982.4	4.33	1031.6	3.55	2005.0
1.8	4.54	992.2	3.82	1959.1	4.43	1044.7	3.65	1998.9
2.0	4.64	990.2	3.92	1926.8	4.53	1058.2	3.75	1970.4

floating resistors. The circuit has been validated by simulation as well as practical measurements using a matched-pair of n-channel JFETs.

The concept of SD-bootstrapped gate and self-tracking is applied for realization of a floating VCR using matched-pair of MOSFETs. Here we face the additional problem of stabilizing the resistance against channel modulation caused by variation in substrate-channel or substrate-source voltage. Several solutions have been presented and evaluated by simulation and practical measurements using a matched-pair of n-channel MOSFETs. Out of these solutions, simulation has shown that the circuit with S-bootstrapped substrate gives most satisfactory results and the linearity is comparable to JFET-based circuit. However, this circuit could not be practically tested, as the available matched-pair MOSFETs have their substrates shorted, while our floating VCR circuit requires them to be driven independently.

In summary, we can use the matched-pair n-channel JFET-based VCR circuit with SD-bootstrapped gate and self-tracking for realizing a time-varying floating resistance with terminal voltages of up to ±1V for use in a bioimpedance simulator. The control voltages can

be generated using a microcontroller with on-chip DAC. MOSFET-based circuit with S-bootstrapped substrate can be used for a relatively larger range of terminal voltages and it needs to be practically tested using matched-pair of MOSFETs with independent substrates.

Chapter 4
BIOIMPEDANCE SIMULATOR

4.1 Introduction

The bioimpedance simulator is needed for testing the linearity, sensitivity, and dynamic response of the impedance measuring instruments. The thoracic impedance is modeled as a basal impedance in parallel with a time-varying impedance. At the excitation frequency used in impedance cardiography, the thoracic impedance is generally modeled as purely resistive.

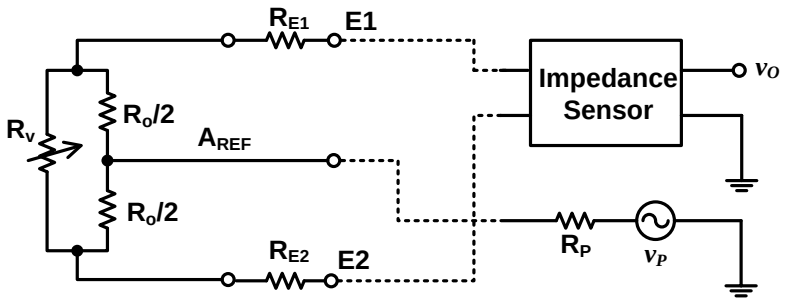
Several circuits have been reported earlier in our lab for implementation of bioimpedance simulators. The impedance simulator developed by Manigandan [13] consisted of an astable multivibrator, manual switches and potentiometer to generate impedance variation in the form of square wave and of desired basal value. Naidu [14] redesigned the hardware using a microcontroller to reduce the wiring. Venkatachalam [15] replaced analog switches with digital potentiometer for obtaining step variation in the resistance. Patil [16] redesigned the simulator to extend the frequency range so that the simulator can be used in the applications of measuring other bio-impedances, e.g., impedance glottography. The simulator redesigned by Desai [8] generated impedance variation in the form of square wave using a microcontroller. The resistance variation was realized using a digital potentiometer and analog switches which were controlled digitally from the microcontroller. All these simulators provide resistance variation in discrete steps. As the signal conditioning and signal processing in many applications involves differentiation of the sensed signal, it is desirable that resistance variation should be in the form of a continuous waveform.

After studying the earlier designs, it has been decided to design a simulator with the following features:

i. Simulated resistance variation with several waveforms (sine, square, typical thoracic impedance waveform) as a continuous function of time,
ii. Wide frequency range of the waveform to extend use of the simulator in several bioimpedance measuring applications such as impedance glottography, peripheral plethysmography, pneumography etc.,
iii. Electrically isolated user interface to set the parameters of the simulator.

The simulator is designed as interconnection of four circuit blocks: resistance variation circuit, controller circuit, serial interface, and power supply. The resistance variation circuit provides time-varying resistance in accordance with sinusoidal or another control waveform,

(a) Bipolar electrode configuration



(b) Tetra-polar electrode configuration

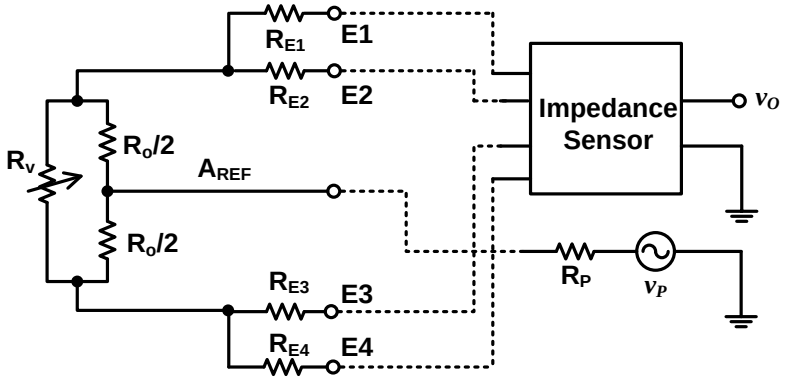


Figure 4.1: Thoracic impedance model [37].

superimposed on a digitally controlled basal resistance. The controller circuit is devised using a microcontroller for digitally setting the basal resistance and generating the analog control waveform for the resistance variation. An isolated serial interface is used for communication between the microcontroller and a PC for setting the simulation parameters: basal resistance, peak resistance variation, waveform, and frequency. These three modules are powered by the power supply circuit.

4.2 Thoracic impedance model

For the purpose of impedance cardiography, the thorax can be modeled as an electrical circuit with a fixed resistance R_o in parallel with a variable resistance R_v. The thoracic impedance model for measurement with an impedance sensor using bipolar electrode configuration is shown in Figure 4.1(a) [37]. The basal component R_o refers to the impedance offered by tissues and fluids located between the measuring points. The time-varying impedance R_v is related to the respiratory and cardiac activities. The basal impedance is the baseline about which the time-varying component fluctuates [1]. The electrode-tissue contact resistances are represented as R_{E1} and R_{E2}. The resistance across E1 and E2 is given as

$$R_{E1E2} = R_o \| R_v + R_{E1} + R_{E2} \tag{4.1}$$

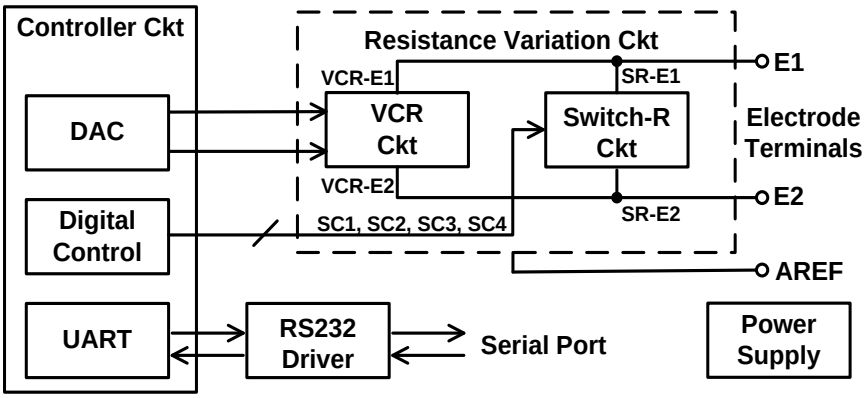


Figure 4.2: Block diagram of bioimpedance simulator.

In an actual bioimpedance measurement, the sensed voltage consists of the voltage across R_{E1E2} due to excitation current and voltages due to various internal bio-signals and external pickups. All such interferences can be modeled as a common mode voltage. It is represented as the voltage v_P in series with resistance R_P between the ground of the impedance sensor and A_{REF}, which is the center point of the resistance R_o. It can be used for assessing common mode interference rejection of the bioimpedance sensor.

The thoracic impedance model for measurement using tetra-polar electrode configuration is given in Figure 4.1(b). It may be noted that it differs only in terms of electrode-tissue contact resistances. There are no differences between the models to be used for measurements using band electrodes, spot electrodes, or array of shorted spot electrodes.

4.3 Bioimpedance simulator realization

The bioimpedance simulator is designed as an interconnection of four circuit blocks: resistance variation circuit, controller circuit, serial interface, and power supply. The block diagram of the bioimpedance simulator is shown in Figure 4.2. The resistance variation circuit consists of a parallel combination of a switch-resistor network for setting the basal resistance R_o and a voltage controlled resistor (VCR) circuit for generating time-varying resistance R_v. The controller circuit is devised for generation of various waves which can be sinusoidal, square, triangular, or a typical thoracic impedance waveform. An isolated serial interface is used for setting the simulation parameters from a PC to the microcontroller. A power supply circuit using low-dropout linear regulators is designed to generate ± 5 V and two 3.3 V supplies from a single input voltage. Each of these blocks is described in the following subsections.

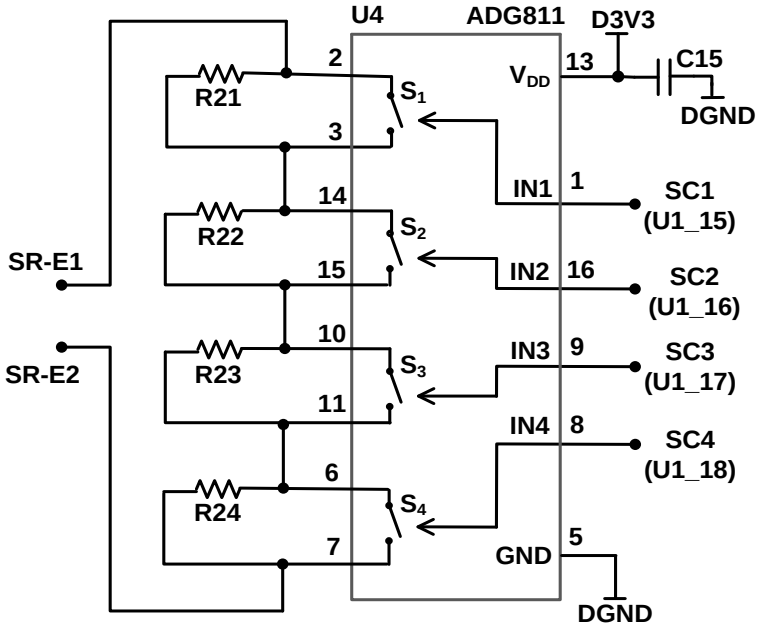


Figure 4.3: Switch-R circuit.

4.3.1 Resistance variation circuit

The variation in resistance is implemented as a parallel combination of a digitally controlled basal resistance and a time-varying resistance realized using a VCR circuit. The digitally controlled basal resistance is realized using a "switch-R" circuit consisting of fixed value resistors and analog switches. The VCR is realized using the JFET-based floating VCR circuit with SD-bootstrapped gate and self-tracking as described in Section 3.4 and shown in Figure 3.12 of the previous chapter.

The switch-R circuit is shown in Figure 4.3. Quad analog switch IC ADG811 (Analog Devices) [38] is used as U4. It is operated at 3.3 V and the control voltage levels are compatible with the 3.3 V logic levels of a microcontroller. Its switches have on-resistance of less than 0.5 Ω. A resistive network with four analog switches and four resistors is used for setting the basal resistance. The values of capacitor C_{15} = 0.1 µF The resistor values used are as the following:

R_{21} = 10 Ω, R_{22} = 20 Ω (two 10 Ω in series), R_{23} = 50 Ω (two 100 Ω in parallel), R_{24} = 100 Ω.

The resistance R_{SW} across the terminals X and Y is given as the following:

$$R_{SW} = S_1 R_{21} + S_2 R_{22} + S_3 R_{23} + S_4 R_{24} \tag{4.2}$$

The switch status (S_1, S_2, S_3, S_4) is 0 if the corresponding switch is closed and 1 if it is open. Different combinations of analog switches $S_1 - S_4$ are used to set different basal resistances, providing 16 resistances with nominal values of 0, 10, 20, 30, 50, 60, 70, 80, 100, 110, 120, 130, 150, 160, 170, and 180 Ω, as shown in Table 4.1 The switch combination is controlled by the controller circuit realized using a microcontroller.

Table 4.1: Nominal values of R_{SW} for different switch combination.

Switch control				Resistance
SC1	SC2	SC3	SC4	R_{SW} (Ω)
0	0	0	0	0
1	0	0	0	10
0	1	0	0	20
1	1	0	0	30
0	0	1	0	50
1	0	1	0	60
0	1	1	0	70
1	1	1	0	80
0	0	0	1	100
1	0	0	1	110
0	1	0	1	120
1	1	0	1	130
0	0	1	1	150
1	0	1	1	160
0	1	1	1	170
1	1	1	1	180

The schematic of the VCR circuit is shown in Figure 4.4. The circuit is implemented using a matched-pair JFET package U441 (Vishay Siliconix) [32] as U5 and op amp IC LT1499 (Linear Technology) [34] as U3. LT1499 is a quad op amp IC with rail-to-rail input and output. It operates with dual-supply having typical current consumption of 6.8 mA [34]. In this application, it is operated at ±5 V. LT1499 is used to generate the gate voltages of the JFETs in the circuit. The voltages v_1 and v_2 are generated by the controller circuit and varied to control the resistance across the terminals X and Y. The values of capacitors and resistors used are as the following:

$C_{12} = C_{13} = C_{39} = 0.1\,\mu\text{F}$

$R_2 = R_3 = 1\ \text{M}\Omega,\ R_4 = R_5 = R_6 = R_7 = 12\ \text{k}\Omega$

$R_8 = 6\ \text{k}\Omega$ (two 12 kΩ resistors in parallel)

$R_{25} = R_{26} = 150\ \text{k}\Omega$.

The terminals SR-E1 and SR-E2 of the switch-R circuit of Figure 4.3 and the terminals VCR-E1 and VCR-E2 of the VCR circuit of Figure 4.4 are connected in parallel to form the terminals E1 and E2 as shown in Figure 4.2. The terminal voltages at E1 and E2must be within the limits for linear operation of the two circuits. For the VCR circuit, this limit is ±1 V with respect to the analog reference terminal marked as AREF. For the switch-R circuit, this limit is the supply voltage of U4 i.e. from 0 to 3.3 V with respect to DGND. The op amp supply voltages marked as A+5V and A−5V are at +5 V and −5 V with respect to AGND, which is shorted to DGND at the power supply ground. Therefore we set the voltage of AREF at half of 3.3 V, i.e. at 1.65 V with respect to AGND. The simulated resistance across the

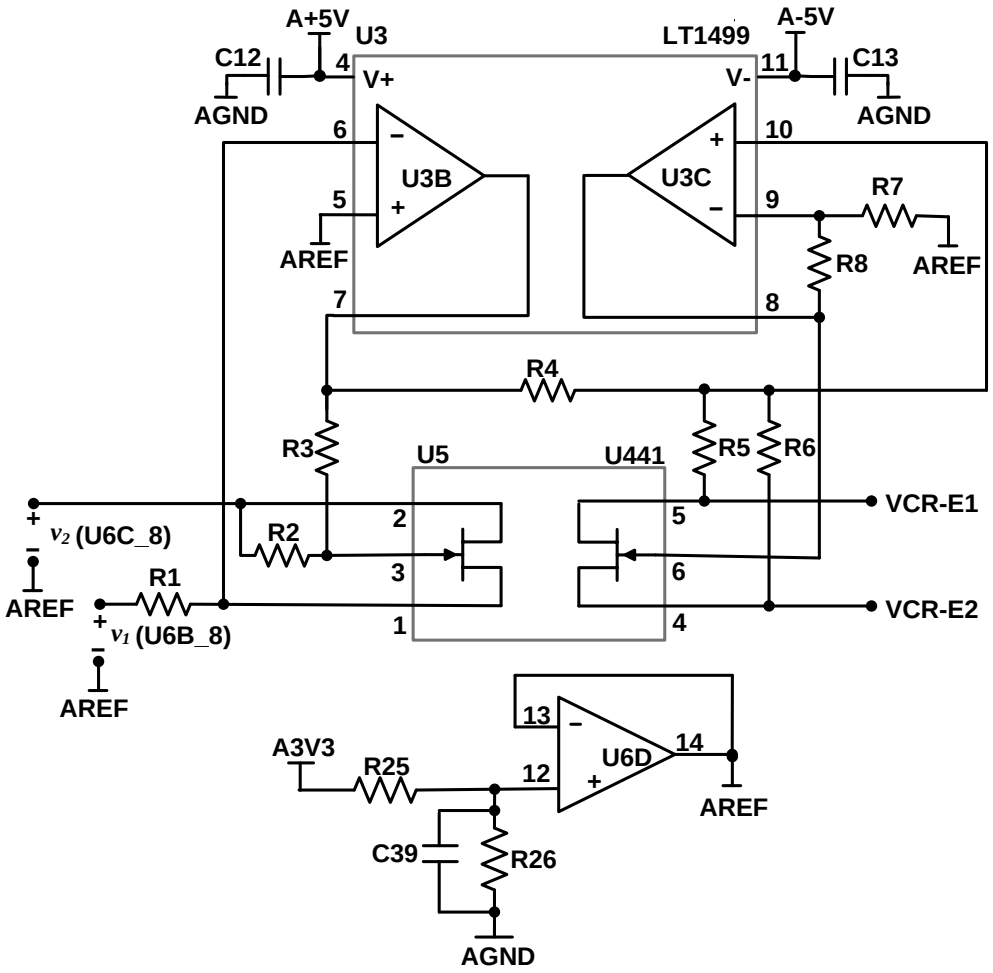


Figure 4.4: VCR circuit implemented using U441 and LT1499.

terminals E1 and E2 has a net linear range of ±1 V with reference to AREF. As the op amps have rail-to-rail input and output voltages, the range for control voltages is [−5 V, +5V] with respect to AGND and it is [−6.65 V, +3.35 V] with respect to AREF. This is compatible with the requirement of negative gate voltages for the JFETs. Analog reference voltage of 1.65V with respect to ground, labeled as AREF, is generated as half of A3V3 and buffered by op amp U6D as shown in Figure 4.4.

4.3.2 Controller circuit

The controller circuit is devised using a microcontroller with on-chip DAC for generating the analog control waveforms for VCR, digital outputs to control the analog switches for setting the basal resistance, serial port for selecting the simulation parameters, and program and data memory and timers for realizing a compact circuit. Figure 4.5 shows the microcontroller connections. Microcontroller DSPIC33FJ128GP802 (Microchip) [39] is used as U1 for generating the control voltage. It is a 16-bit microcontroller having two UART modules, and a DAC module. It can be powered by 3 − 3.6 V supply. In the proposed circuit, it is operated at

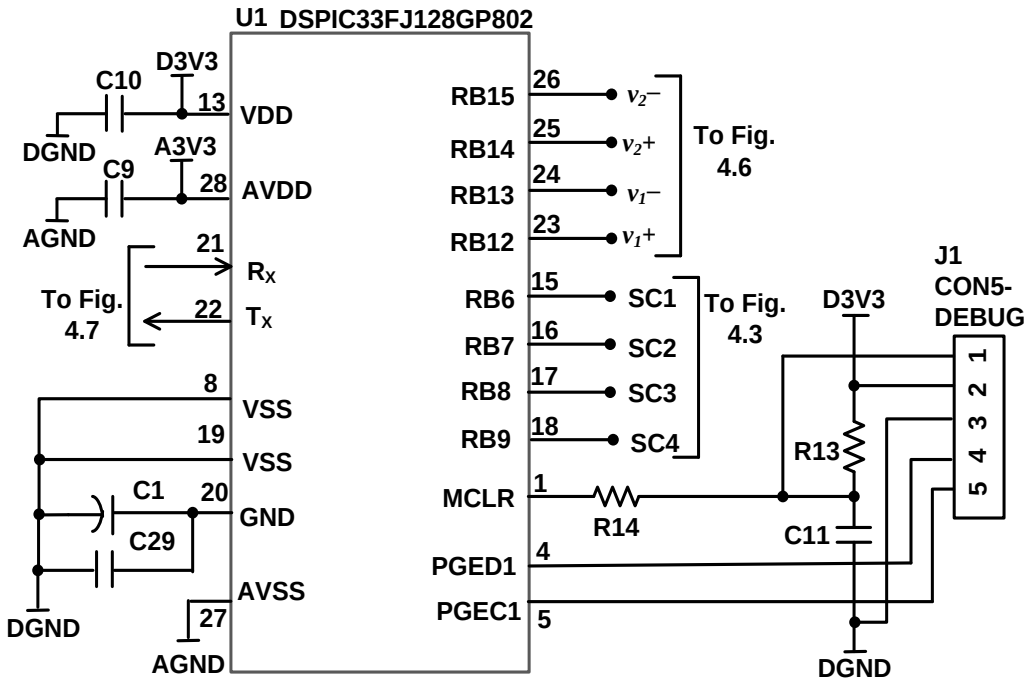


Figure 4.5: Microcontroller connections.

3.3 V. Its internal RC oscillator with PLL is used for generating clock, eliminating the use of external oscillator. The values of capacitor C_{39} = 0.1 μF. The values of R_{13} = 10 kΩ and R_{14} = 100 Ω. The capacitor values used are as the following:

$C_9 = C_{10} = C_{11} = C_{29} = 0.1\,\mu\text{F}$, $C_1 = 10\,\mu\text{F}$.

The microcontroller U1 has a DAC module with two output channels. Each DAC output is a differential output with complementary positive and negative pins, with the range of [1.09 V, 2.36 V]. A differential amplifier is used to generate a single ended output with respect to AREF for providing analog control voltage for VCR. Op amp IC LT1499 (Linear Technology) as U6 is used to implement two differential amplifiers, one for each DAC channel, as shown in Figure 4.6 to provide the control voltages v_1 and v_2. The two outputs are given as the following:

$$v_1 = v_{AREF} + \alpha_1(v_{1-} - v_{1+}) \tag{4.3}$$

$$v_2 = v_{AREF} + \alpha_2(v_{2+} - v_{2-}) \tag{4.4}$$

The resistor values in the circuit are selected to provide differential gain of α_1 for v_1 and α_2 for v_2. The resistors are selected as

$R_{11} = R_{12} = R_{19} = R_{20}$ = 1.2 kΩ,

$R_{15} = R_{16} = R_{17} = R_{18}$ = 0.6 kΩ (two 1.2 kΩ resistors in parallel).

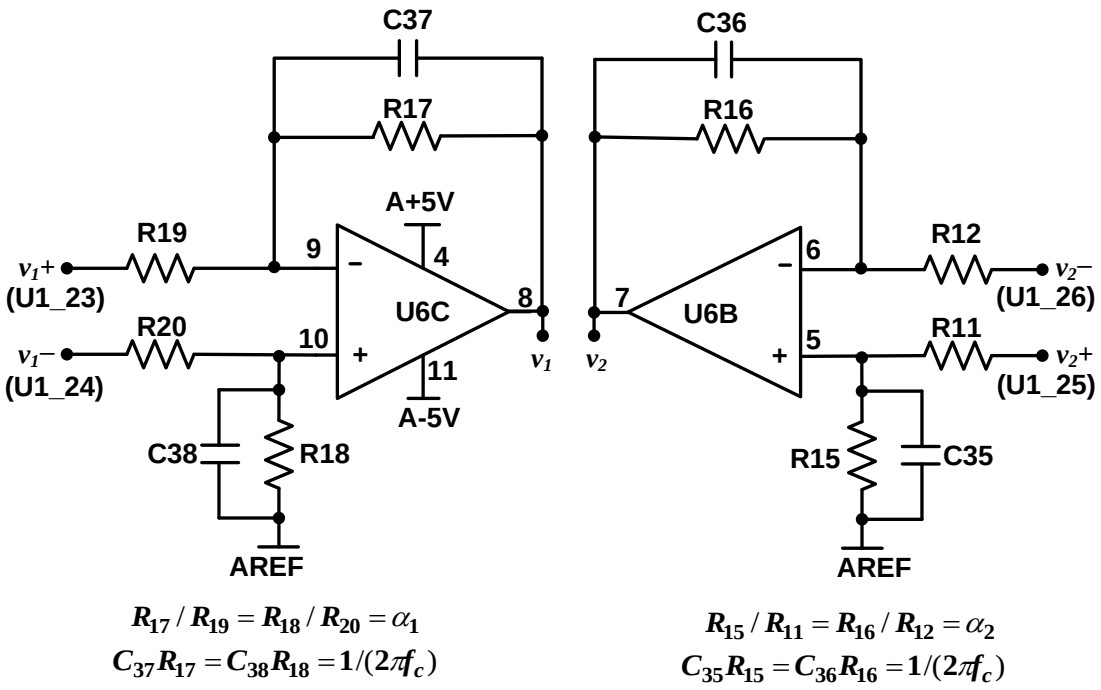


Figure 4.6: Differential amplifiers for generating v_1 and v_2 from the two DAC channels of the microcontroller U1.

To provide α_1 =2 and α_2 = 2. Capacitors in the circuit are selected to provide low-pass filtering. For signal sampling rate of f_s, the DAC channels of U1 use interpolation for outputting at an internal sampling rate of $256f_s$ and therefore a single-order low-pass filter with cutoff f_c of $12.8f_s$ may be considered adequate as a smoothing filter for DAC outputs. In our application, we use sampling frequency of 64 Hz and 6.4 kHz. Therefore, the capacitors are selected of value 0.1µF for $f_c \approx 1.28$ kHz.

4.3.3 Serial interface

An isolated serial interface is used for selecting the simulation parameters in the microcontroller program using a user interface program on a PC. An RS232 line driver is connected to one of the UART modules of the microcontroller for serial communication with a PC. The serial communication between PC and microcontroller is setup using ADM3251E (Analog Devices) as U2. The connection of RS232 line driver is shown in Figure 4.5. The port pin RB.10 of the microcontroller U1 is configured as receiver pin to UART module, while the pin RB.11 is configured as transmit pin from UART.

The single-channel line driver ADM3251E [40] provides isolated RS232 interfacing, with Tin and Rout forming the primary side with microcontroller logic levels and Tout and Rin forming the secondary side with RS232 levels (PC). In addition to isolated line driving, the chip has isolated dc-dc converter for driving the secondary side by using power from the

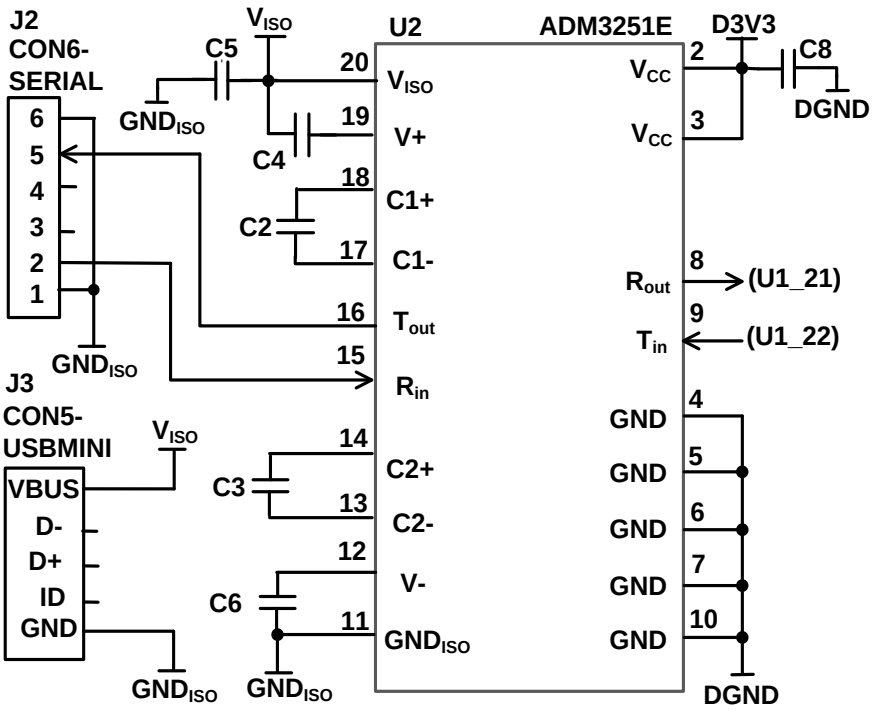


Figure 4.7: Connections of RS232 line driver.

primary side. With its internal isolated dc-to-dc converter enabled, it can be operated at a single supply of 5 V (with current consumption of approximately 110 mA) on the primary side. With power supply of 3.3V on the primary side, its internal dc-to-dc converter remains disabled, and it needs to be powered by an external 5 V. In our application, the driver is powered by 3.3 V (supply current of approximately 2.5 mA) on the primary side and by 5 V (supply current of approximately 12 mA) on the secondary side. Use of external 5 V supply on the secondary side reduces the current requirement on the primary side from 110 mA to 2.5 mA. The secondary side 5 V supply is isolated from the primary side supply and is connected to the pins V_{ISO} and GND_{ISO} through the connector J3 and can be obtained from USB port of the PC. The data transfer from the PC to the microcontroller takes place using connector J2. The capacitor values used are as the following:

$C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = 0.1\,\mu\text{F}$.

4.3.4 Power supply

The three simulator circuit blocks as described in the preceding subsections need ±5 V and 3.3 V supplies. The 3.3 V, 5 V, and −5 V supplies needed for the analog operation are labeled as A3V3, A+5V, and A−5V, respectively and the 3.3 V supply for the digital operations is labeled as D3V3. The microcontroller U1, primary side of RS232 line driver U2, and analog switch IC U4 are powered with D3V3. The op amp ICs U3 and U6 are powered with A+5V and A−5V. The analog part of the microcontroller is powered by A3V3. The current

Table 4.2: Estimation of current consumption for the bioimpedance simulator.

Supply voltage	Component	Current requirement (mA)
D3V3	U1: DSPIC33FJ128GP802	24.0
	U2: ADM3251E	12.0
	U4: ADG811	0.5
	Total	36.5
A3V3	U1: DSPIC33FJ128GP802	5.0
A+5V	U4: LT1499	6.8
	U6: LT1499	6.8
	Total	13.6
A−5V	U4: LT1499	6.8
	U6: LT1499	6.8
	Total	13.6

requirement for these supplies is estimated by considering current requirements by the individual chips and is shown in Table 4.2. The simulator circuit should be isolated from AC mains in order to reduce external pickups. The power supply circuit is designed to work with a single 3.6 V − 5.5 V input supply. It provides the flexibility of powering the circuit from an isolated 5 V supply or a chargeable battery with nominal output of 3.3 to 4.7 V. The secondary side of line driver U2 is powered by a separate external isolated 5 V supply as described earlier.

The power supply circuit is shown in Figure 4.8. It is designed, using a combination of charge-pump based dc-dc converters and linear regulators, to generate regulated outputs of ±5 V as A+5V and A−5V and two 3.3 V as D3V3 and A3V3 from a single 3.6 V − 5.5 V input supply. The analog and digital grounds labeled as AGND and DGND, respectively, are shorted at the negative terminal of the input supply. The capacitor values used are as the following:

$$C_{16} = C_{18} = C_{20} = C_{22} = C_{24} = C_{26} = C_{28} = C_{30} = C_{40} = C_{41} = 0.1\,\mu\text{F}$$

$$C_{19} = C_{23} = C_{27} = C_{31} = C_{32} = C_{34} = 10\,\mu\text{F}$$

The two supplies D3V3 and A3V3 of 3.3 V are obtained using two low-dropout linear regulator ICs MCP1755-3.3 (Microchip) [41] as U7 and U8, respectively. This chip has input voltage range is from 3.6 to 16.0 V and a low quiescent current of 68 µA. To obtain ±5 V, we use charge pump based dc-dc converters followed by linear regulators. The charge pump based converter IC TC962 (Microchip) [43] can work as voltage doubler or inverter with input voltage range is from 3 to 18 V and typical quiescent current of 510 µA. One TC962 as U12 is used as a voltage doubler with the nominal output of $2V_{in}-2V_D$ and labeled as VIN2P. Another TC962 as U13 is used as a voltage inverter with the nominal output of $-(2V_{in}-2V_D)$ and labeled as VIN2N. The supply A+5V of 5 V is obtained by applying VIN2P

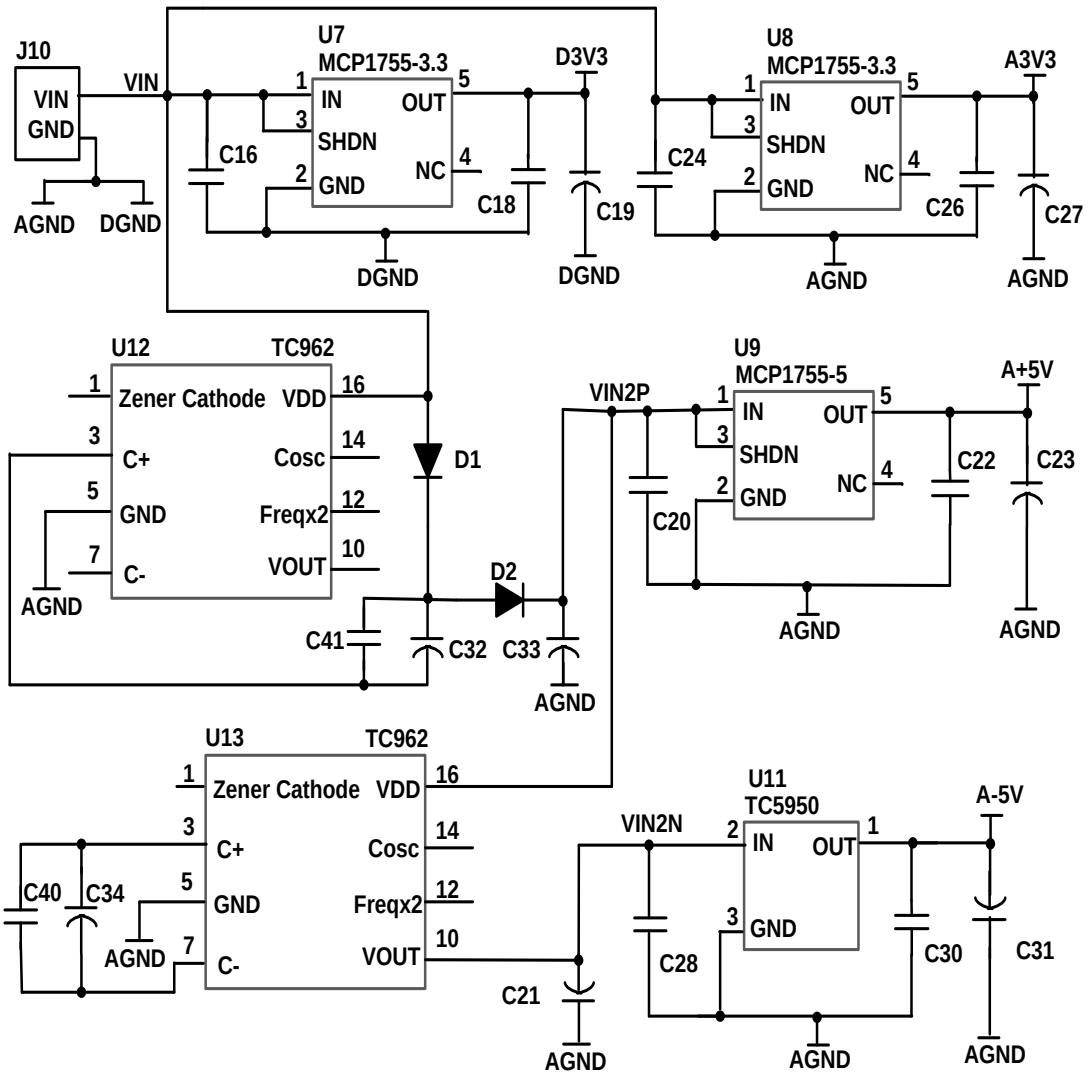


Figure 4.8: Power supply circuit.

as input to a positive low-dropout linear regulator IC MCP1755-5 (Microchip) [41] as U9. Its input voltage range is from 5.5 V to 16.0 V and quiescent current is 68 µA. The supply A−5 V of −5 V is obtained by applying VIN2N as input to a negative low-dropout linear regulator IC TC5950 (Microchip) [42] as U11. Its input voltage range is from −5.6 V to −10 V and quiescent current is 3.5 µA.

4.4 Software

The software has been developed for setting the simulation parameters and generating the resistance variation. It consists of two programs:

i. A PC-based graphical user interface (GUI) program “biosim_gui” to set the simulation parameters and send them using RS232 interface to the microcontroller of the simulator.

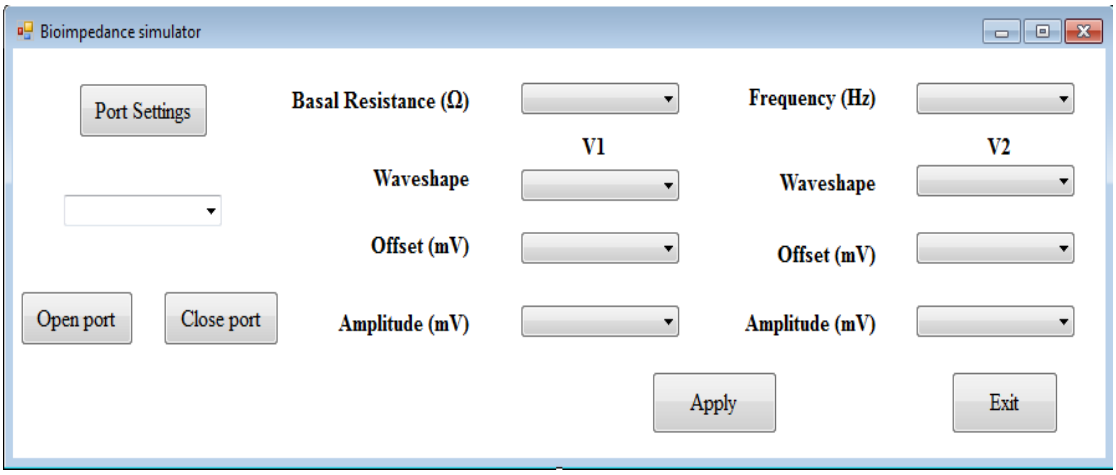
ii. A microcontroller program “biosim_control” to communicate with the PC-based GUI for receiving the simulation parameters and for generating the controls for the resistance variation circuit in accordance with the set parameters.

4.4.1 PC-based GUI

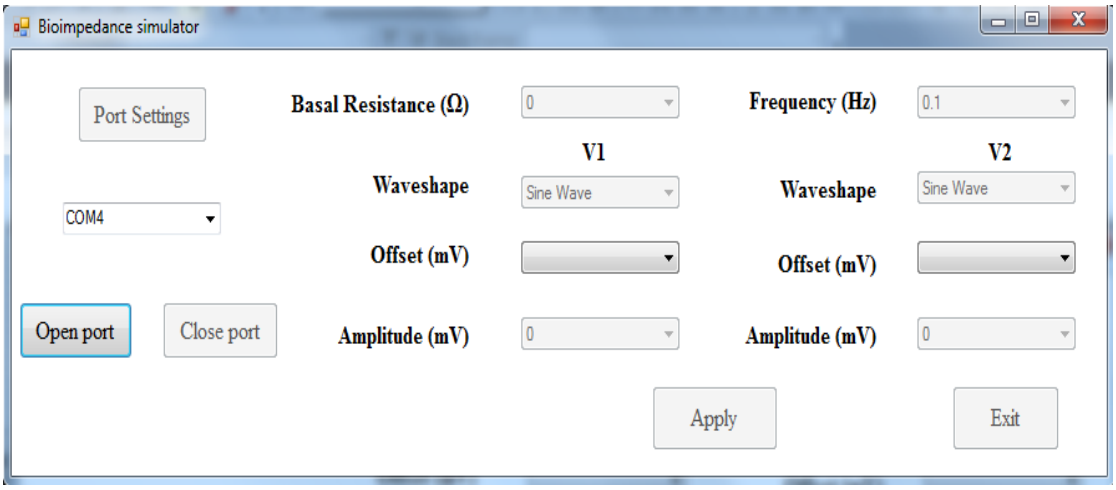
A PC based program “biosim_gui” has been developed using Visual Basic as GUI for setting the simulation parameters of the bioimpedance simulator: basal resistance, frequency of resistance variation, and waveshape, offset, and amplitude of the two resistance control waveforms. The program communicates the parameter values to the controller hardware using RS232 link. For this purpose, a USB-to-RS232 converter is connected to one of the USB ports of the PC. The program is initiated by clicking on the icon for its executable file. The screenshots of the program operation are shown in Figure 4.9. The program detects the USB-to-RS232 converter and displays its port information. Clicking on the “Open port” button configures USB port for serial data transfer at 9600 bits per second. Clicking on “Close port” button releases the port for USB connection. After opening the port for serial communication, the basal resistance and the frequency for time-varying component of the resistance are selected using dropdown menus. In the simulator, the time-varying resistance is controlled by the amplitudes and waveshapes of the control voltages v_1 and v_2, as described in Subsection 4.3.2. The amplitudes and waveshapes of these two voltages are selected by using the corresponding dropdown menus. Clicking on the “Apply” button sends the selected values tothe microcontroller of the simulator via serial port as 8 bytes of data and enables the next cycle of parameter setting. The codes and the corresponding values for the parameters are given in Table 4.3. The program can be stopped by clicking on the “Exit” button which closes the serial port and the interface window.

4.4.2 Microcontroller program

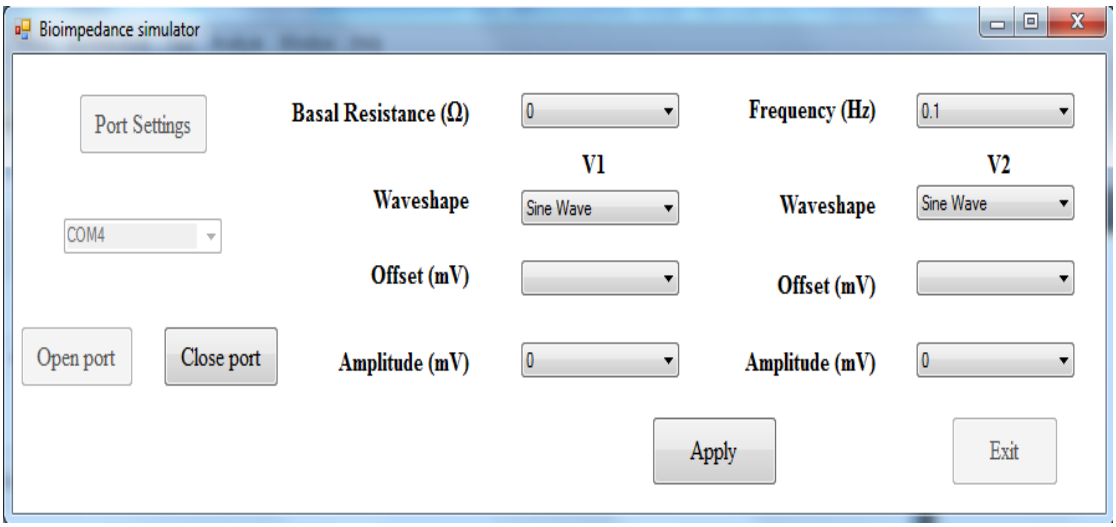
An analog waveform can be generated by outputting its pre-stored digitized samples through a DAC and a smoothening low-pass filter. For outputting a periodic waveform, we need to store samples for one period of the waveform in the memory and output these values using a cyclic address counter. With N_p samples in a period of the waveform and sampling frequency of f_s, the frequency of the resulting waveform is $f_o = f_s/N_p$. If the output waveform has significant components up to frequency f_m, we should have $N_p \geq 2 f_m / f_o$ for a low-distortion waveform. The DAC channels of the microcontroller used in our controller hardware use interpolation for outputting at an internal sampling rate of $256f_s$. Therefore, thecutoff frequency f_c of the smoothening low-pass filter should be selected such that $f_m < f_c < 256f_s - f_m$ and the filter response should ensure that the spectral components of the waveform are not



(a)



(b)



(c)

Figure 4.9: Screenshots of GUI "biosim_gui": (a) Initial screenshot of bioimpedance simulator, (b) Screenshot for opening the port for serial communication, (c) Screenshot for selecting the simulation parameters.

Table 4.3: Control bytes for setting the simulation parameters.

Byte No.	Parameter	Code Values (decimal)	Parameter values
1	Basal resistance (Ω)	0 to15	0, 10, 20, 30, 50, 60, 70, 80, 100, 110, 120, 130, 150, 160, 170, 180
2	Frequency (Hz)	0 to 7	0.1, 0.2, 0.5, 1, 5, 10, 20, 50, 100
3	V1-waveshape	0 to 2	sine, square, thoracic
4	V1-offset (mV), ref.: AREF	0 to 10	0, −100, −200, −300, −400, −500, −600, −700, −800, −900, −1000
5	V1-amplitude (mV)	0 to 10	0, 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000
6	V2-waveshape	0 to 2	sine, square, thoracic
7	V2-offset (mV), ref.: AREF	0 to 10	0, 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000
8	V2-amplitude (mV)	0 to 10	0, 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000

affected and the aliased spectral components at the DAC output get eliminated. In case of a first-order low-pass filter, the roll-off rate is low. Therefore, to get a low-distortion output, we need to select f_c such that $f_m << f_c << 256f_s - f_m$. Since $256f_s >> f_m$, a first-order low-pass filter may be considered adequate as a smoothing filter for DAC outputs if f_c is such that $10f_m < f_c < 25.6f_s$. For a given f_c, f_m and f_s should satisfy the condition that $f_m < f_c/10$ and $f_s > \max(2f_m, f_c/25.6)$. In our circuit, $f_c \approx 1.28$ kHz and therefore $f_m < 128$ Hz and $f_s > \max(2f_m, 50$ Hz).

Waveforms with different frequencies can be generated by outputting the same set of N_p samples at different sampling frequencies, but this may require use of programmable low-pass filters. We can use a fixed-cutoff low-pass filter by keeping f_s constant and changing N_p. However, this requires storing sets of waveforms samples for all the frequencies and thus increases the memory requirement. The memory requirement can be decreased by storing the required samples for the highest output frequency and using interpolation for generating the required number of samples for lower output frequencies. This is the most suitable method used with our controller circuit with a single fixed-cutoff low-pass filter. For waveform generation, the pre-stored samples from the program memory are copied to the data memory. If required, the interpolation is carried out before the waveform generation. While, we can store a large number of waveforms with varying number of samples in the program memory, the data memory size of the microcontroller permits a maximum of 2000 interpolated samples for each of the two DAC channels.

With $f_m/f_o = 32$, we need $N_p \geq 64$. With $f_s = 6.4$ kHz and $N_p = 64$, we can generate waveforms with $f_o = 100$ Hz. With the same sampling frequency and using interpolated samples with N_p up to 640, we get f_o down to 4 Hz. For generating lower frequencies, we need

to use a lower sampling frequency. With f_s = 64 Hz, we can generate frequencies from 1 Hz down to 0.1 Hz. Thus with these two sampling frequencies of 64 Hz and 6.4 kHz, 64 pre-stored samples along with interpolation can be used for generating waveforms over the frequency range from 0.1 Hz to 100 Hz.

The on-chip DAC hardware has 4-sample FIFO buffer for each channel and a default buffer. The on-chip DAC hardware of the microcontroller outputs the samples from the corresponding FIFO buffers to the two DAC channels at the set sampling frequency. In case the FIFO buffers get empty, the value in the default buffer is output to both channels. The sampling frequency is programmed by writing to its control register and is derived from the master clock. Use of FIFO buffers facilitates a jitter-free output through the DAC channels at the programmed sampling rate, provided writing to the DAC FIFO buffers is carried out in such a manner that they do not get empty.

As described in Subsection 4.3.2, the control operations of the impedance simulator are handled through four digital control outputs and two DAC channels of the microcontroller DSPIC33FJ128GP802 as U1 in Figure 4.5. For these operations, the microcontroller program "biosim_control" is written in embedded C using "Microchip MPLAB IDE®". The program is subdivided into a main program and three interrupt service routines (ISR): "U1RXInterrupt" ISR for servicing the UART interrupt and receiving the simulation parameters, "DAC1LInterrupt" ISR for handling the left DAC channel interrupt, and "DAC1RInterrupt" ISR for handling the right DAC channel interrupt. The main program has an initialization part followed by outputting the waveform samples from both DAC channels in a cyclic manner. It is done by writing to the DAC data buffer of each channel. The two DAC ISRs are invoked by corresponding DAC interrupts which are triggered by writing to the corresponding DAC buffers. The writing to DAC is followed by a loop for waiting for a new set of simulation parameters to be received over the serial port, setting the selected parameters, and calculating the samples of the two selected waveforms at the set frequency from the pre-stored samples. The tasks of receiving the simulation parameters over the serial port and outputting the waveform samples through the DAC channels are handled by interrupt service routines. The U1RXInterrupt ISR is invoked by UART interrupt. It receives the parameter values over the serial port and returns with "`uart_flag`" set to indicate to the main program that a new set of parameters have been received.

A flowchart of the main program is given in Figure 4.10. The main program starts with setting the system clock. The microcontroller has internal power-on reset and starts with internal default oscillator as the clock source. The microcontroller master clock is configured at f_{clk} of 37 MHz. The program initializes the DAC module, UART module, and input/output

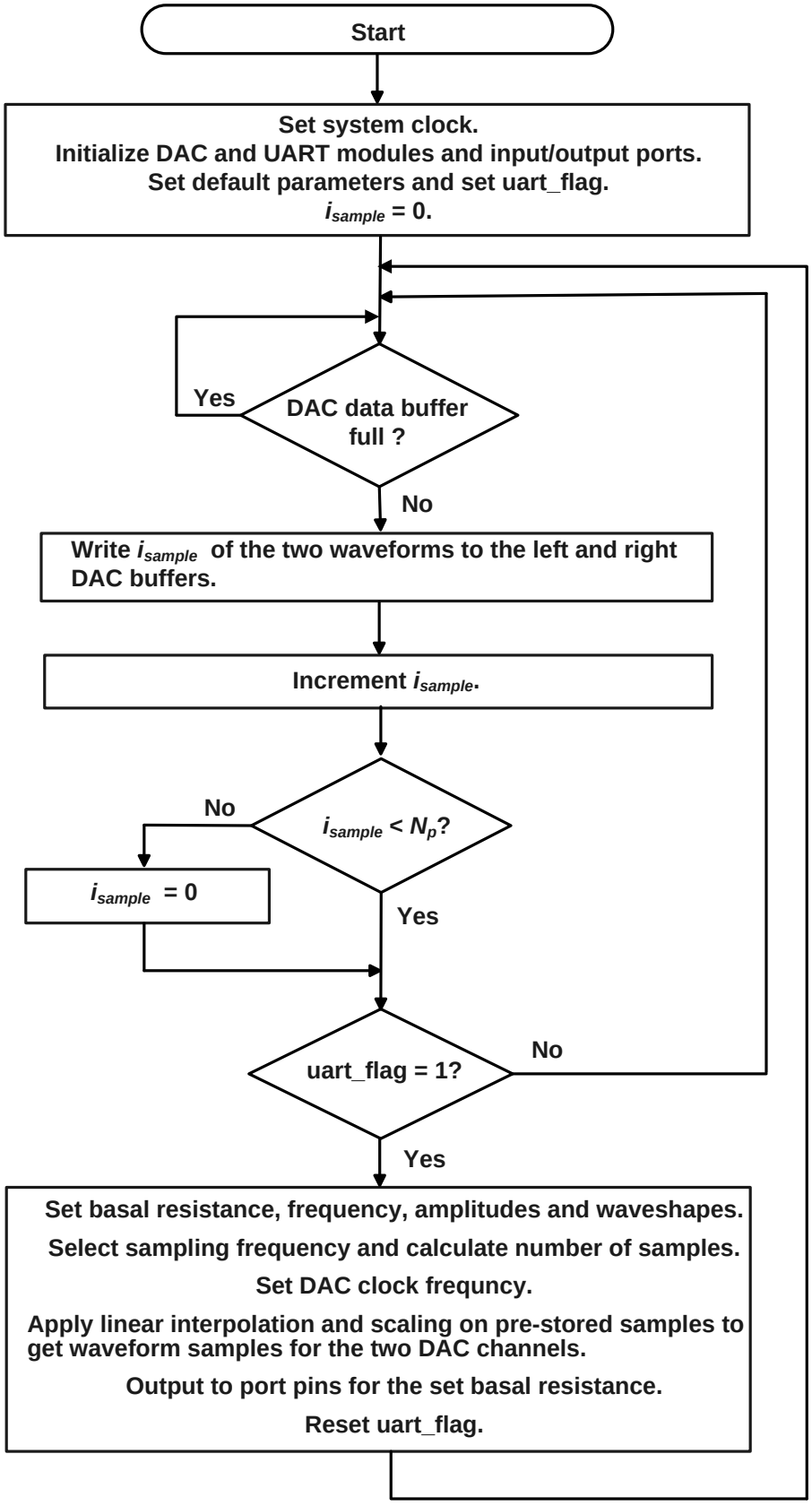


Figure 4.10: Flow chart of the main program of "biosim_control".

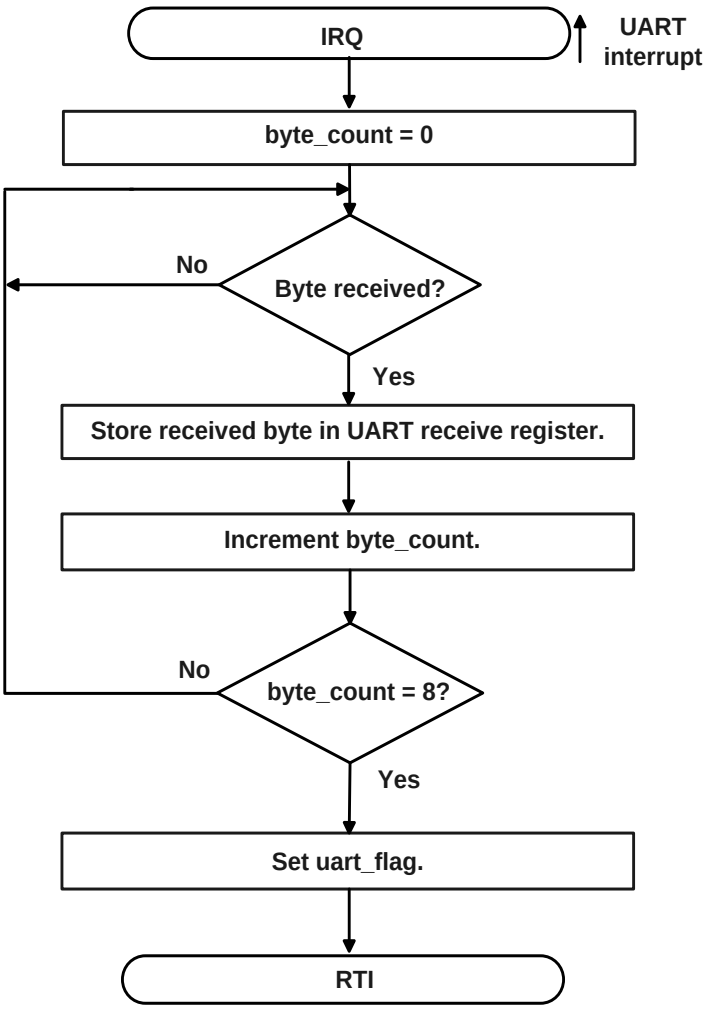


Figure 4.11: Flow chart for U1RXInterrupt ISR of biosim_control.

ports by loading the appropriate TRIS and PORT registers. The default simulation parameters are set as the following:

Basal resistance: 100 Ω, Frequency: 10 Hz,

V1-waveshape: sine, V1-offset: 1000 mV (ref: AREF), V1-amplitude: 0 mV

V2-waveshape: sine, V2-offset: 1000 mV (ref: AREF), V2-amplitude: 0 mV

The control waveforms can be generated through DAC channels by outputting the waveform samples in a cyclic manner. It is carried out by writing to each of the DAC data buffers of corresponding channels. If the buffers are full, then the program waits for DAC buffers to have space to store one sample. The program then checks for `uart_flag`. If the flag is not set, checking is repeated after writing to the DAC data buffers. If the flag is found to be set, it indicates that a new set of simulation parameters have been received over the serial port. These new parameters corresponding to the basal resistance, frequency, two waveshapes, and two amplitudes are loaded for control operations. Depending on the frequency, the sampling rate is selected as f_s = 64 Hz for $f_o \leq$ 1 Hz and 6.4 kHz otherwise. The number of samples is

calculated and DAC clock frequency is set according to the selected sampling frequency. The sets of samples of the two selected waveshapes are taken from the program memory and the sets of samples corresponding to the current frequency and sampling rate are obtained from the stored samples using linear interpolation. The samples are scaled in accordance with the corresponding amplitudes and stored as waveform samples for outputting through the DAC channels. Basal resistance is set by outputting to the corresponding port pins. The `uart_flag` is reset. The cycle is repeated by writing to the DAC data buffers followed by checking for `uart_flag`.

The interrupt service routine U1RXInterrupt ISR is invoked by UART interrupt. Its flowchart is shown in Figure 4.11. It checks for `uart_flag`. 8 bytes of the data are received one-by-one from PC-based GUI over the serial port, `uart_flag` is set, and a return to the main program is executed. It may be noted that operation of writing to DAC buffers gets suspended during the data reception, and therefore DAC channels output default sample values during this period.

Writing to each DAC data register invokes a DAC interrupt and these interrupts result in invoking of the corresponding ISR: DAC1LInterrupt for the left channel DAC interrupt and DAC1RInterrupt for the right channel DAC interrupt. Each ISR clears the corresponding interrupt flag and returns back.

Chapter 5
TEST RESULTS

5.1 Introduction

The bioimpedance simulator provides a time-varying resistance in the form of a small variation in resistance superimposed on a basal resistance. The testing of the bioimpedance simulator was done in two stages. The first stage involved testing of the waveform generation using the on-chip DAC of the microcontroller U1 of the controller circuit. The second stage was carried out to test the resistance variation circuit by providing the generated waveform as control voltages. The simulation parameters in both the cases were set using PC-based GUI.

5.2 Test results for the waveform generation circuit

The operation of the bioimpedance is controlled by setting the simulation parameters for controlling the basal resistance, frequency, and waveshape, offset, and amplitude of the two control waveforms. The basal resistance is controlled by the digital port pins of the microcontroller and the control voltages are generated through its DAC channels. The selectable parameter values are given in Table 4.3 of the fourth chapter.

The levels on the four digital control lines for controlling the analog switches for changing the basal resistance were verified by setting the different values from the GUI. Operation of the DAC channels for generation of the control waveforms for different settings was tested by observing the waveforms using a CRO and the waveforms were found to be jitter-free. The output waveforms v_1 and v_2 are shown in Figures 5.1 − 5.3 for different combinations of frequency (0.1, 10, 100 Hz), waveshapes (sine, square, thoracic), offset (0, 1000 mV ref: AREF), amplitude (0, 500, 1000 mV).

5.3 Test results for the resistance variation circuit

The testing of the resistance variation circuit was done in two phases. In the first phase, the values of the basal resistance as provided by the switch-R network in response to the digital controls from the microcontroller were measured. The second phase involved testing of the VCR circuit for the time-varying resistance. The operations of these circuits were tested independently without connecting them in parallel.

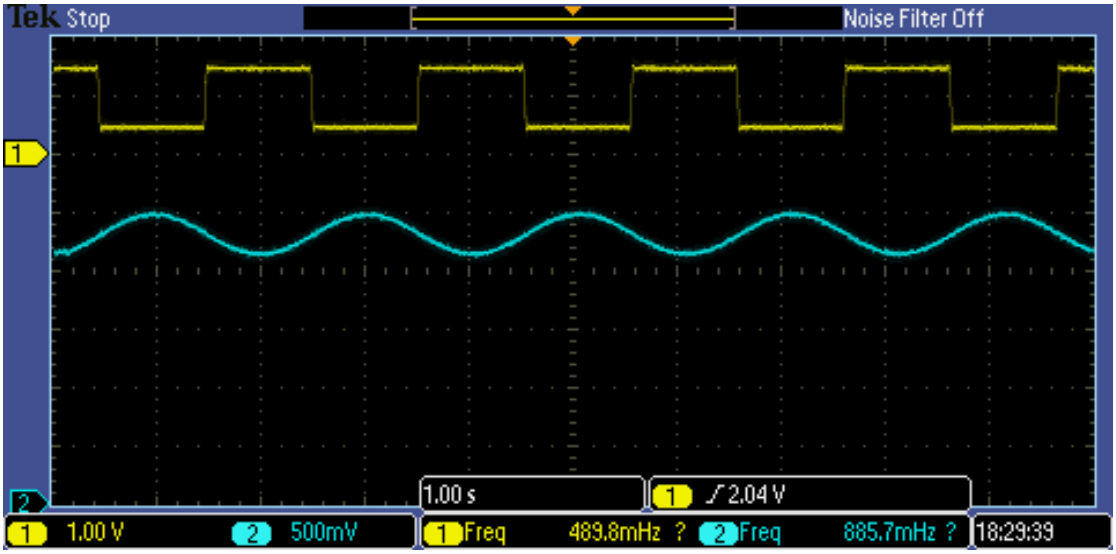


Figure 5.1: Output waveforms v_1 (Ch. 1) and v_2 (Ch. 2) for f = 0.1 Hz, v_1 :1 V offset and 1 V p-p square wave, v_2 : 0 V offset and 0.5 V p-p sine wave.

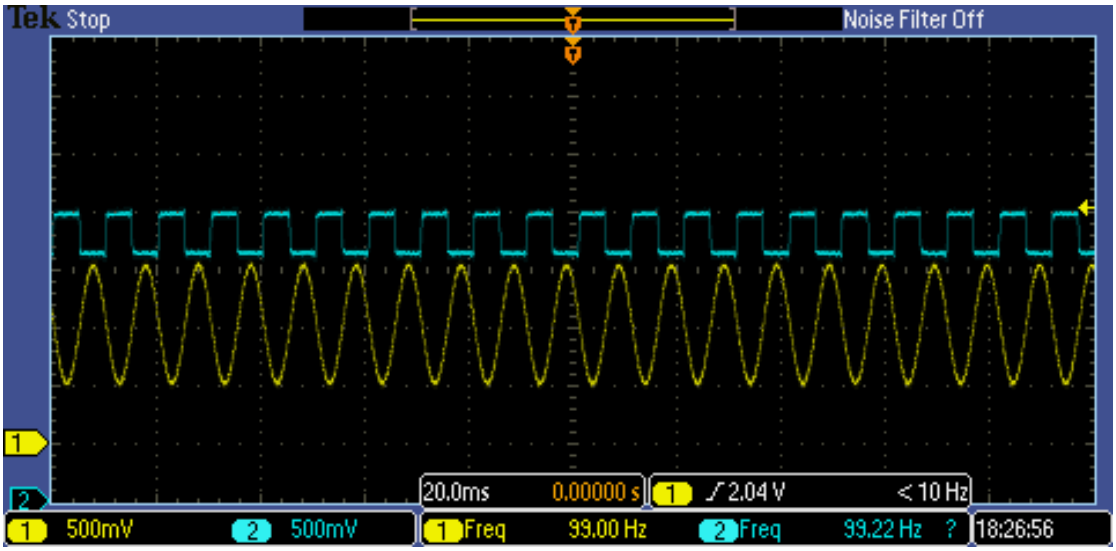


Figure 5.2: Output waveforms v_1 (Ch. 1) and v_2 (Ch. 2) for f = 100 Hz, v_1 : 0 V offset and 1 V p-p sine wave, v_2 : 0 V offset and 0.5 V p-p square wave.

The measured values of the digitally controlled basal resistance are given in Table 5.1 along with the corresponding nominal values, and the calculated values (calculated from the measured values of actual resistance values in switch-R circuit: R_{21} = 10.0 Ω, R_{22} = 19.8 Ω, R_{23} = 49.5 Ω, R_{24} = 100.1 Ω). The deviations of the measured values from the calculated values are as expected due to on-resistance (<0.5 Ω) of the analog switches.

For measuring the time-varying resistance of the VCR circuit, dc voltage were applied across the X and Y terminals: v_Y was kept at 0 (ref: AGND) and v_X was varied with respect to AGND. The voltage-to-current converter, as shown in Figure 3.24 was used with R_Y = 10 kΩ. It gives the output $v_{OUT} = -i_X R_Y$ and thus $v_{OUT} = -v_X R_Y / R_{XY}$. The

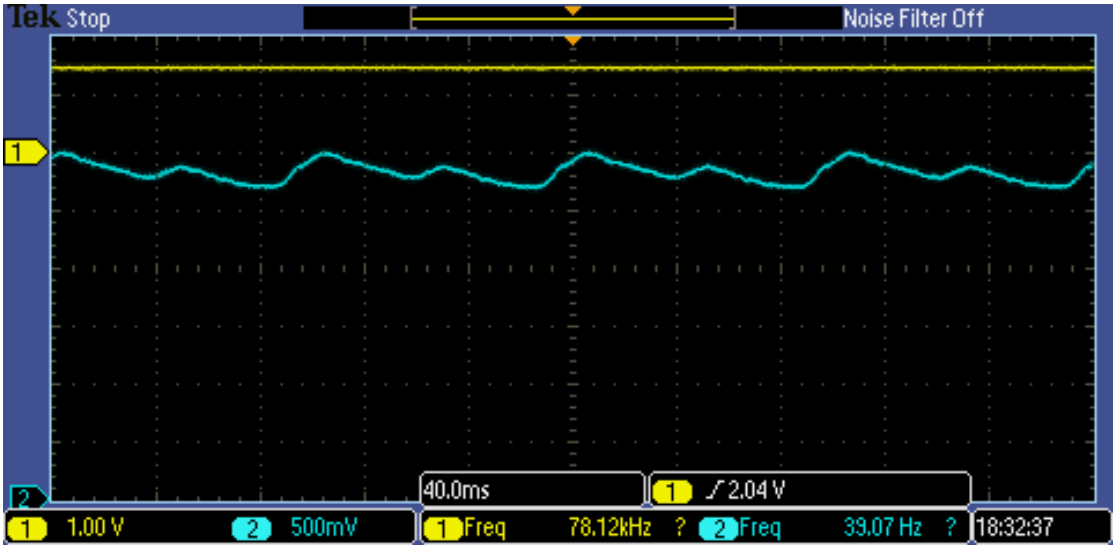


Figure 5.3: Output waveforms v_1 (Ch. 1) and v_2 (Ch. 2) for f = 10 Hz, v_1 : −0 V dc, v_2 : 1 V offset and 0.5 V p-p thoracic wave.

Table 5.1: Values (Ω) of the basal resistance of the digitally controlled switch-R circuit.

Nominal	Calculated	Measured
0	0	3.1
10	10.0	11.8
20	19.8	22.5
30	29.8	32.8
50	49.5	52.3
60	59.5	62.7
70	69.3	71.3
80	79.3	81.4
100	100.1	102.6
110	110.1	112.0
120	119.9	121.9
130	129.9	131.6
150	149.6	151.2
160	159.6	160.9
170	169.4	170.4
180	179.4	180.7

resistance of the VCR circuit is $R_{XY} = R_1 v_2 /(-v_1)$. Therefore $v_{OUT} = v_X (R_Y / R_1)(v_1 / v_2)$.

The circuit was tested with R_1 = 2.34 kΩ (set using a pot). The control waveforms v_1 and v_2 were generated by the DAC channels of the microcontroller by selecting the corresponding parameters from the GUI. For testing the VCR operation, several combinations of v_1 and v_2 were selected and the control waveforms and the resulting output v_{OUT} were observed. The output waveforms were found to be as expected. The waveforms recorded using a DSO for a few representative cases are shown in Figures 5.4 − 5.7 and described below. It may be noted that the settings for the control waveforms v_1 and v_2 are with respect

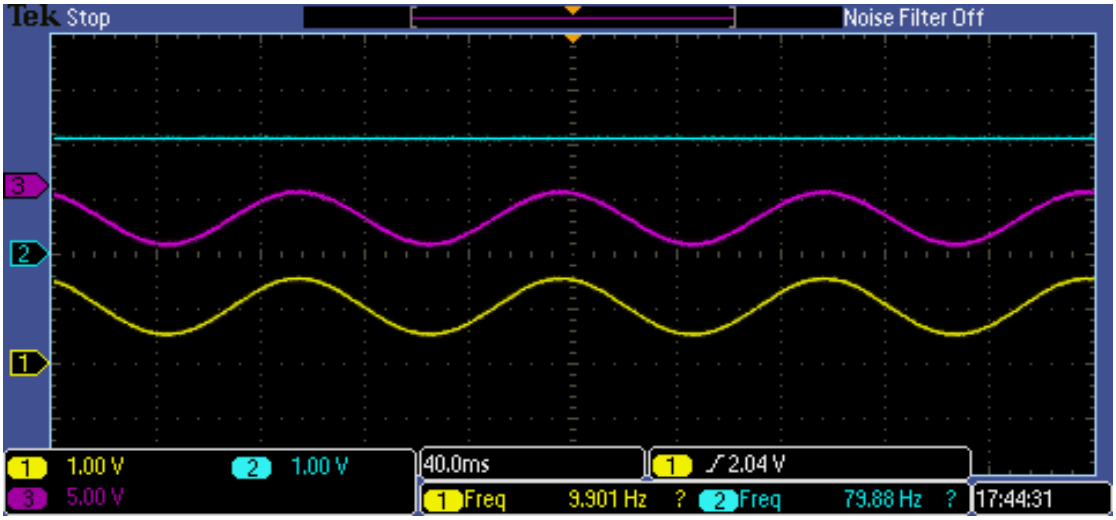


Figure 5.4: Output waveforms v_1 (Ch. 1), v_2 (Ch. 2), and v_{OUT} (Ch. 3) for f = 10 Hz, v_X = 0.5 V, v_1 : −0.8 V offset (0.85 V w.r.t. AGND) and 1 V p-p sine, v_2 : 0.4 V dc (2.05 V w.r.t. AGND).

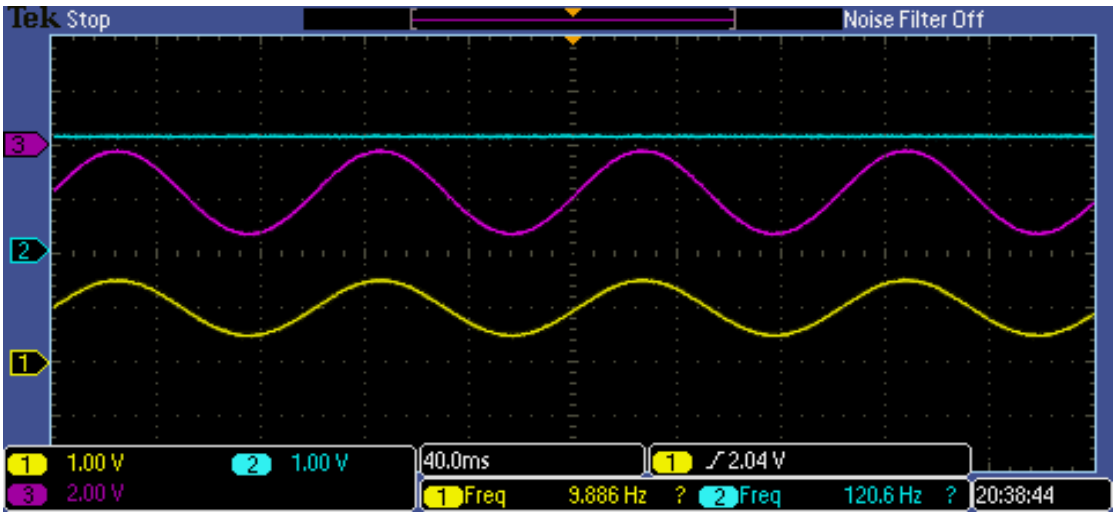


Figure 5.5: Output waveforms v_1 (Ch. 1), v_2 (Ch. 2), and v_{OUT} (Ch. 3) for f = 10 Hz, v_X = 0.3 V, v_1 : −0.8 V offset (0.85 V w.r.t. AGND) and 1 V p-p sine, v_2 : 0.4 V dc (2.05 V w.r.t. AGND).

to AREF (1.65 V w.r.t. AGND) and v_{OUT} is with respect to AGND. All the waveforms on DSO were observed with respect to AGND.

For the waveforms in Figure 5.4, v_1 was set as a 1 V p-p sine with −0.8 V offset and v_2 was set as a dc voltage of 0.4 V. This combination of v_1 and v_2 with v_X = 0.5 V, R_1 = 2.34 kΩ, and R_Y = 10 kΩ corresponds to v_{OUT} being a 2.67 V p-p sine with offset of −4.27 V. Changing v_X resulted in dc offset and p-p value of v_{OUT} getting proportionately changed without any change in its waveshape, showing that R_{XY} remained constant. Figure 5.5 shows such an example with v_X = 0.3 V. This combination corresponds to v_{OUT} being a 1.60 V p-p sine with offset of −2.56 V.

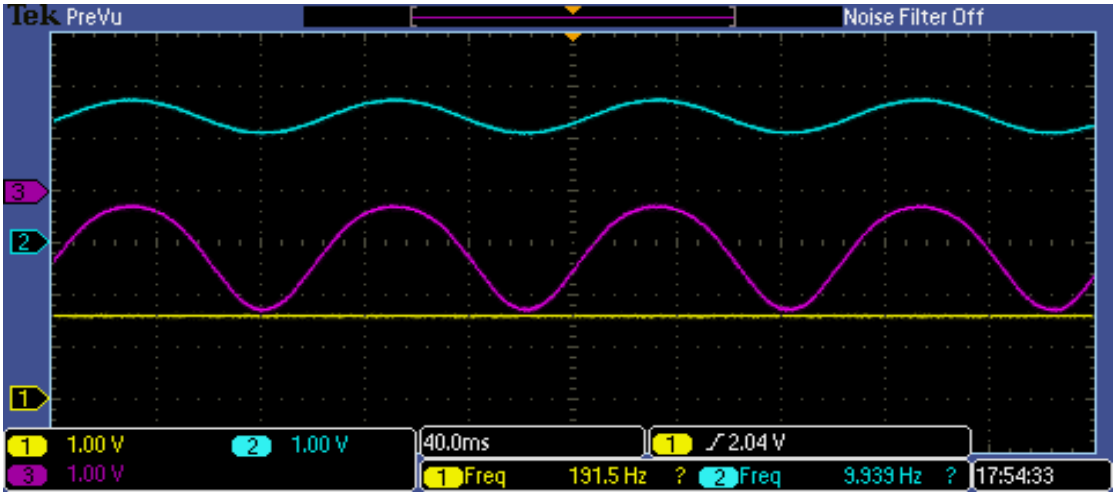


Figure 5.6: Waveforms v_1 (Ch. 1), v_2 (Ch. 2), and v_{OUT} (Ch. 3) for f = 10 Hz. v_1: −0.1 V dc (1.55 V w.r.t. AGND), v_2: 0.4 V offset (2.05 V w.r.t. AGND) and 0.4 V p-p sine.

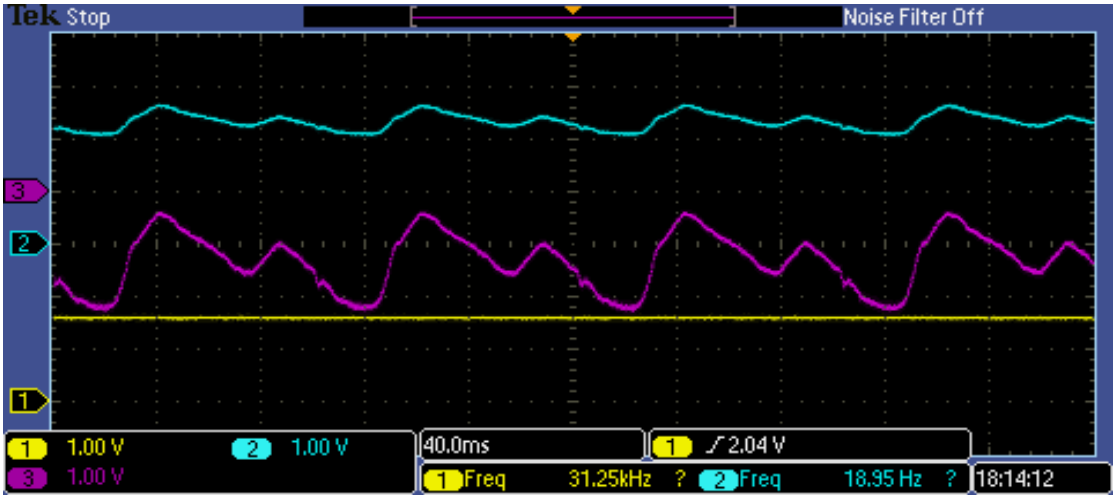


Figure 5.7: Waveforms v_1 (Ch. 1), v_2 (Ch. 2), and v_{OUT} (Ch. 3) for f = 10 Hz. v_1: −0.1 V dc (1.55 V w.r.t. AGND), v_2: 0.4 V offset (2.05 V w.r.t. AGND) and 0.4 V p-p thoracic wave.

For the waveforms in Figure 5.6, v_1 was set as a −0.1 V dc and v_2 was set as a 0.4 V offset with 0.4 V p-p sine wave. This combination of v_1 and v_2 with v_X = 1 V, R_1 = 2.34 kΩ, and R_Y = 10 kΩ corresponds to v_{OUT} having an offset of −1.07 V and a distorted sine.

For the waveforms in Figure 5.7, v_1 was set as a −0.1 V dc and v_2 was set as a 0.4 V offset with 0.4 V p-p thoracic wave. This combination of v_1 and v_2 with v_X = 1 V, R_1 = 2.34 kΩ and R_Y = 10 kΩ corresponds to v_{OUT} being a thoracic wave with offset on −1.07 V.

Chapter 6
SUMMARY AND CONCLUSIONS

The project objective was to develop a bioimpedance simulator for testing and calibrating the impedance measuring instruments. As these instruments generally have a differentiator as part of their signal conditioning circuit, the simulated impedance should not have discrete steps and there should be provision for selecting different test waveforms. To meet this requirement, a bioimpedance simulator has been developed for generating an arbitrary analog waveform as resistance variation. It has four circuit blocks: resistance variation circuit, controller circuit, serial interface, and power supply circuit. The resistance variation circuit is implemented as a parallel combination of a digitally controlled basal resistance obtained using analog switches and a time-varying resistance generated using a VCR circuit.

After studying earlier VCR circuits, an analysis of several JFET and MOSFET-based VCR circuits has been carried out. By simulation and practical measurements, it has been shown that a matched-pair JFET-based circuit with SD-bootstrapped gate and self-tracking can be used to get a floating VCR for linear operation over an extended range of terminal voltages and to make its resistance independent of the device parameters within certain operational constraints. It is further shown by circuit simulation that a matched-pair MOSFET-based circuit with SD-bootstrapped gate, S-bootstrapped substrate, and self-tracking can be used for the same purpose. The MOSFET based circuit could not be practically tested due to unavailability of matched-pair MOSFETs with independent substrates.

The VCR circuit realized using n-channel matched-pair JFET has been used in the bioimpedance simulator. The controller circuit is devised using a microcontroller with on-chip DAC for generating the analog control waveforms for obtaining the time-varying resistance, digital outputs to control the analog switches for setting the basal resistance, and serial port for selecting the simulation parameters. An isolated serial interface is used for selecting the simulation parameters in the microcontroller program using a user interface program on PC. The power supply circuit has been designed and tested using charge-pump based converters and linear regulators to power the analog and digital blocks of the simulator from a single 3.6 − 5.5 V voltage.

Operation of the controller and the resistance variation circuit along with the serial interface for setting the simulation parameters has been extensively tested and verified. The

simulator needs to be tested by measuring its basal and time-varying resistances by a few commercially available impedance cardiographs.

APPENDIX A

Schematic of bioimpedance simulator

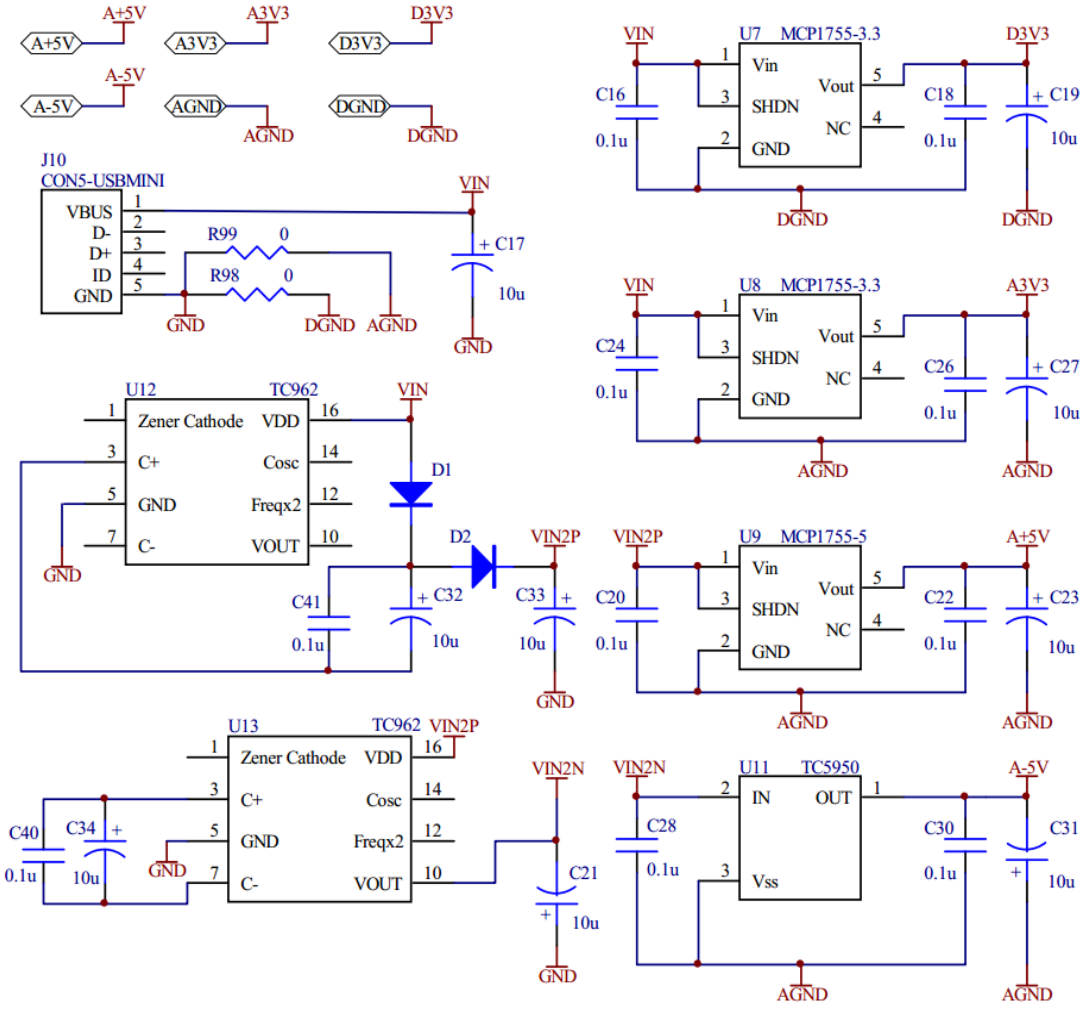


Figure A.1: Power supply circuit.

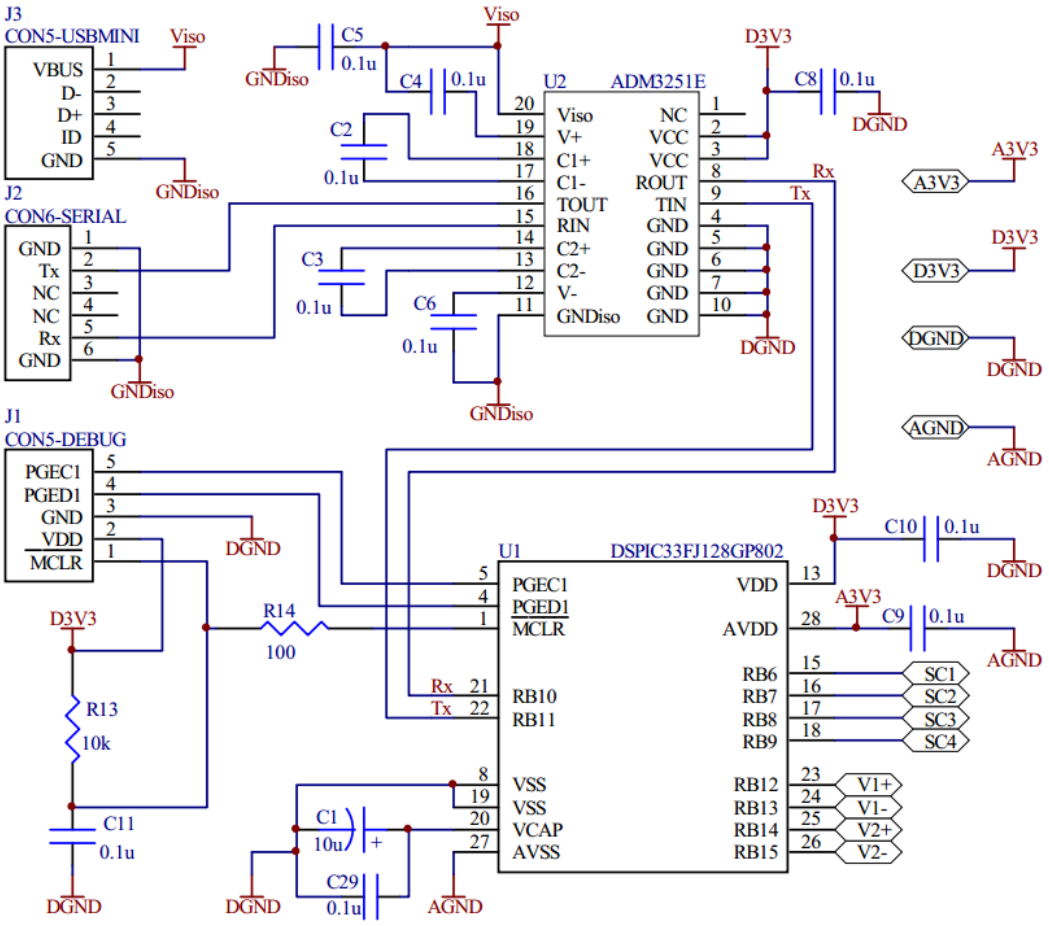


Figure A.2: Controller circuit.

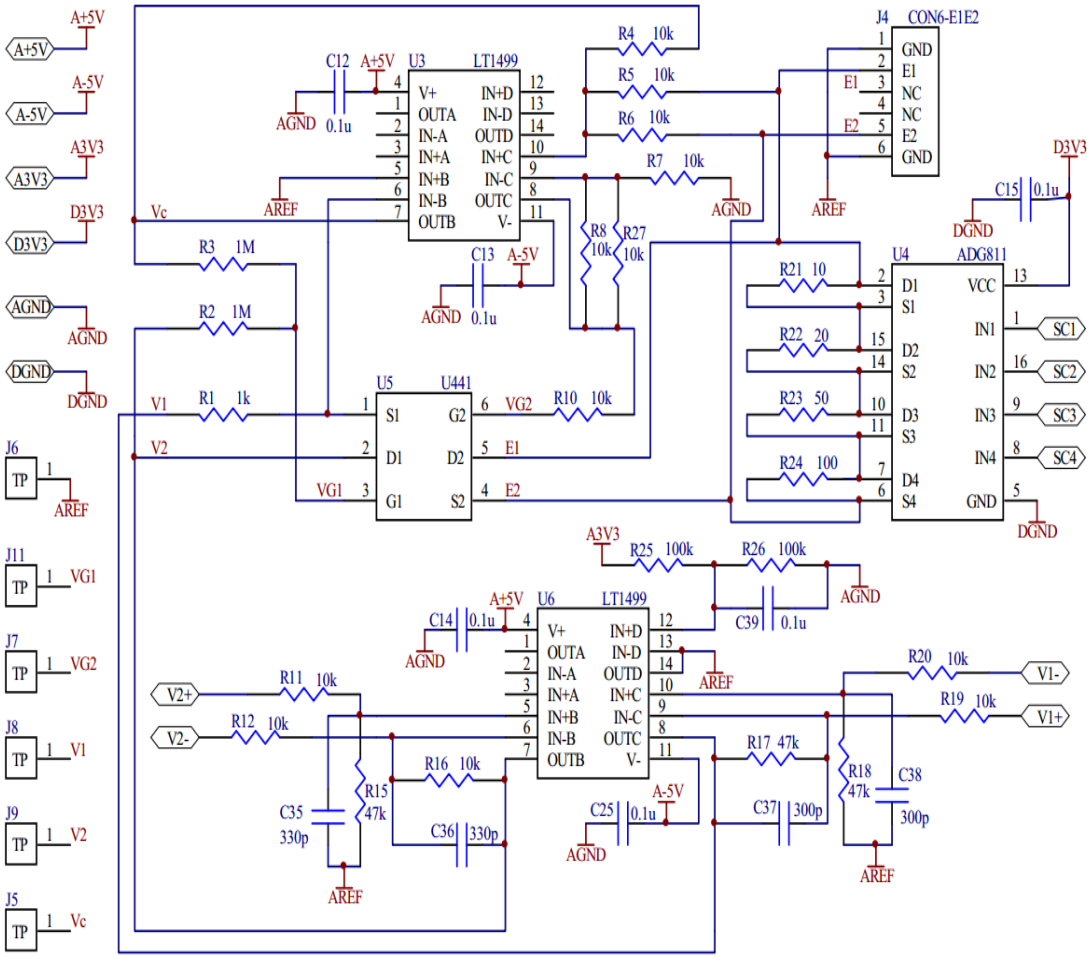


Figure A.3: VCR circuit.

APPENDIX B

PCB layout of bioimpedance simulator

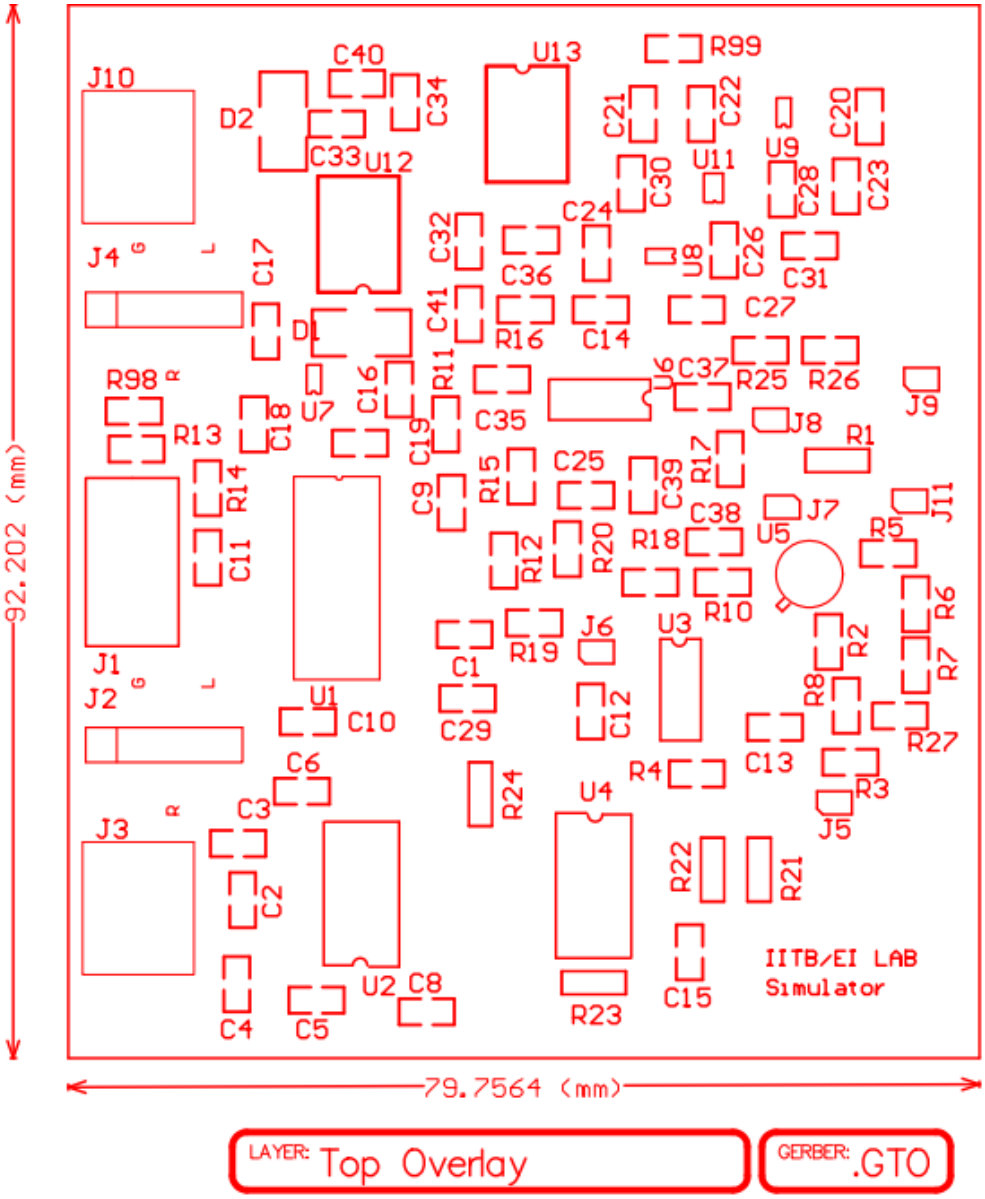


Figure B.1: Top overlay of PCB.

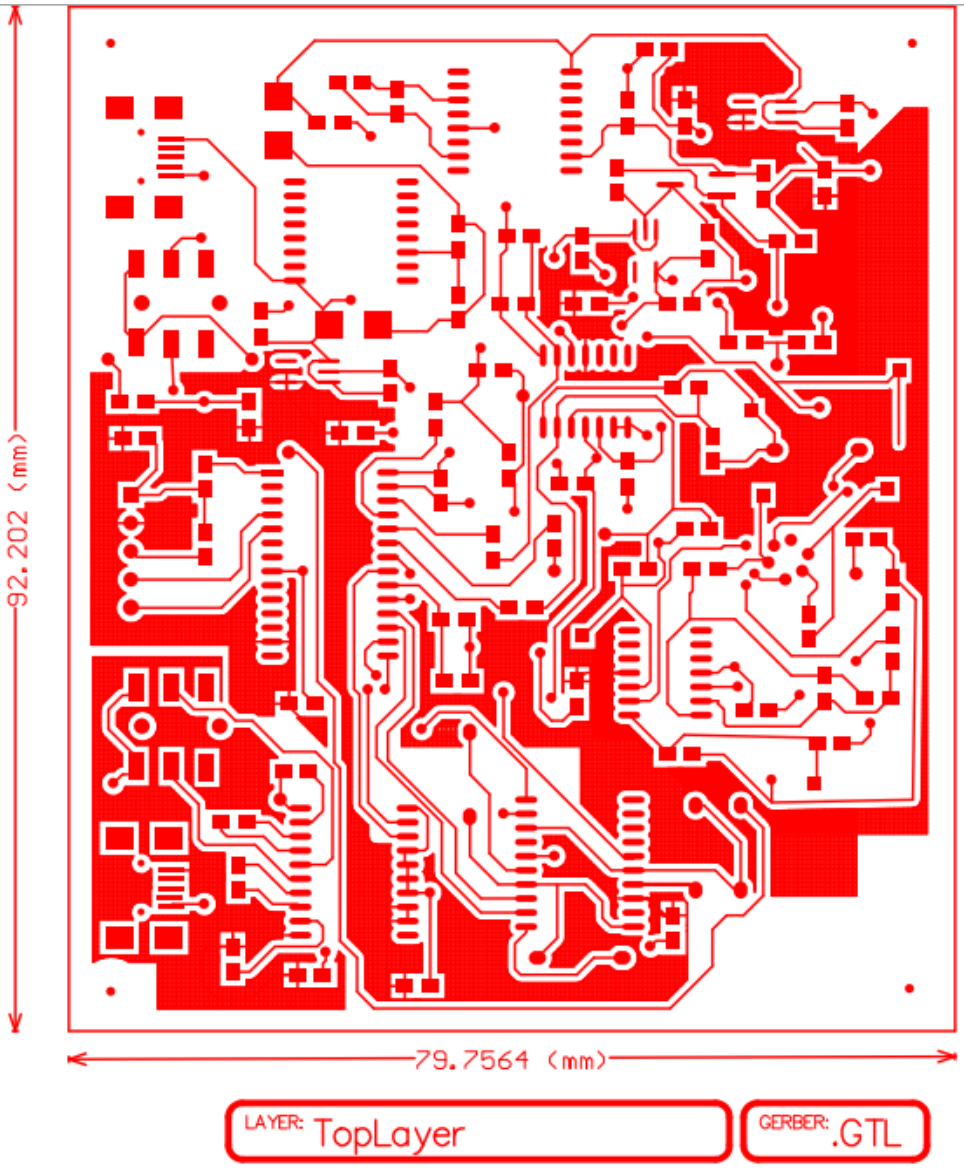


Figure B.2: Top layer of PCB.

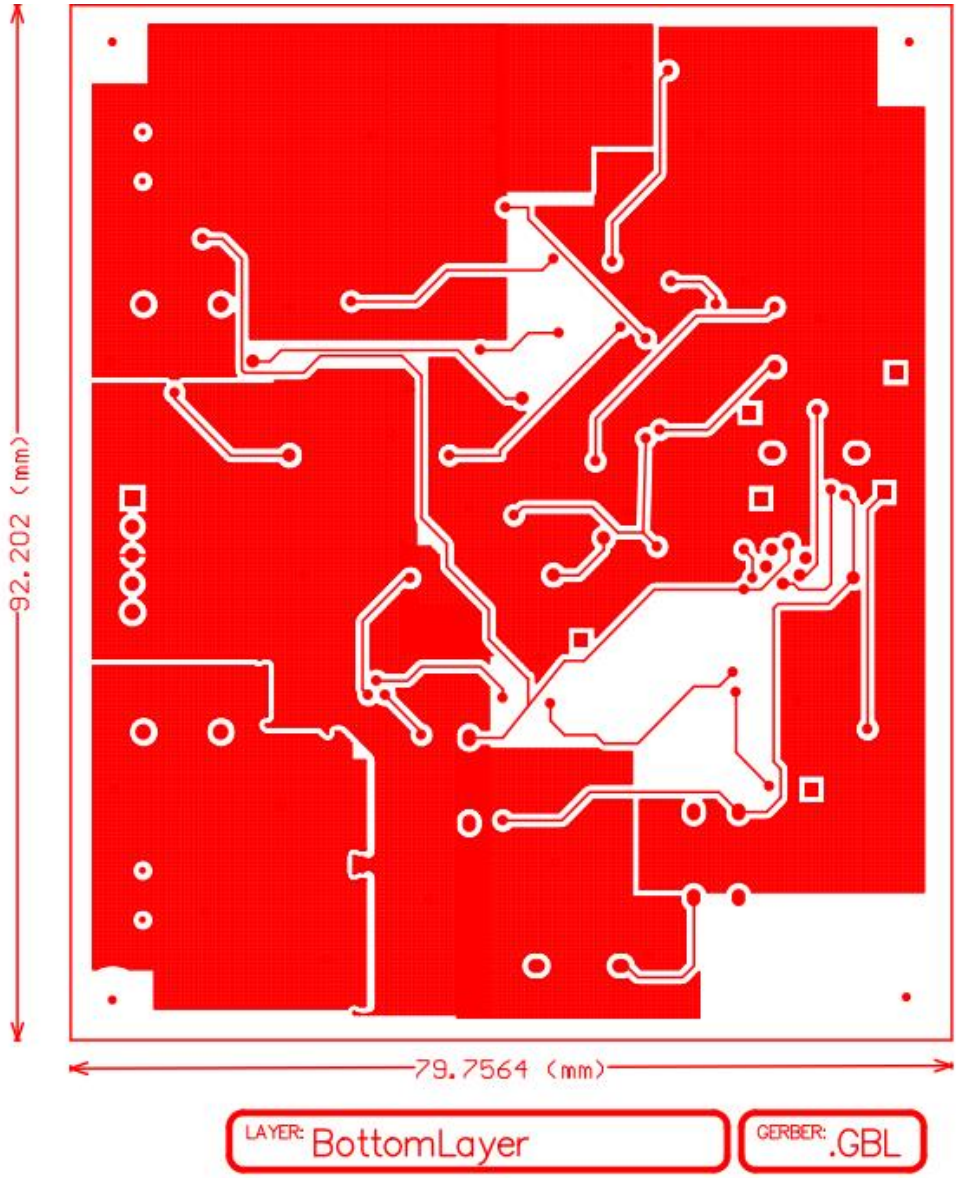


Figure B.3: Bottom layer of PCB.

APPENDIX C

Component list for bioimpedance simulator

Table C.1: Component list of the bioimpedance simulator

Component designator	Component description	Part Number /value	Quantity
C2, C3, C4, C5, C6, C8, C9, C10, C11, C12, C13, C14, C15, C16, C18, C20, C22, C24, C25, C26, C28, C29, C30, C39, C40, C41, C35, C36, C37, C38	Capacitor, ceramic, chip	0.1 µF	26
C1, C17, C19, C21, C23, C27, C31, C32, C33, C34	Capacitor, ceramic, chip	10 µF	10
R4, R5, R6, R7, R8, R10, , R13, , R27	Resistor	10 kΩ	11
R15, R16, R17, R18	Resistor	1.2 kΩ	4
R11, R12, R19, R20	Resistor	620 Ω	4
R2, R3	Resistor	1 MΩ	2
R21	Resistor	10 Ω	1
R22	Resistor	20 Ω	1
R23	Resistor	50 Ω	1
R14, R24	Resistor	100 Ω	2
R1	Resistor	1 kΩ	1

R25, R26	Resistor	100 kΩ	2
U1	IC, Microcontroller	DSPIC33FJ128GP802	1
U2	IC, RS232 driver	ADM3251E	1
U3, U6	IC, Op amp	LT1499	2
U4	IC, Analog switch	ADG811	1
U5	Package, JFET	U441	1
U7, U8	IC, LDO	MCP1802-3.3	2
U9	IC, LDO	MCP1802-5	1
U11	IC, LDO	TC5950	1
U12, U13	IC, DC-DC converter	TC962	2
J1	Connector, 5-pin	DEBUG	1
J2, J4	Stereo phone jack	PHONEJACK	2
J3, J10	Stereo phone jack	PHONEJACK	2
J6, J7	USBCON	USBMINIB	2
J5, J6, J7, J8, J9, J11	Connector, 1-pin	Test pin	6
D1, D2	Diode	Diode	2

REFERENCES

[1] S. Grimnes and O. G. Martinsen, *Bioimpedance and Bioelectricity Basics*, 2nd ed., Oxford, UK, Elsevier, 2008.

[2] D. Tsunami, J. McNames, A. Colbert, S. Pearson, and R. Hammerschlag, "Variable frequency bioimpedance instrumentation," in *Proc. 26th Annual Int. Conf. IEEE Eng. Med. Biol. Soc.*, San Francisco, pp. 2386−2389, 2004.

[3] H. P. Schwan and C. F. Kay, "Specific resistance of body tissues," *Circulation Research*, vol. 4 (6), pp. 664−670, 1956.

[4] R. P. Patterson, "Fundamentals of impedance cardiography*," IEEE Eng. Med. Biol. Mag.*, vol. 8 (1), pp. 35–38, 1989.

[5] Z. Lababidi, D. A. Ehmke, R. E. Durnin, P. E. Leaverton, and R. M. Lauer, "The first derivative thoracic impedance cardiogram," *Circulation Research*, vol. 41 (4), pp. 651–658, 1970.

[6] H. H. Woltjer, H. J. Bogaard, and P. M. J. M. de Vries, "The technique of impedance cardiography," *Euro. Heart J.*, vol. 18 (9), pp. 1396–1403, 1997.

[7] L. E. Baker, "Principles of impedance technique," *IEEE Eng. Med. Biol. Mag.*, vol. 8 (1), pp. 11–15, 1989.

[8] M. D. Desai, "Development of an impedance cardiograph," M Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2012.

[9] J. Fortin, W. Habenbacher, A. Heller, A. Hacker, R. Grüllenberger, J. Innerhofer, H. Passath, C. Wagner, G. Haitchi, D. Flotzinger, R. Pacher, and P. Wach, "Non-invasive beat-to-beat cardiac output monitoring by an improved method of transthoracic bioimpedance measurement," *Comput. Biol. Medicine*, vol. 36 (11), pp. 1185–1203, November 2006.

[10] H. H. Woltjer, B. J. M. van der Meer, H. J. Bogaard, and P. M. J. M. de Vries, "Comparison between spot and band electrodes and between two equations for calculations of stroke volume by means of impedance cardiography ," *Med. Biol. Eng. Computing*, vol. 33 (3), pp. 330−334, 1995.

[11] H. H. Woltjer, B. W. G. J. Arntzen, H. J. Bogaard, and P. M. J. M. de Vries, "Optimalisation of the spot electrode array in impedance cardiography," *Med. Biol. Eng. Computing*, vol. 34 (1), pp. 84−87, 1996.

[12] D. P. Bernstein, “A new stroke volume equation for thoracic electrical bioimpedance: Theory and rationale,” *Critical Care Med.*, vol. 14 (10), pp. 904–909, 1986.

[13] N. S. Manigandan, “Development of hardware for impedance cardiography,” M.Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2004.

[14] N. K. S. Naidu, “Hardware for impedance cardiography,” M.Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2005.

[15] L. Venkatachalam, “Development of hardware for impedance cardiography,” M.Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2006.

[16] B. B. Patil, “Instrumentation for impedance cardiography,” M. Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2009.

[17] J. Millman and C. C. Halkias, “Field effect transistors,” in *Integrated Electronics*, 2nd ed., New York, McGraw Hill, 2010, pp. 322−327.

[18] Wai-Kai Chen, “JFET, MESFET, and HEMT technology and devices,” in *Analog and VLSI Circuits*, 3rd ed., Boca Raton, FL, CRC Press, 2009, pp. 82−87.

[19] A. S. Sedra and K. C. Smith, “MOS field effect transistors,” in *Microelectronic Circuits*, 5th ed., New York, Oxford University Press, 2004, pp 248−259.

[20] Y. Tsividis, “The four-terminal MOS transistor,” in *Operation and Modelling of the MOS Transistor*, 2nd ed., Singapore, WCB/McGraw Hill, 1999.

[21] I. M. Filanovsky and A. Allam, “Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits,” *IEEE Trans. Circuits Syst.*, vol. 48 (7), pp. 876−884, Jul. 2001.

[22] R. Senani, “Realisation of linear voltage-controlled resistance in floating form,” *Electronics Letters*, vol. 30 (23), pp. 1909−1911, Nov. 10, 1994.

[23] H. F. Storm and N. Y. Delmar, “Insulated gate field effect transistor used as a voltage-controlled linear resistor,” U.S. Patent 3 577 019, 1971.

[24] G. Moon, M. E. Zaghloul, and R. W. Newcomb, “An enhancement-mode MOS voltage-controlled linear resistor with large dynamic range,” *IEEE Trans. Circuits Syst.*, vol. 37 (10), pp. 1284−1288, Oct. 1990.

[25] N. Tiwari, “Circuit for a voltage controlled resistor,” R & D project report, SPI Lab, Electrical Eng., IIT Bombay, Mumbai, India, Dec. 2012.

[26] J. Fort, “MOS resistor with second or higher order compensation,” U. S. Patent 8 067 975, 2011.

[27] T. L. Clarke, “FET pair and op amp linearize voltage controlled resistor,” *Electronics Letters*, pp. 111, Apr. 28, 1977.

[28] J. K. Greason, “Voltage-controlled resistance element with superior dynamic range,” U.S. Patent 5 264 785, Nov. 23, 1993.

[29] B. White and M.N. Hagh, “Precision MOS resistor,” U. S. Patent 5 345 118, 1994.

[30] A. Bilotti, “Operation of a MOS transistor as a variable resistor,” *IEEE Proc. Letters*, pp. 1093−1094, Aug.20, 1966.

[31] A. C. Barber, “Linearization of voltage-controlled amplifier using MOSFET gain control circuit,” U. S. Patent 5 808 516, 1998.

[32] Vishay, “Matched n-channel JFET pairs,” Available online, http://pdf.datasheetcatalog .com/datasheet/vishay/70251.pdf, downloaded on Apr. 22, 2014.

[33] Linear Systems. (2003, Jan. 17). jfet2003_ls5911familyspicemodels.zip [Online]. http://www.linearsystems.com/products_details.php?pr=jfet-amplifiers-- duals&pro_id =27.

[34] Linear Technology, “10MHz, 6V/μs, dual/quad rail-to-rail input and output precision C-load op amps,” Available online, http://cds.linear.com/docs/en/datasheet/ 14989fg.pdf, downloaded on May 22, 2014.

[35] Advanced Linear Devices, “Quad/dual n-channel matched pair MOSFET array,” Available online, http://www.aldinc.com/pdf/ALD1116.pdf, downloaded on June 26, 2012.

[36] Advanced Linear Devices. (2003, May 5). ALD 11xx MOSFET PSPICE model [Online]. Available: http://www.aldinc.com/view-pdf.php.

[37] V. K. Pandey, P. C. Pandey, and J. N. Sarvaiya, “Impedance simulator for testing of instruments for bioimpedance sensing,” *IETE J. Research*, vol. 54 (3), pp. 203−207, 2008.

[38] Analog Devices, “< 0.5 Ω CMOS, 1.65V−3.6V, quad SPST switches,” Available online, http://www.analog.com/static/imported-files/data_sheets/ADG811_812_813. pdf, downloaded on Aug. 27, 2013.

[39] Microchip, “16-bit digital signal controller,” Available online, http://www.microchip.com/downloads/en/DeviceDoc/70292E.pdf, downloaded on Aug. 27, 2013.

[40] Analog Devices, “Isolated, single channel RS232 line driver/receiver,” Available online, http://www.analog.com/static/imported-files/data_sheets/ADM3251E.pdf, downloaded on Aug. 27, 2013.

[41] Microchip, “300 mA, 16V, high-performance LDO,” Available online, http://ww1.microchip.com/downloads/en/DeviceDoc/25160A.pdf, downloaded on May 29, 2014.

[42] Microchip, “Low dropout, negative output voltage regulator,” Available online, http://ww1.microchip.com/downloads/en/DeviceDoc/21438C.pdf, downloaded on Feb. 12, 2014.

[43] Microchip, “High current charge pump DC-to-DC converter,” Available online, http://ww1.microchip.com/downloads/en/DeviceDoc/21484D.pdf, downloaded on May 29, 2014.

[45] M. Banu and Y. Tsividis, “Floating voltage controlled resistors in CMOS technology,” *Electronics Letters*, vol. 18 (15), pp. 678−679, July 22, 1982.

[46] L. E. Baker, “Applications of impedance technique to the respiratory system,” *IEEE Eng. Med. Biol. Mag.*, vol. 8 (1), pp. 50–52, 1989.

ACKNOWLEDGEMENT

I would like to express my sincere gratitude towards my guide Prof. P. C. Pandey for his invaluable guidance and support during this project. I am thankful to him for all the support in understanding and implementing this project and in learning new concepts. I am grateful to him for giving me moral support whenever I needed.

I am thankful to Nitya Tiwari for providing the groundwork for my project and supporting me in its implementation. I am highly indebted to Pai Sir (Mr M V Nandakumar) for many fruitful discussions on microcontroller based designs and PCB layouts and to Mr Vidyadhar Kamble for help and support for the development and test facilities for the hardware related work in the lab. I would also like to thank my friends for their support during my stay at IITB.

Last but not the least; I am thankful to my parents for their unconditional love and support in every phase of my life.

AUTHOR'S RESUME

Rani Holani: She has received her B.E. degree in Biomedical Engineering from Shri Govindram Seksaria Institute of Technology and Science, Indore in 2012. Presently, she is pursuing M.Tech. degree in Biomedical engineering at the Indian Institute of Technology Bombay. Her research interests include biomedical instrumentation, electronic system design, and embedded system design.