A Bioimpedance Simulator

A dissertation
submitted in partial fulfilment of
the requirements for the degree of

Master of Technology
in Electrical Engineering

by

Vikas Marla
(15307R012)

under the supervision of

Prof. P. C. Pandey

Department of Electrical Engineering
Indian Institute of Technology Bombay
June 2018

Indian Institute of Technology Bombay
Department of Electrical Engineering

M. Tech. Dissertation Approval

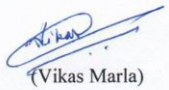
This dissertation entitled "**A Bioimpedance Simulator**" by **Vikas Marla** (Roll No.**15307R012**) is approved, after the successful completion of *viva voce* examination, for the award of the degree of **Master of Technology** in **Electrical Engineering** with specialization in **Electronic Systems**.

Supervisor:	..... 30/06/2018	(Prof. P. C. Pandey)
Examiners:	.....	(Prof. V. Rajbabu)
	.....	(Prof. J. John)
Chairman:	.....	(Prof. J. John)

Date: 30 June 2018
Place: Mumbai

DECLARATION

I declare that this dissertation represents my own ideas and words. I have cited and referenced the original sources adequately wherever other's ideas and words are included. I also declare that I have adhered to all principles of academic honesty and integrity and have not misprinted or fabricated or falsified any idea/data/fact/source in my submission. I understand any violation of the above will cause for disciplinary action by the institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.



(Vikas Marla)

(Roll No. 15307R012)

Date: 30 June 2018

Place: Mumbai

Vikas Marla / Prof. P. C. Pandey (Supervisor), “A Bioimpedance simulator,” *M.Tech. Dissertation*, Department of Electrical Engineering, Indian Institute of Technology Bombay, July 2018.

ABSTRACT

Impedance cardiography is a non-invasive technique involving measurement of the impedance of the thorax region for assessing the stroke volume and some other cardiovascular parameters which may be useful in diagnosis of cardiac disorders. A bioimpedance simulator is required to assess the impedance cardiograph instruments and also other bioimpedance measuring instruments. A bioimpedance simulator is developed to provide continuous time-varying impedance with adjustable basal impedance to imitate the thorax impedance. It consists of four blocks: a time varying impedance circuit and basal impedance circuit connected in parallel, controller circuit, wireless serial interface, and power circuit. A precision linear floating voltage-controlled resistor (VCR) is realized using a circuit with a matched pair of MOSFET devices, with independent substrates. The linear range of operation of MOSFET is extended by source drain (SD) bootstrapping of both gate and substrate terminals, and precise operation is achieved by self-tracking arrangement using an op amp. The time-varying impedance is simulated using the VCR. The adjustable basal impedance is simulated using resistor network and an analog multiplexer. The controller circuit is realized using a microcontroller with on-chip DAC and is serially connected to a Bluetooth module. The control waveforms to vary the resistance of the VCR are provided by the DAC of the microcontroller, and the controls to analog multiplexer to set the basal impedance are provided by IO port pins of the microcontroller. The parameters for the amplitude, frequency, waveforms of time-varying impedance, and basal impedance are set wirelessly through the Bluetooth module.

CONTENTS

LIST OF ABBREVIATIONS

Abbreviation	Explanation
AGND	analog ground
ASCII	American Standard Code for Information Interchange
COM	communication
DAC	digital-to-analog converter
DGND	digital ground
ECG	electrocardiogram
GND	ground
GUI	graphical user interface
IC	integrated circuit
ICG	impedance cardiogram
IO	input-output
ISR	interrupt service routine
JFET	junction field-effect transistor
LDO	low drop-out
LF-VCR	linear floating voltage controlled resistor
LVET	left ventricular ejection time
MOSFET	metal-oxide-semiconductor field-effect transistor
MUX	analog multiplixer
PC	personal computer
PCB	printed circuit board
SD	source-drain
SV	stroke volume
UART	universal asynchronous receiver/transmitter
VCR	voltage-controlled resistor

LIST OF SYMBOLS

Symbol	Explanation
$AV3V3$	analog supply of 3.3 V
A_{VREF}	reference voltage in the VCR circuit
$DV3V3$	digital supply of 3.3 V
f_S	sampling frequency of DAC
i_D	drain current
i_X	current through terminal X
i_Y	current through terminal Y
R_{DS}	drain-source channel resistance
R_{XY}	resistance across X-Y terminal
R_o	fixed resistance in the simulator model of thorax
R_v	variable resistance in the simulator model of thorax
v_A	control voltage
v_B	substrate voltage
v_{BS}	substrate-source voltage
v_C	common mode voltage
v_d	differential voltage
v_{DS}	drain-source voltage
v_G	gate voltage
v_{GS}	gate-source voltage
V_{T0}	threshold voltage without body effect
V_T	threshold voltage
v_X	X-terminal voltage
v_Y	Y-terminal voltage
V_{BB}	substrate bias voltage
ρ	specific resistivity

LIST OF FIGURES

LIST OF TABLES

Chapter 1

INTRODUCTION

1.1 Background

Bioimpedance measurement is a technique for quantifying and assessing the change in the electrical impedance of the biological materials like tissues, blood, body fluids, etc. [1], [2], [3]. These measurements may be helpful in diagnosis of abnormality in human body. Some of the common applications include assessment of blood volumes, vocal cord dynamics, and cardiac disorders [1]. The blood has highest conductivity among all the biological materials [2] and variation in the amount of blood in the thorax during the cardiac cycle causes variation in the thoracic impedance. Impedance cardiography (ICG) is the study of cardiac function using non-invasive measurement of electrical impedance of the thorax [3]. The thoracic impedance consists of a basal impedance and a time-varying component. ICG can be used for assessing cardiac activity by measuring blood flow parameters such as blood ejection time, maximum blood ejection velocity, stroke volume, cardiac output etc. In impedance cardiography technique, a low amplitude (< 5 mA) and high frequency (20 −100 kHz) current is injected through a pair of electrodes to the thorax region. The voltage across the thorax gets amplitude modulated due to the variation in the thoracic impedance. It is picked-up using another pair of electrodes and is demodulated to sense the impedance variation [8]. Some of the commercially available ICG instruments are Medis non-invasive cardiac output monitor (Niccomo) [11] and Philips ICG (Model 862146) [12].

The bioimpedance simulator is used for testing an ICG instrument by assessing its linearity, sensitivity, and dynamic response [13]. It should be able to simulate the basal and time-varying components of the thoracic impedance in a settable manner.

1.2 Project Objective

The objective of this project is to develop a bioimpedance simulator for the purpose of testing an impedance measuring instrument in terms of its linearity, sensitivity, and dynamic response. The simulator should be able to simulate the impedance variation of various waveform shapes (sine wave, square wave, triangular wave, thoracic impedance waveform). The amplitude, frequency, and waveshape of the impedance variation should be externally controllable. For this purpose, a circuit consisting of four modules is developed: resistance variation circuit, controller circuit using a microcontroller, serial interface and bluetooth module, and power circuit. The resistance variation circuit is realized using a MOSFET based

voltage controlled resistor. The resistance variation is controlled by the controller circuit devised using microcontroller to generate control waveforms. The control parameters are sent wirelessly to the microcontroller using a PC-based user interface.

1.3 Report Outline

Chapter 2 provides a review of impedance cardiography. Chapter 3 presents the study of MOSFET based VCR circuits and the test results. The design and implementation of the bioimpedance simulator is presented in Chapter 4, and the test results are presented in fifth chapter. The last chapter provides a summary and conclusion of the work.

Chapter 2

BASICS OF IMPEDANCE CARDIOGRAPHY

2.1 Introduction

Impedance cardiography is a non-invasive technique to estimate the blood ejection time, maximum blood ejection rate, stroke volume, etc. by measuring and analysing the impedance variation across the thorax region. The variation in the thoracic impedance is due to change in the blood volume in blood vessels and change in specific resistivity of blood as a function of velocity of blood flow due to cardiac activity, and due to variation of air volume in the lungs during ventilation [1], [2]. An excitation current having low amplitude (< 5mA) and high frequency (20 − 100 kHz) is injected in the thorax region through a pair of electrodes. The resulting amplitude modulated voltage due to variation in impedance is measured using another pair of electrodes and its amplitude is used to measure the impedance [3], [5], [6], [9]. The impedance consists of basal impedance along with a small time-varying component [9]. The basal impedance is typically 20 − 200 Ω and the time-varying component is about 0.1 – 2 % of the basal impedance [7]. For the current injected at the above frequency range, the tissue is not excitable, thereby minimizing the risk of any physiological effects and also the thoracic impedance variation is primarily resistive in nature [3]. Use of above frequency range also results in lower carrier ripple after demodulation. At higher frequency (> 500 kHz) the current does not penetrate into the deeper region of the thorax and the time-varying component of the impedance signal decreases.

2.2 ICG waveform

The impedance signal $Z(t)$ has a basal impedance Z_o with a superimposed time-varying component $z(t) = Z(t) - Z_o$. An example of time-varying impedance signal $-z(t)$, its first derivative $-dZ/dt$ with its characteristic points marked on it, and ECG signal are shown in Fig. 2.1 [6]. The A point follows the P wave of ECG indicating atrial contraction. The B point indicates the opening of the aortic valve and the X point indicates the closure of the aortic valve. The C point is the maximum of the waveform and occur during the systole. The O point is an upward deflection indicating the opening of the mitral valves. A study of relationship between the occurrence of the ICG characteristics points with reference to the ECG characteristic points in the cardiac cycle can be helpful in diagnosis of cardiac disorders.

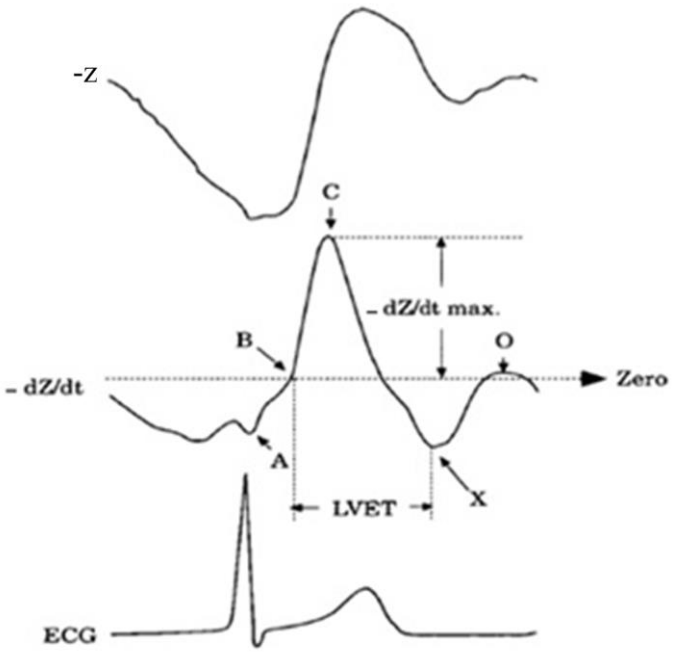


Fig. 2.1 The thoracic impedance waveform (z (t)), ICG $\left(\frac{-dZ}{dt}\right)$, and ECG, adapted from [6].

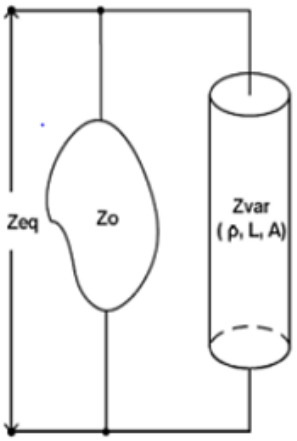


Fig. 2.2 Parallel column model of thoracic impedance, source [3].

The time duration between the A and X points is known as the left ventricular ejection time (LVET). The product of $(-dz/dt)_{\max}$ and LVET is used for calculating the stroke volume.

2.3 Parallel column model of thoracic impedance

The parallel column model of the thoracic impedance, as shown in Fig. 2.2, is used to analyse and quantify the impedance change of the thorax region due to cardiac activity [3]. The model has constant impedance Z_O in parallel with the variable impedance Z_{var} represented by a cylindrical column, of fixed length *L*, resistivity ρ, and time-varying cross sectional area *A*. Using this model, it has been shown that the change in the volume is related to change in the impedance as the following:

$$\Delta V = \left(\frac{\rho L^2}{{Z_O}^2} \right) \Delta Z \tag{2.1}$$

Based on this model, Kubicek et al. [8] assumed ΔV to be stroke volume SV and modelled ΔZ as ventricular ejection time $(-dz/dt)_{\max} T_{LVET}$, and developed the formula for stroke volume as

$$\text{SV} = \left(\frac{\rho L^2}{{Z_O}^2} \right) \left(-\frac{dZ}{dt} \right)_{\max} T_{LVET} \tag{2.2}$$

Kubicek's equation for SV was modified by Sramek [9] by considering thorax region as a truncated cone and relating L to person's height *H* given, as

$$\text{SV} = \left(\frac{(0.17H)^3}{4.25 Z_O} \right) \left(-\frac{dZ}{dt} \right)_{\max} T_{LVET} \tag{2.3}$$

Bernstein added a weight correction factor δ and the SV equation was modified as Sramek-Bernstein [7], [9] equation

$$\text{SV} = \delta \left(\frac{(0.17H)^3}{4.25 Z_O} \right) \left(-\frac{dZ}{dt} \right)_{\max} T_{LVET} \tag{2.4}$$

Most techniques for SV estimation using ICG are based on one of the above formula or some variants.

2.4 Impedance cardiography

In impedance cardiography, the time-varying impedance of the thorax region is measured by injecting an alternating current through a pair of electrodes placed across it and picking up the resulting amplitude modulated voltage through another pair of electrodes, Fig. 2.3 shows the block diagram of an impedance cardiograph instrument. The electrodes are placed on thorax region in tetra-polar configuration [3], [11]. A pair of electrodes i.e. current source electrodes are used to inject current and the other pair i.e. voltage sensing electrodes are used to pick-up the resulting voltage. The frequency of alternating current applied is in the

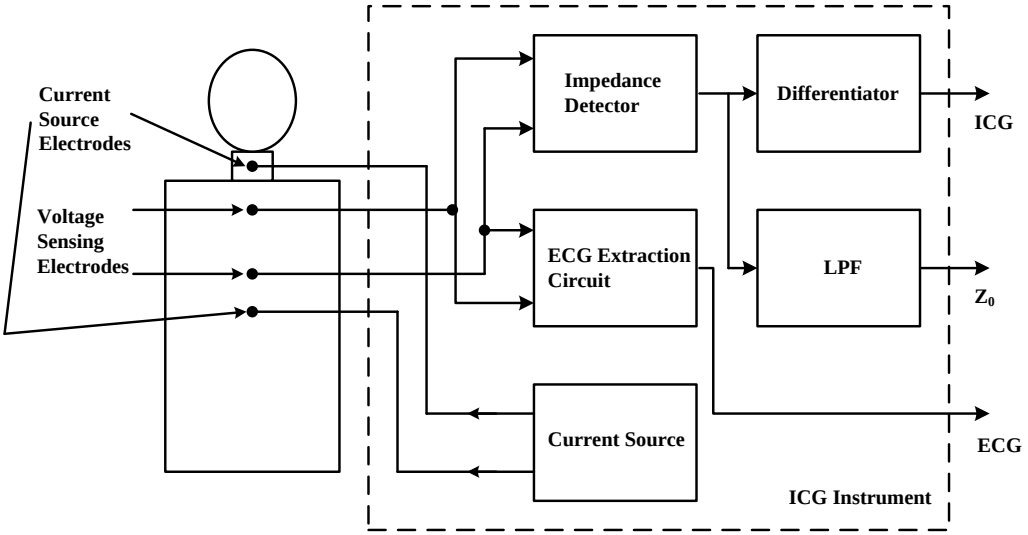


Fig. 2.3 Block diagram for impedance cardiograph instrument with tetra-polar electrode configuration

range of 20 − 100 kHz with a low amplitude (< 5 mA) [6]. The voltage picked-up across the thoracic region gets amplitude modulated due to variation in the thoracic impedance.

The impedance detector block demodulates the amplitude modulated signal due to impedance variation. The modulation index is 0.1 % to 2 % of the basal value. To demodulate, the impedance detector needs to be highly sensitive to impedance variation signal and able to reduce additive noise in the sensed voltage and suppress ripples related to the excitation frequency. The output of the demodulator is proportional to the impedance $Z(\mathrm{t})$. It is passed through a differentiator to obtain the ICG signal dZ/dt and it is low pass filtered to obtain the basal impedance Z_O. The ECG signal is extracted using ECG extraction circuit sensed through the same voltage sensing electrodes used in impedance detection. The ECG signal is used as a reference for detection of characteristic points of ICG [14].

Chapter 3

VOLTAGE CONTROLLED RESISTOR

3.1 Introduction

A bioimpedance simulator provides a time-varying impedance in accordance with the control input applied to mimic the bioimpedance variations. A JEFT or MOSFET can be used as voltage controlled resistor, by controlling its drain-to-source resistance by varying its gate-source voltage. However, it acts as linear resistor for a small range of drain-source voltage, and the drain-source resistance varies with its temperature and device parameters. Thus, we need a precision linear floating voltage-controlled resistor (VCR). In this chapter, MOSFET operation, constraints in using it as a precision linear floating VCR, various circuit realizations to overcome the constraints with theoretical analysis, and test results are presented. A VCR circuit, in addition to being used in bioimpedance simulator, can also be used in multipliers, modulators, demodulators, volume controllers and tunable filters.

3.2 MOSFET basics

A MOSFET operated in triode region can be used as a VCR [16], [17], [18], as its drain-to-source resistance is a function of the gate-to-source voltage. For an n-channel MOSFET with gate-to-source voltage v_{GS}, drain-to-source voltage v_{DS}, and drain current i_D, the i_D vs v_{DS} characteristics with threshold voltage V_T are shown in Fig. 3.1. There are three regions of operation: cut-off, triode, and saturation. The saturation region is used to operate MOSFET as an amplifier. The triode and the cut-off regions are used to operate MOSFET as a switch. MOSFET can also be used as voltage-controlled resistor when operated in the triode region. In the cut-off region,

$$i_D = 0,\ v_{GS} < V_T \tag{3.1}$$

In the saturation region,

$$i_D = k(v_{GS} - V_T)^2,\ v_{GS} \geq V_T \text{ and } v_{GS} - V_T \leq v_{DS} \tag{3.2}$$

In the triode region,

$$i_D = k((v_{GS} - V_T)v_{DS} - \frac{1}{2}{v_{DS}}^2),\ v_{GS} \geq V_T \text{ and } v_{GS} - V_T > v_{DS} \tag{3.3}$$

The value of the device parameter k is given as

$$k = \mu_n C_{ox} \frac{W}{L}, \tag{3.4}$$

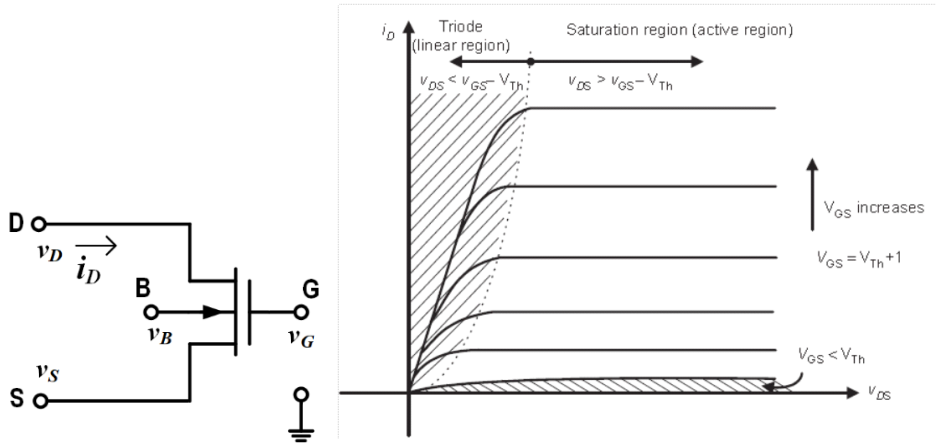


Fig. 3.1: $i_{DS} - v_{DS}$ characteristics for an n-channel enhancement type MOSFET [14]

where, μ_n is the carrier mobility, C_{ox} is the gate oxide overlap capacitance, and *W* and *L* are width and length of MOSFET respectively [16]. The carrier mobility depends on the temperature *T* [16] and the relation is given as

$$\mu(T) = \mu_O \left(\frac{T_O}{T} \right)^m , \tag{3.5}$$

where μ_O is the mobility at the reference temperature T_O, and *m* is the constant in the range of 1.2−2 [32], [33].

The threshold voltage V_T depends on the temperature T as

$$V_T(T) = V_T(T_O) - K(T - T_O), \tag{3.6}$$

where *K* is the temperature drift coefficient, V_T is also reported to be dependent on v_{BS} [32]

$$V_T = V_{TO} + \gamma(\sqrt{2\varphi_B + v_{BS}} - \sqrt{2\varphi_B}), \tag{3.7}$$

where V_{TO} is the threshold voltage for $v_{BS} = 0$, γ is a parameter related to the fabrication process, and φ_B is physical parameter with typical value of 0.3 V [16]. Thus, the drain current of the MOSFET changes with the change in substrate bias. In a model [15], based on the symmetry of the source and drain terminals, the threshold voltages at source and drain are given as

$$V_{TD} = V_{TO} + (\alpha - 1)(v_D - v_B), \tag{3.8}$$

$$V_{TS} = V_{TO} + (\alpha - 1)(v_S - v_B) \tag{3.9}$$

where v_B is the substrate (body or bulk) voltage applied, V_{TO} is the threshold voltage without considering the body effect, and α is a process dependent parameter (typically 1.05 – 1.35) [17]. Thus, there is shift in the threshold voltage of the MOSFET due to the channel substrate

voltage at the two ends of the channel. For a MOSFET, the source and drain terminals are interchangeable. For an n-channel MOSFET, the terminal at higher potential is drain and the other one is source and opposite to this is in the case of p-channel MOSFET. During normal operation of the MOSFET, no current flows into the gate and substrate terminals. To operate in triode region, the gate-channel voltage must be higher than the threshold at the source and drain terminals, and gate voltage of MOSFET is selected such that:

$$v_G - v_S \geq V_{TS}, \tag{3.10}$$

$$v_G - v_D \geq V_{TD}, \tag{3.11}$$

Using (3.8) and (3.9), (3.10) and (3.11) can be rewritten as

$$v_G - v_B \geq V_{TO} + \alpha(v_S - v_B), \tag{3.12}$$

$$v_G - v_B \geq V_{TO} + \alpha(v_D - v_B), \tag{3.13}$$

In the triode region, the drain current i_D is given as [21]

$$i_D = \frac{k}{2\alpha}((v_{GS} - V_{TS})^2 - (v_{GD} - V_{TD})^2), \tag{3.14}$$

From (3.8), (3.9), and (3.14), i_D is given as

$$i_D = \frac{k}{2\alpha}((v_G - v_S - (V_{TO} + (\alpha - 1)(v_S - v_B)))^2 - (v_G - v_D - (V_{TO} + (\alpha - 1)(v_D - v_B)))^2) \tag{3.15}$$

Simplifying (3.15), results in:

$$i_D = k\left(v_G - v_B - V_{TO} - \alpha\left(\frac{v_D + v_S}{2} - v_B\right)\right)(v_D - v_S), \tag{3.16}$$

The drain-to-source resistance $R_{DS} = (v_D - v_S)/i_D$ is given as

$$R_{DS} = \frac{1}{k\left(v_G - v_B - V_{TO} - \alpha\left(\frac{v_D + v_S}{2} - v_B\right)\right)} \tag{3.17}$$

It may be noted that the circuit is acting as a floating VCR and the resistance can be controlled by varying voltage at gate terminal v_G. As the resistance R_{DS} depends on the common mode voltage ($v_D + v_S$)/2, the MOSFET device will not act as a linear resistor.

For small v_{DS} applied, the substrate terminal is tied with the source terminal to ensure that substrate-to-channel is not forward biased. However, for larger v_{DS}, the channel potential varies across its length, known as channel length modulation, and variation of substrate-to-channel potential introduces variation in the resistance. With v_S = 0 V, R_{DS} can be used as a grounded VCR. However, it is not linear because it depends on v_D. Further as R_{DS} depends on k and V_{TO}, it varies with process dependent parameters and also due to temperature

variations and substrate-channel bias v_B. Therefore, the resulting VCR does not serve as precision VCR.

3.3 Voltage controlled resistor circuits

A voltage controlled resistor circuit is used to vary the resistance controlled by an external voltage applied to it. The resistance variation in continuous form is realized using a MOSFET acting as a VCR [16]. The drain-to-source resistance of a MOSFET device operating in triode region can be varied by controlling the gate voltage, with the substrate terminal connected to external bias to maintain the reverse bias across the substrate-channel junction. A linear VCR is required to have the current through it to be proportional to the voltage across the resistance terminals. As described in the previous section, MOSFET operating in its triode region can be used as a linear VCR [16], [17], [18]. The drain-to-source resistance is constant for very small range of drain-to-source voltage typically of tens of mV. The drain to source resistance is dependent on the device parameter which may vary with temperature and also may have significant piece-to-piece variation [32]. For a precision resistance, the effect of temperature-dependent and piece-to-piece variations in the device parameters should be reduced. And also, a precision VCR should be deterministically related to the control voltage to it. The VCR circuits are implemented as either grounded or floating. In grounded VCR, one of the terminals is grounded. In floating VCR, neither of the terminal is grounded, and the current entering into one terminal will be equal to the current coming out of the other terminal. Several circuits have been reported to satisfy one or more of the above requirements [19], [20], [23], [24], [25], [32], [33].

Clarke [20] used two matched JFETs and an op amp to realize a grounded VCR whose resistance value is independent of the device parameters. The source terminal of one of the two JFETs is connected to the negative terminal of the op amp. The output of the op amp is connected to the gate terminal of the JFET, acting as a control voltage, thus forming a negative loop with the JFET. The output of the op amp is also given to gate terminal of the other JFET acting as grounded VCR. For this VCR circuit, the resistance does not depend on the device parameters and the circuit can be used as a precision VCR. However, it has restrictions of low voltage range and is a grounded VCR. Moon [23] used a pair of matched MOSFETs connected in parallel to implement VCR. One of the MOSFET is operated in triode region and the other in saturation region. The non-linearity in the sum of the drain currents flowing through each of the two MOSFETs gets eliminated. An independent voltage source is connected to the source terminal of the MOSFET operating in triode region, so that its gate-to-source voltage remains above the threshold voltage for the applied range of drain-to-source voltage. Senani [19] used a JFET operating in triode region to implement floating

VCR. The control voltage, the source and drain terminal voltages of the JFET are added using an op amp based adder, and the output of the adder is applied to the gate terminal of the JFET. The non-linearity terms in the expression of drain current of the JFET is eliminated due to the addition of source and drain terminal voltages. The circuit acts as linear floating VCR but depends on the device parameters, and thus cannot be used as a precision VCR.

Holani [32] proposed a VCR circuit using matched JFET pairs operating in triode region and two op amps to realize a linear floating precision VCR. One of the JFETs and an op amp are connected in a negative feedback loop which provides the control voltage for the other JFET. The control voltage, drain and source terminal voltages of other JFET are added using an op amp based adder circuit to obtain the voltage at the gate terminal voltage of the other JFET whose resistance is to be controlled. The matched JFET pair eliminates the effect of device dependent parameters from the drain current, and the addition of drain and source voltages extends the linear range of operation.

3.3.1 MOSFET based voltage controlled resistor circuits

The expression for the current in (3.16) can be rewritten as:

$$i_D = k\left(v_G - \frac{v_D + v_S}{2} - V_{TO} - (\alpha - 1)\left(v_B - \frac{v_D + v_S}{2} \right) \right)(v_D - v_S) \qquad (3.18)$$

The dependence of i_D is on the common mode voltage can be avoided by eliminating the term $(v_D + v_S)/2$ in the above equation. This can be achieved by obtaining the gate voltage v_G and substrate voltage v_B from voltage v_A, and substrate bias V_{BB} as the following:

$$v_G = v_A + \frac{v_D + v_S}{2} \qquad (3.19)$$

$$v_B = V_{BB} + \frac{v_D + v_S}{2} \qquad (3.20)$$

With these voltages given, (3.18) can be expressed as

$$i_D = k\left(v_A - V_{T0} - (\alpha - 1)V_{BB} \right)(v_D - v_S) \qquad (3.21)$$

Thus, the drain to source resistance $R_{DS} = (v_D - v_S)/i_D$, can be rewritten as

$$R_{DS} = \frac{1}{k\left(v_A - V_{T0} + (\alpha - 1)V_{BB} \right)} \qquad (3.22)$$

Thus, the addition of common mode voltage $(v_D + v_S)/2$ voltage can be used to realize linear floating VCR (LF-VCR). Addition of the mean of source and drain voltages to the gate and substrate terminals is also called as source-drain bootstrapping. The floating VCR circuit shown in Fig. 3.2 implements the above technique. The resistance R_{DS} is obtained across floating terminals X and Y which are connected to the drain and source terminals of

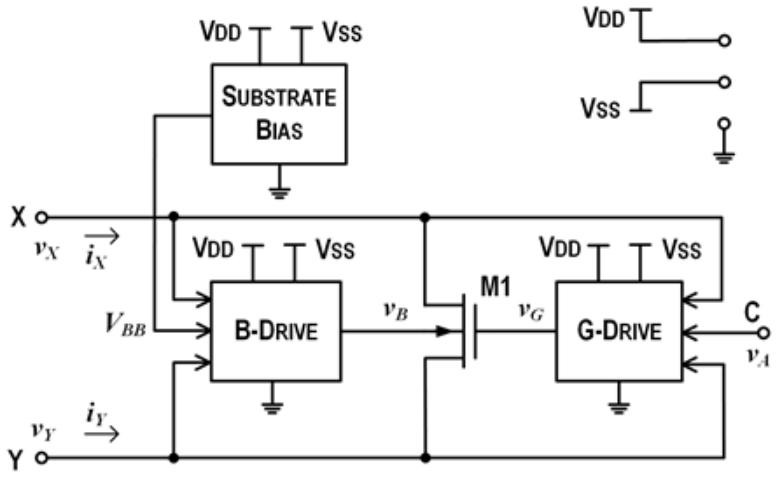


Fig. 3.2 Block diagram of NMOS based linear floating VCR

MOSFET M1 respectively. The voltages v_X and v_Y are applied across terminals X and Y with current i_X and i_Y flowing into them, with $i_Y = -i_X$. The voltages v_G and v_B as given in (3.19) and (3.20) can be implemented by the G-drive and B-drive block respectively as shown in Fig. 3.2. Control voltage v_A controls the resistance across drain-source terminals of MOSFET M1. The substrate bias block is used to obtain the external bias V_{BB} for substrate terminal of M1. The G-drive block obtains the sum of its three inputs i.e. control voltage v_A, drain and source terminal voltages (as a common mode voltage $(v_D + v_S)/2$) and generates the output v_G to drive the gate terminal of M1. Similarly, the B-drive block has external bias V_{BB}, drain, and source terminal voltages as its inputs and generates the output v_B to drive the substrate terminal. All the blocks are powered by connections to VDD, VSS and ground. All the above mentioned blocks can be realized using op amps and resistors, or MOSFETs for realization of circuit as a part of integrated circuit (IC) chip. As can be noted from (3.22), the resistance R_{XY} depends on the device parameters k , V_{T0} , and α . Thus, the circuit cannot be used as a precision VCR circuit. To obtain a precision VCR, the resistance must not change with the device parameters or temperature. By changing the control voltage v_A corresponding to the change in device parameters or temperature, the variation of R_{XY} can be compensated. This is achieved by the technique proposed by Debbarma [33], whose block diagram is shown in Fig. 3.3. The schematic of VCR with a pair of n-channel MOSFETs M1 and M2 with independent substrate terminals with both operating in triode region, is shown in Fig. 3.3. In this circuit, there are two VCRs i.e. variable LF-VCR similar as shown in Fig. 3.2, using MOSFET M1, G-drive block 1, B-drive block 1, and the other is reference LF-VCR using MOSFET M2, G-drive block 2, B-drive block 2. All these blocks are powered by connecting

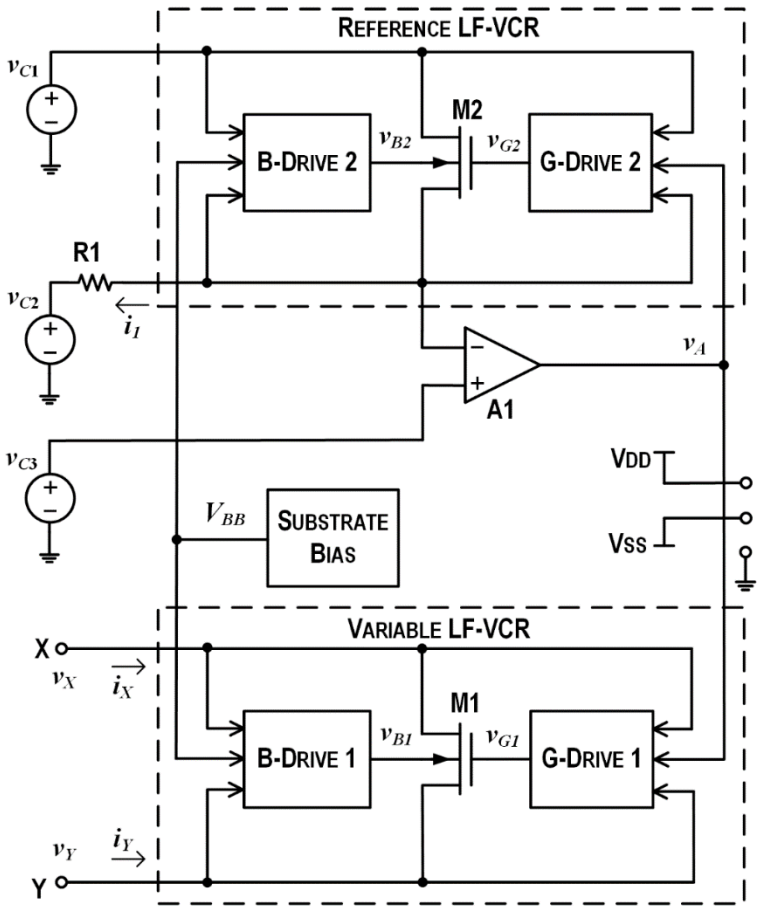


Fig. 3.3 Block diagram of NMOS based precision linear floating VCR using voltage control or resistance control

to VDD, VSS and ground, which is not shown in the figure. The reference LF-VCR along with the op amp A1 forms a negative feedback loop. With MOSFETS M1 and M2 being matched, the output of the op amp v_A compensates for the variation in the device parameters. The output of op amp acts as a control voltage v_A for both the variable LF-VCR and reference LF-VCR. The voltages v_{C1}, v_{C2}, v_{C3}, and R1 are the control parameters to vary the resistance R_{DS2} across the drain and source terminals of MOSFET M2. For a negative feedback loop from the output of the op amp to the negative terminal with MOSFET M2, the direction of current i_1 should be as shown in Fig. 3.3. For this condition, the external voltages should be such that $v_{C1} > v_{C3} > v_{C2}$. And also due to op amp connected as negative feedback, the voltage at non-inverting terminal v_{C3} is equal to voltage at inverting terminal. The resistance R_{DS2} which is part of reference LF-VCR is mirrored to the resistance R_{DS1} across drain and source terminals of M1. The voltages at gate terminals v_{G1} and v_{G2} of M1 and M2 respectively are

obtained by adding source and drain terminals with v_A using G-drive1 and G-drive2 block respectively, given as

$$v_{G1} = v_A + \frac{v_X + v_Y}{2} \tag{3.23}$$

$$v_{G2} = v_A + \frac{v_{C1} + v_{C3}}{2} \tag{3.24}$$

The substrate terminal voltages v_{B1} and v_{B2} for M1 and M2, respectively, are obtained by adding voltages at source and drain terminals with V_{BB} using B-drive1 and B-drive2 block respectively,

$$v_{B1} = V_{BB} + \frac{v_X + v_Y}{2} \tag{3.25}$$

$$v_{B2} = V_{BB} + \frac{v_{C1} + v_{C3}}{2} \tag{3.26}$$

The current through M2 is given as

$$i_1 = \frac{v_{C3} - v_{C2}}{R_1} \tag{3.27}$$

Drain to source resistance R_{DS2} of M2 is given as

$$R_{DS2} = \frac{v_{C1} - v_{C3}}{i_1} \tag{3.28}$$

From (3.27) and (3.28) R_{DS2} is given as follows:

$$R_{DS2} = \frac{v_{C1} - v_{C3}}{v_{C3} - v_{C2}} \times R_1 \tag{3.29}$$

Using (3.16), the drain current i_1 through M2 is given as:

$$i_1 = k_2 \left(v_{G2} - v_{B2} - V_{TO2} - \alpha_2 \left(\frac{v_{C1} + v_{C3}}{2} - v_{B2} \right) \right) (v_{C1} - v_{C3}) \tag{3.30}$$

Substituting values of v_{G2} and v_{B2} from (3.24) and (3.26) in (3.30), the drain current i_1 of M2 can be rewritten as:

$$i_1 = k_2 \left(v_A - (V_{TO2} + (1 - \alpha_2) V_{BB} \right) (v_{C1} - v_{C3}) \tag{3.31}$$

From (3.27) and (3.31) v_A is given as:

$$v_A = \left(\frac{v_{C3} - v_{C2}}{(v_{C1} - v_{C3}) k_2 R_1} + V_{TO2} + (1 - \alpha_2) V_{BB} \right) \tag{3.32}$$

From the above equation, it may be concluding that output of the op amp A1 is dependent on v_{C1}, v_{C2}, v_{C3}, and R1 and also on the device parameters of the MOSFET. Thus, the output of the op amp v_A which is control voltage to both the MOSFETs varies with the external

control parameters v_{C1}, v_{C2}, v_{C3}, and R1 and also compensates for variation in the device parameters.

From (3.16), the current i_X through M1 is given as:

$$i_X = k_1\left(v_{G1} - v_{B1} - V_{TO1} - \alpha_1\left(\frac{v_X + v_Y}{2} - v_{B1}\right)\right)(v_X - v_Y) \tag{3.33}$$

Substituting values of v_{G1} and v_{B1} from (3.23) and (3.25) in (3.33) the drain current i_X can be rewritten as

$$i_X = k_1\left(v_A - (V_{TO1} + (1-\alpha_1)V_{BB}\right)(v_X - v_Y) \tag{3.34}$$

Drain to source resistance R_{XY} of M1 is given as

$$R_{XY} = \frac{v_X - v_Y}{i_X} \tag{3.35}$$

From (3.34) and (3.35) R_{XY} in terms of v_A is given as

$$R_{XY} = \frac{1}{k_1\left(v_A - (V_{TO1} + (1-\alpha_1)V_{BB}\right)} \tag{3.36}$$

Substituting value of v_A from (3.32) in (3.36) gives R_{XY} as

$$R_{XY} = \frac{1}{k_1\left(\frac{v_{C3} - v_{C2}}{(v_{C1} - v_{C3})k_2 R_1} + V_{TO2} - V_{TO1} - (\alpha_2 - \alpha_1)V_{BB}\right)} \tag{3.37}$$

As M1 and M2 are matched MOSFETS, $\alpha_1 = \alpha_2$, $k_1 = k_2$, and $V_{TO1} = V_{TO2}$ in (3.37), R_{XY} can be expressed as

$$R_{XY} = \frac{v_{C1} - v_{C3}}{v_{C3} - v_{C2}} \times R_1 \tag{3.38}$$

Thus, from (3.38), it can be seen that R_{XY} only depends on the external control inputs v_{C1}, v_{C2}, v_{C3}, and R1. It is independent of the common mode voltage, differential voltage (drain to source voltage) and device parameters. Thus, the circuit shown in Fig. 3.3 realizes a linear and precision floating resistor, whose value can be controlled by combination of v_{C1}, v_{C2}, v_{C3}, and R1, or any one of them.

From (3.12) and (3.13) the conditions for M1 to operate in triode region is given as

$$v_{G1} - v_{B1} \geq V_{TO1} + \alpha(v_X - v_{B1}), \tag{3.39}$$

$$v_{G1} - v_{B1} \geq V_{TO1} + \alpha(v_Y - v_{B1}), \tag{3.40}$$

From (3.23), (3.25), (3.39) and (3.40), the boundary condition on drain-to-source voltage of M1 to operate in triode or linear region is given as

$$|v_X - v_Y| \leq \frac{2}{\alpha}(v_A - V_{TO1} - (1-\alpha)V_{BB}) \tag{3.41}$$

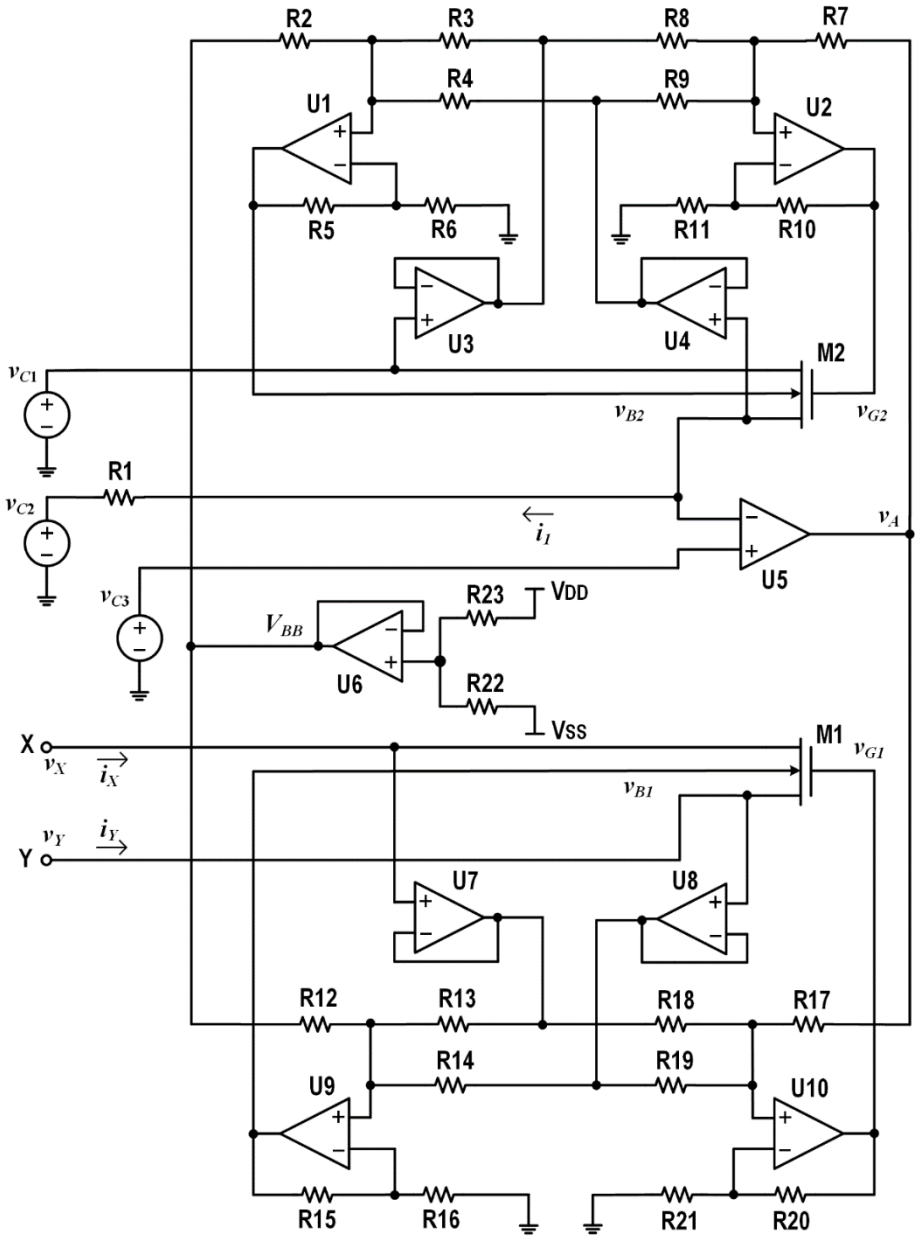


Fig. 3.4 Circuit for realization of NMOS based precision linear floating VCR using op amps

For substrate channel junction to remain in reverse biased, $v_X > v_{B1}$ and $v_Y > v_{B1}$, which can be rewritten as $v_X > V_{BB} + \frac{v_X + v_Y}{2}$ and $v_Y > V_{BB} + \frac{v_X + v_Y}{2}$.

Thus, the boundary condition for drain-to-source voltage, for substrate terminal to remain in reverse biased is given as

$$|v_X - v_Y| < -2V_{BB} \tag{3.42}$$

Thus, with a larger negative values of V_{BB}, a larger range of differential input ($v_X - v_Y$) can be applied. From (3.41) and (3.42), the range of drain-to-source voltages that can be applied across the X and Y terminals for linear operation, and substrate channel junction to be in reverse biased is given as

$$|v_X - v_Y| < \min\left(\frac{2}{\alpha}(v_A - V_{TO} - (1-\alpha)V_{BB}), -2V_{BB}\right) \tag{3.43}$$

The precision LF-VCR schematic shown in Fig. 3.3 can be implemented using op amps and resistors as shown in Fig. 3.4. The op amp U5 forms a negative feedback loop with M2 to generate the output voltage v_A. As U5 is connected in negative feedback loop, the negative terminal of U5 is at potential v_{C3}. Op amp based voltage adders U1, U2, U9, and U10 are used to realize G-drive 2, B-drive 2, B-drive 1, and G-drive 1 blocks, respectively, in the same way as shown in Fig. 3.3. The op amps U3, U4, U7, and U8 are used as buffers with source and drain terminals of M1 and M2 as their inputs. The op amp U6 with R_{22} and R_{23} is used to realize the substrate bias block to provide the substrate bias V_{BB} to the MOSFET circuit. The output v_{B1} of the op amp U9 is given as

$$v_{B1} = (1+R_{15}/R_{16})\,[V_{BB}(R_{13} \| R_{14})/(R_{12}+R_{13} \| R_{14}) + v_X\,(R_{12} \| R_{14})/(R_{13}+R_{12} \| R_{14}) + v_Y\,(R_{12} \| R_{13})/(R_{14}+R_{12} \| R_{13})] \tag{3.44}$$

To obtain the relation in (3.44) the same as that in (3.25), the resistor values are selected as

$$R_{15} = R_{16} \tag{3.45}$$

$$R_{13} = R_{14} = 2R_{12} \tag{3.46}$$

Similarly, to obtain the output voltages of op amp adders v_{G1}, v_{G2} and v_{B2} as given in (3.23), (3.24), and (3.26) respectively, the resistor values are selected as the following:

$$R_{20} = R_{21} \tag{3.47}$$

$$R_{18} = R_{19} = 2R_{17} \tag{3.48}$$

$$R_{10} = R_{11} \tag{3.49}$$

$$R_8 = R_9 = 2R_7 \tag{3.50}$$

$$R_5 = R_6 \tag{3.51}$$

$$R_3 = R_4 = 2R_2 \tag{3.52}$$

The resistors R_{22} and R_{23} used as voltage divider are selected to provide the desired voltage V_{BB} at the output of op amp U6 which is used as buffer is given as

$$V_{BB} = V_{DD}\,R_{22}/\,(R_{22}+R_{23}) + V_{SS}\,R_{23}/\,(R_{22}+R_{23}) \tag{3.53}$$

As the devices M1 and M2 are n-channel devices, V_{BB} should be negative.

The precision linear floating VCR schematic shown in Fig. 3.4 has its control parameters as v_{C1}, v_{C2}, v_{C3}, and R_1. This circuit can also be realized by replacing voltage source v_{C2} and resistor R_1 by the current source i_{C2} with $i_{C2} = i_1$, as shown in Fig. 3.5. This

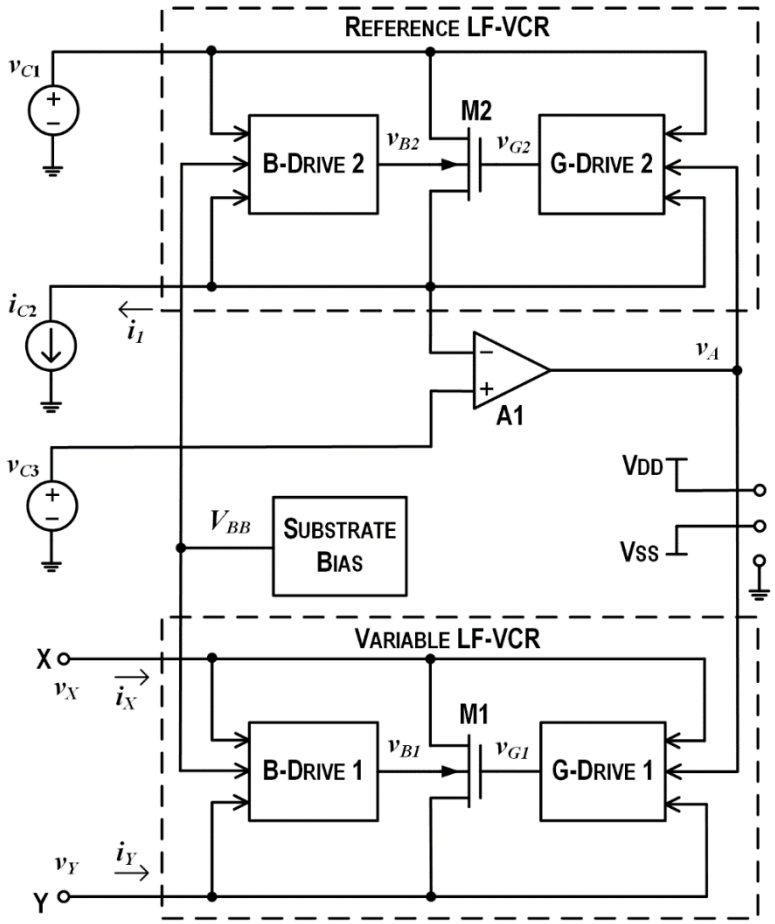


Fig. 3.5 Circuit for realization of NMOS based precision linear floating VCR using current control

type of implementation is particularly suited for current mode circuits. Replacing $(v_{C3} - v_{C2}) / R1$ by i_{C2} in (3.38) the resistance across the X and Y terminals of variable LF-VCR is given as

$$R_{XY} = \frac{v_{C1} - v_{C3}}{i_{C2}} \tag{3.54}$$

The precision linear floating VCR shown in Fig. 3.3 is realized using two n-channel MOSFETs M1 and M2 with positive control input v_{C1}, negative control input v_{C2}, and negative substrate bias. Similar VCR circuit can be realized using two p-channel MOSFETs with negative control input v_{C1}, positive control input v_{C2}, and positive substrate bias. These two precision LF-VCRs one with n-channel and other with p-channel MOSFETs can be connected in parallel to further improve the linearity of combined VCR circuit. The realization of the combined VCR circuit is shown in Fig. 3.6 with two matched n-channel MOSFETs M1 and M2, connected in parallel with two matched p-channel MOSFETs M3 and M4, all with independent substrates. All the G-drive and B-drive blocks shown in Fig. 3.6 are used to add common mode voltage to the control voltage and substrate bias, similar to the

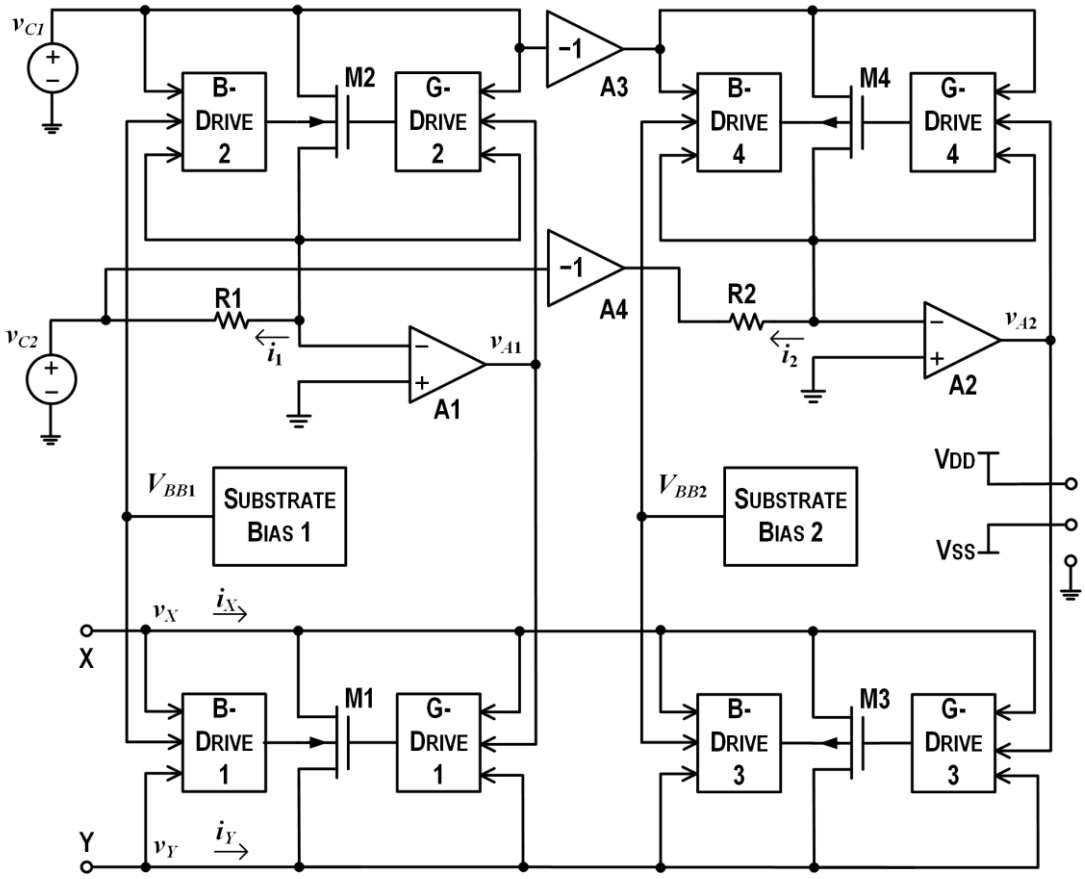


Fig. 3.6 Block diagram of CMOS based precision linear floating VCR

realization as shown in Fig. 3.3. The external control inputs v_{C1} and v_{C2} are applied to the control terminals of NMOS based reference LF-VCR (using M2) to vary the resistance across resistance terminals of NMOS based variable LF-VCR (drain source terminals of M1). These inputs v_{C1} and v_{C2} are inverted using inverting amplifiers A3 and A4 respectively, and applied to the control terminals of PMOS based reference LF-VCR (using M4) to vary the resistance across resistance terminals of PMOS based variable LF-VCR (drain source terminals of M3). The substrate bias 1 block is used to provide substrate bias V_{BB1} for the VCR circuit with n-channel MOSFETs M1 and M2. Substrate bias 2 to provide V_{BB2} for VCR circuit with p-channel MOSFET M3 and M4. Resistance of this VCR circuit vary across X and Y terminals due to parallel combination of n-channel and p-channel based LF-VCR.

The variable LF-VCR shown in Fig. 3.3 tracks the resistance of the reference LF-VCR. This technique is used in resistance mirror circuits. The schematic shown in Fig. 3.7 is the realization of resistor mirror circuit with two variable LF-VCRs, indeed more than two variable resistors can also be used in mirroring. The variable LF-VCR 1 using M1A provides varying resistance across X1 and Y1 terminals. The variable LF-VCR 2 using M1B provides

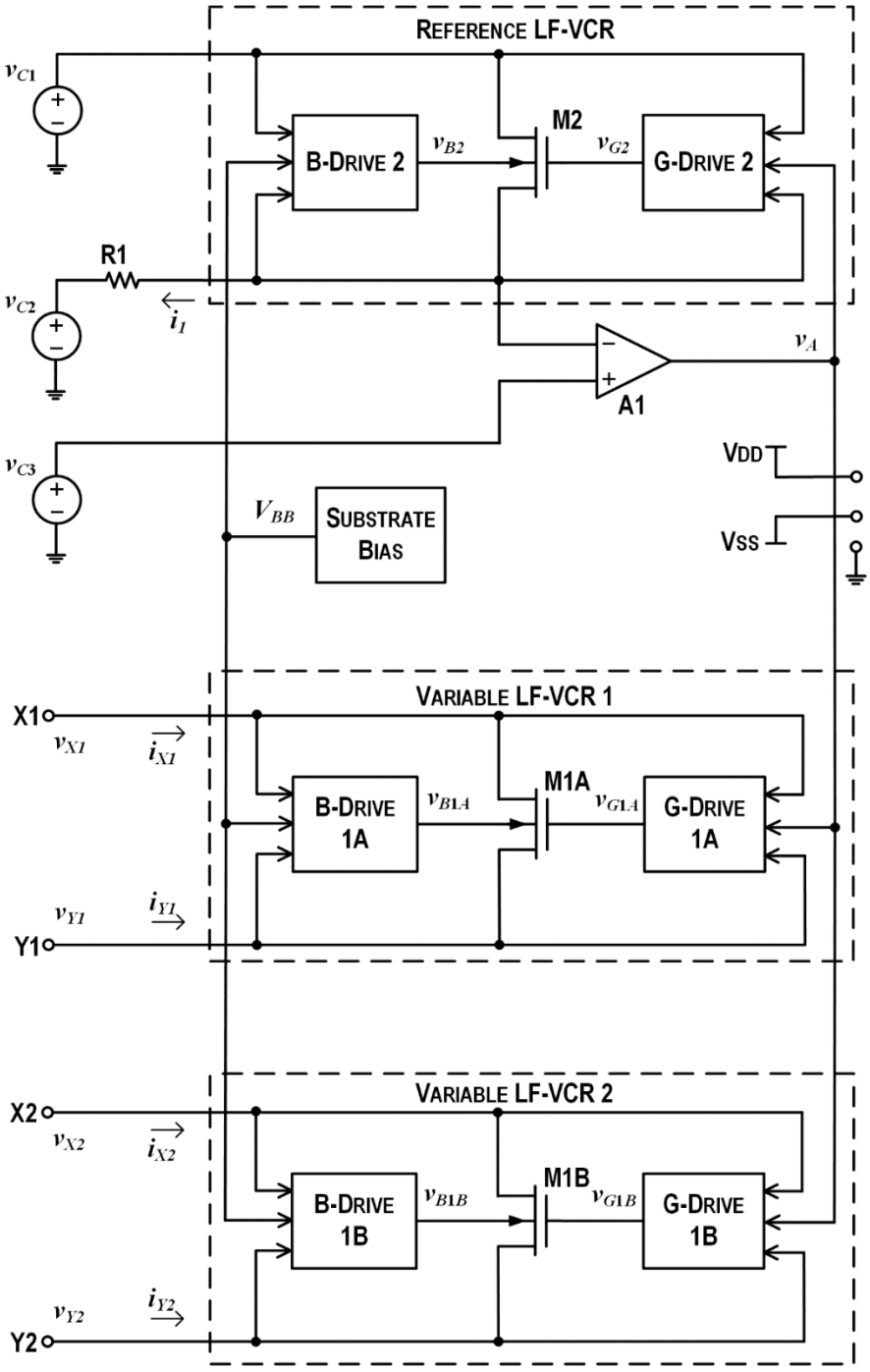


Fig. 3.7 Block diagram of mirroring of LF-VCR

varying resistance across X2 and Y2 terminals. These two LF-VCRs mirror the resistance across the drain and source terminals of reference LF-VCR using M2. The MOSFETs M1A, M1B and M2 are matched with independent substrate terminals, with external substrate bias V_{BB} provided to all of them.

G. Bret [34] presented a technique where the operating range of MOSFET based voltage controlled resistor can be increased by scaling the resistance due to MOSFET. Using

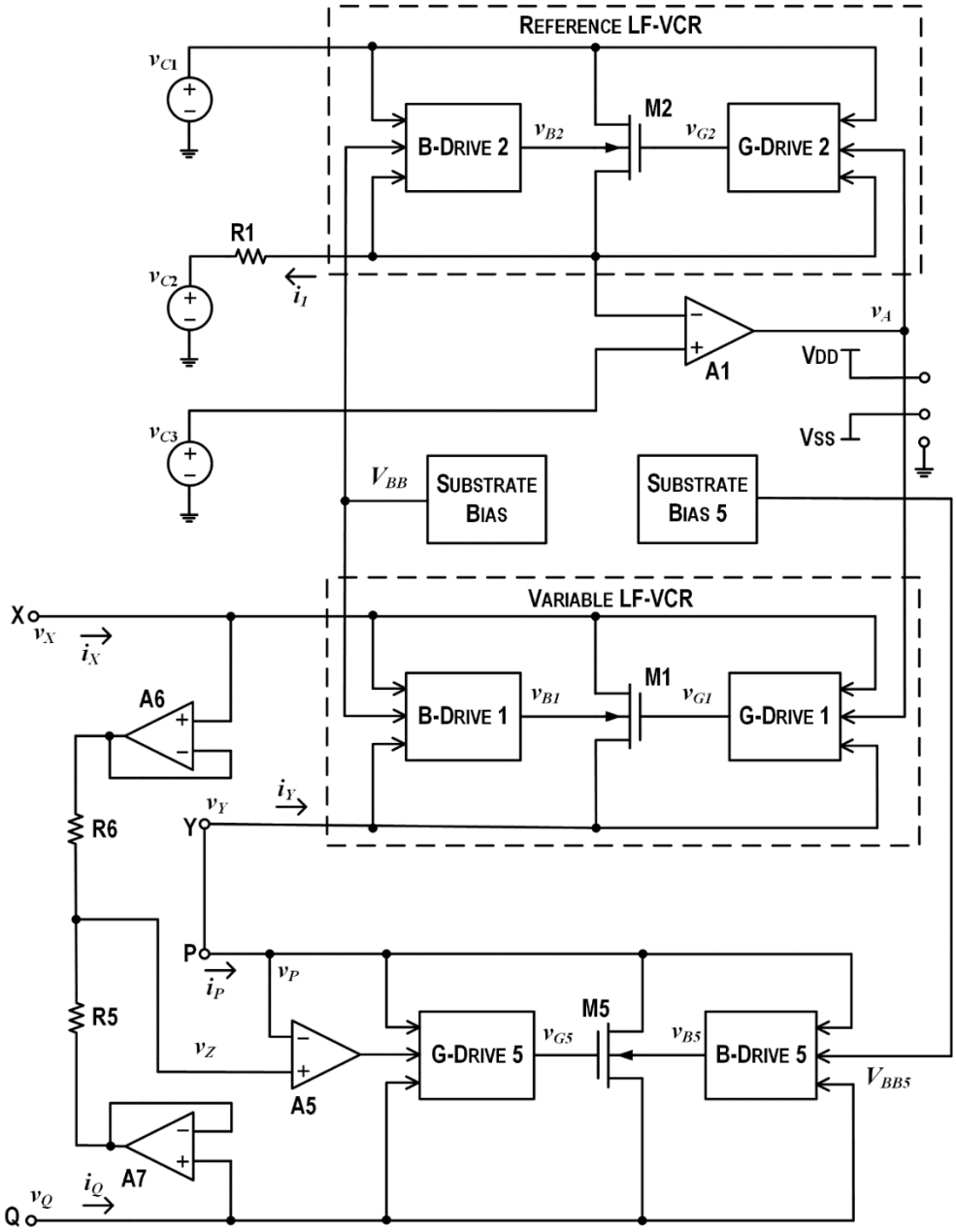
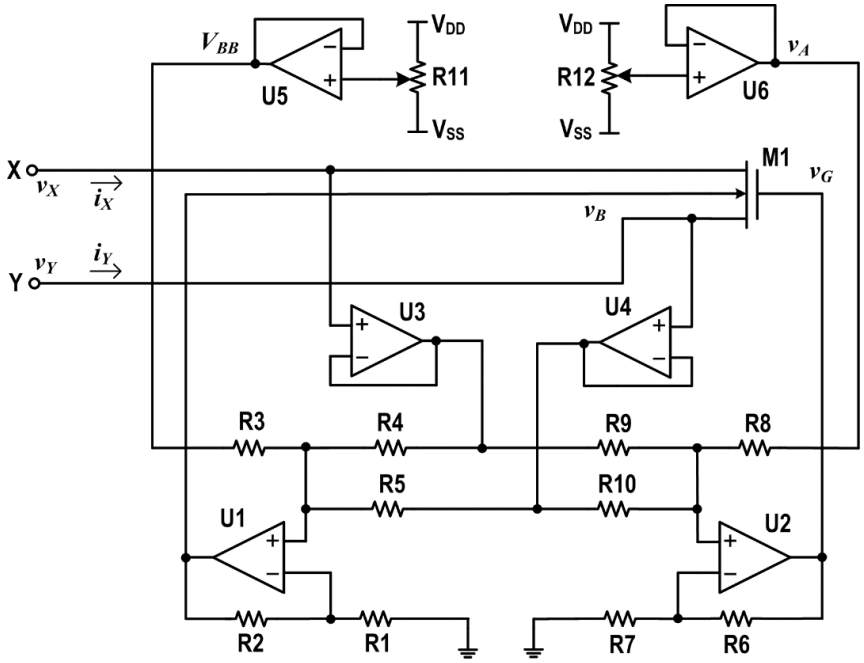


Fig. 3.8 Block diagram of LF-VCR with resistance scaling to increase the range of operation

this technique combined with the VCR schematic shown in Fig. 3.3, a VCR schematic with increased (scaled) linearity range is shown in Fig. 3.8. The VCR circuit is realized using reference LF-VCR (using M2) and variable LF-VCR (using M1) which are similar as in Fig. 3.3, with LF-VCR scaler (using M5) connected to the circuit. All the G-drive and B-drive blocks shown in Fig. 3.8 are used to add common mode voltage to the control voltage and substrate bias. The drain and source terminals (X and Y) of M1 are connected in series with the drain and source terminals (P and Q) of M5 to provide the net resistance across X and Q terminals. The voltage applied across X and Q terminals (v_{XQ}) is scaled down to voltage



R1 = R3 = R6 = R7

R2 = R5 = R1/2

R4 = R8 = 2R1

Fig. 3.9 LF-VCR circuit for practical testing

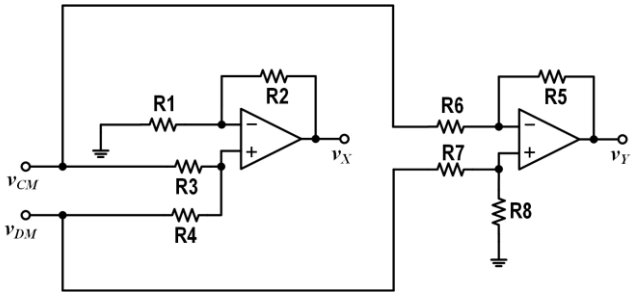
v_Z using voltage divider circuit comprising resistors R6 and R5, and buffers A6 and A7. Op amp A5 provides the control input to M5 and forms a negative feedback loop with M5 leading to $v_Z = v_P$. Thus, a scaled down voltage is applied across the X and Y terminals of variable LF-VCR (using M2) which is in the limit of range of operation of M2. In this case, M5 need to have a required range of channel resistance and voltage range of operation, and need not to be matched with M1 and M2.

3.4 Test results

The circuit as shown in Fig. 3.9 was bread boarded and tested to examine the properties of a linear floating VCR using MOSFET M1 (ALD1106) as VCR, with source drain (SD) bootstrapping of the gate and substrate terminals. The substrate voltage v_B at the substrate terminal of M1 with substrate bias V_{BB} added to common mode voltage is given as

$$v_B = V_{BB} + \frac{v_X + v_Y}{2} \tag{3.55}$$

The voltage v_G at the gate terminal of M1 with control voltage v_A added to common mode voltage is given as



$$R_1 = R_3 = R_6 = R_7$$
$$R_2 = R_5 = R_1/2$$
$$R_4 = R_8 = 2R_1$$

Fig. 3.10 Circuit to generate v_X and v_Y from given v_{DM} and v_{CM}

$$v_G = v_A + \frac{v_X + v_Y}{2} \tag{3.56}$$

The voltages v_{DM} and v_{CM} represent the differential mode and common mode voltages respectively, for the terminals voltages v_X and v_Y, and are given as the following:

$$v_{DM} = v_X - v_Y \tag{3.57}$$

$$v_{CM} = \frac{v_X + v_Y}{2} \tag{3.58}$$

For experimentally testing the circuit operation for different combinations of v_{DM} and v_{CM}, the terminal voltages v_X and v_Y were obtained for given v_{DM} and v_{CM} using adder circuit as shown in Fig. 3.10, and given as

$$v_X = v_{CM} + \frac{v_{DM}}{2} \text{ and } v_X = v_{CM} - \frac{v_{DM}}{2}$$

3.4.1 Test results of floating VCR

The LF-VCR circuit shown in Fig. 3.9. was tested with the following four cases:

Case 1 (no bootstrapping): $v_G = v_A,\ v_B = v_{BB}$ (3.59)

Case 2 (SD bootstrapping for gate): $v_G = v_A + v_{CM},\ v_B = v_{BB}$ (3.60)

Case 3: (SD bootstrapping for gate and S bootstrapping for substrate):

$$v_G = v_A + v_{CM},\ v_B = V_{BB} + \min(v_X, v_Y) \tag{3.61}$$

Case 4: (SD bootstrapping for gate and substrate):

$$v_G = v_A + v_{CM},\ v_B = v_{BB} + v_{CM} \tag{3.62}$$

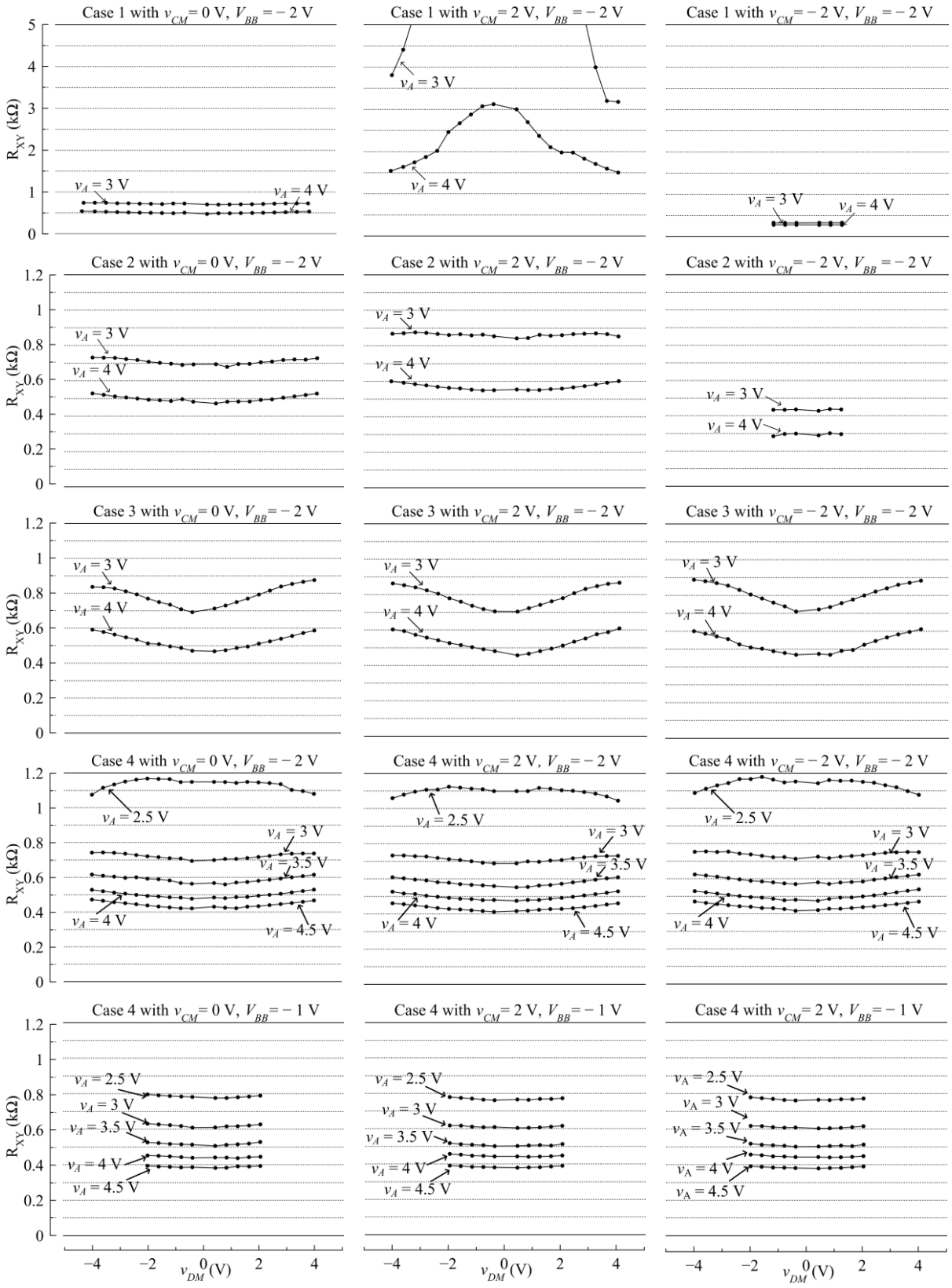


Fig. 3.11 Plots of R_{XY} vs v_{DM} with v_A ranging from 2.5 V to 4.5 V, $V_{BB} = -2$ V and $V_{BB} = -1$ V, for floating VCR for v_{CM} = 0 V, 2 V and −2 V.

Fig. 3.11 shows R_{XY} vs v_{DM} plots for the above cases by sweeping v_{DM} from negative to positive values with the constraints mentioned in (3.43). The measurements were taken for $V_{BB} = -2$ V, with common mode voltages $v_{CM} = -2$ V, 0 V, and 2 V and the values of v_A ranging from 2.5 V to 4.5 V for all the above-mentioned cases. A set of plots is also obtained for the case 4 for $V_{BB} = -1$ V. In the case 1, with no addition of common mode voltage, there is a large variation in R_{XY}. The variation in R_{XY} is reduced in the case 2, with the common mode voltage added to the gate terminal. R_{XY} remains constant in both the cases 3 and 4. However, the variation in the R_{XY} in the case 3 is more compared to the case 4, where common voltage is added to both the gate and substrate terminals i.e., SD bootstrapping for both gate and substrate terminals. Thus, the linearity of the circuit is improved by adding v_{CM} to both gate and substrate terminals. The curves of R_{XY} are shifted for the case 1 and the case 2 for three different values of v_{CM} (0 V, 2 V, − 2 V), whereas for the case 3 and the case 4, the curves are independent of the v_{CM}. Thus, bootstrapping of the gate and substrate terminals makes the VCR circuit to be independent of the change in the v_{CM}. It is also seen that the resistance R_{XY} becomes more constant with an increase in the control voltage v_A, indicating that linearization of the channel resistance improves under strong inversion. As in the case 4, the set of plots with $V_{BB} = -1$ V, the VCR circuit can be operated for the v_{DM} range of ± 2 V which is in accordance with (3.43) and also the resistance values are lower compared to the one with $V_{BB} = -2$ V (operating range of v_{DM} is ± 4 V) for the same values of v_A. As V_{BB} is decreased with reference to ground, the resistance is increased. The value of V_{BB} determines the range of v_{DM} that can be applied i.e. with lower values of V_{BB} the range of differential voltage v_{DM} that can be applied is increased.

3.4.2 Test results of grounded VCR

The VCR circuit shown in Fig. 3.9 is connected as grounded (single-ended) VCR by connecting Y terminal to ground i.e. $v_Y = 0$ V. The voltage v_X is applied at X terminal and swept with the constraint as in (3.43). The voltages at gate and substrate terminals of M1 are given as

$$v_G = v_A + \frac{v_X}{2} \tag{3.63}$$

$$v_B = V_{BB} + \frac{v_X}{2} \tag{3.64}$$

The circuit was tested with the following three cases

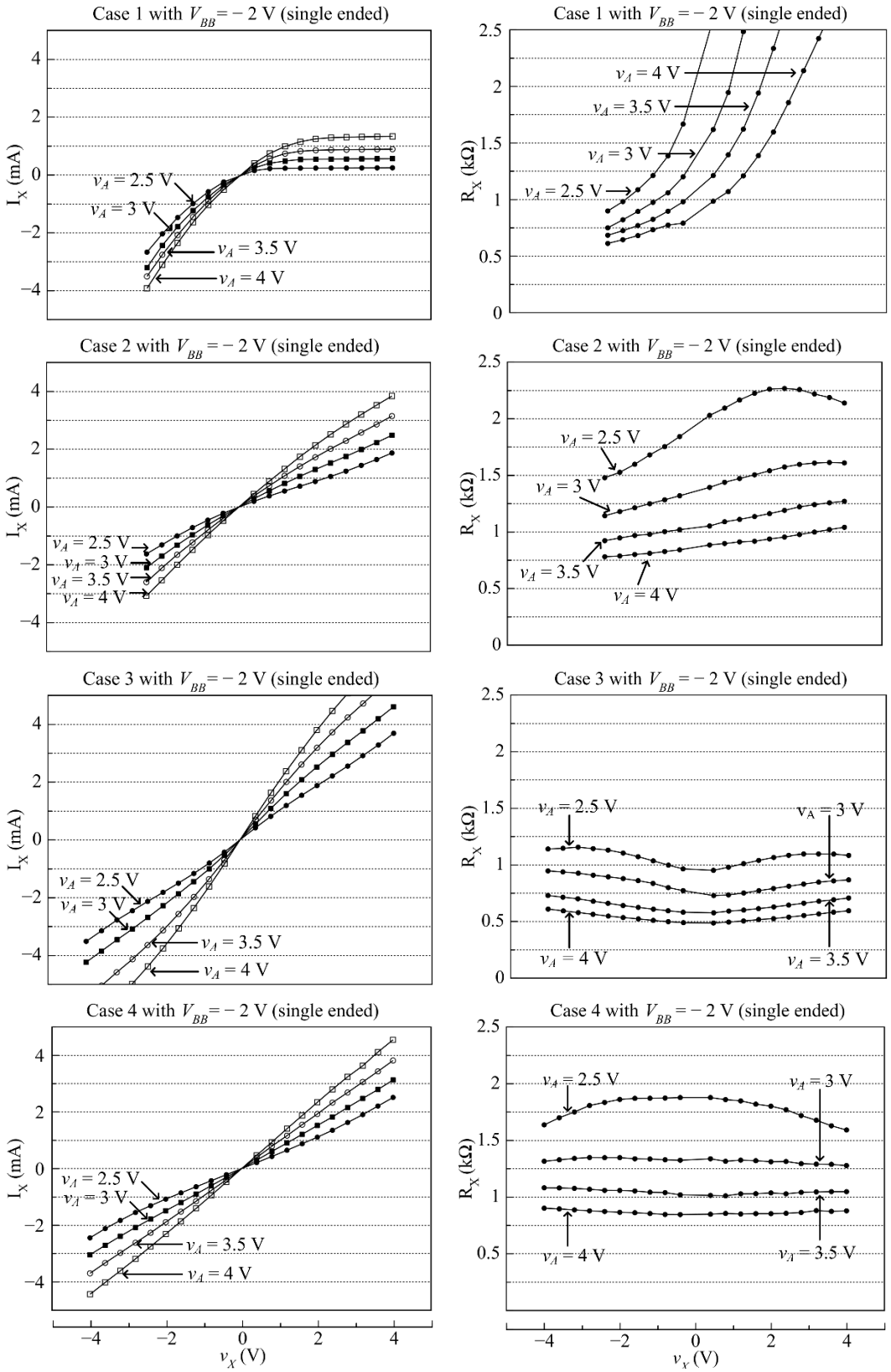


Fig. 3.12 Plots of R_{XY} vs v_X , and I_X vs v_X with v_A ranging from 2.5 V to 4 V, $V_{BB} = -2$ V, for grounded VCR

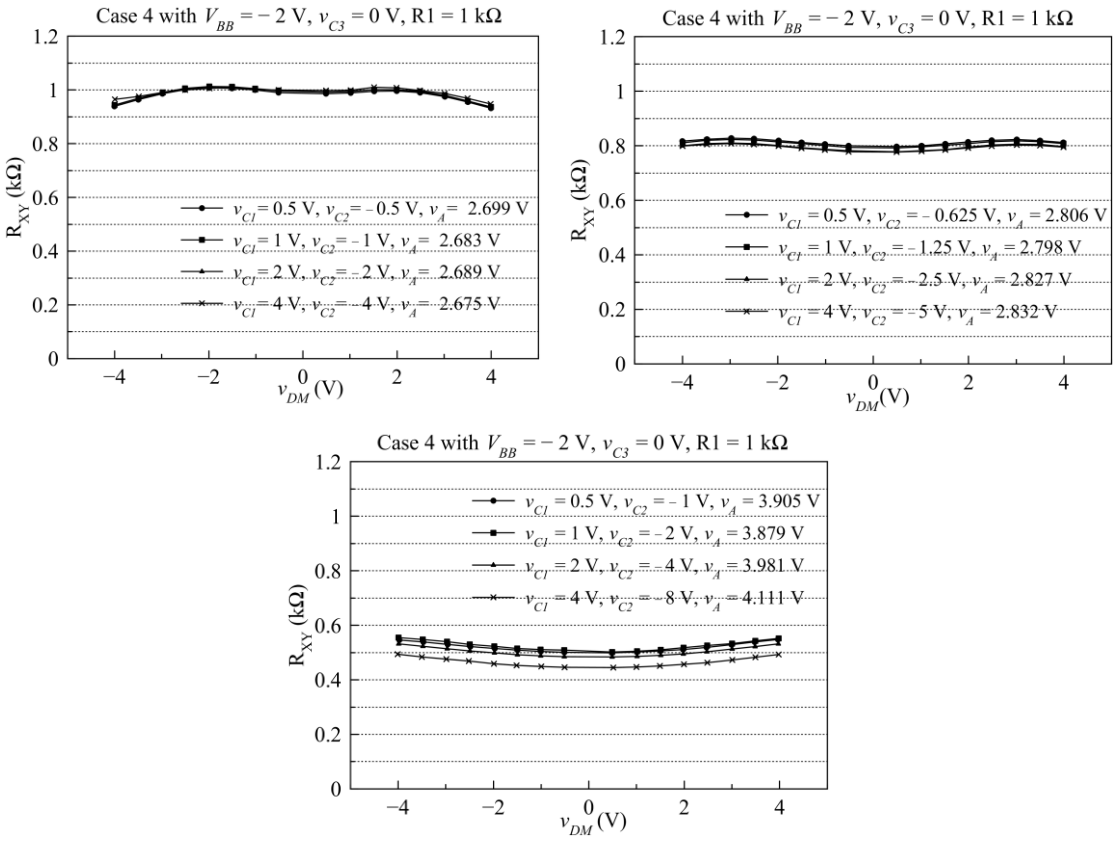


Fig. 3.13 Plots of R_{XY} vs v_{DM} for precision LF-VCR with combinations of v_{C1} and v_{C2}

Case 1 (no bootstrapping): $$v_G = v_A,\ v_B = V_{BB} \tag{3.65}$$

Case 2 (drain bootstrapping for gate): $$v_G = v_A + \frac{v_X}{2},\ v_B = V_{BB} \tag{3.66}$$

Case 3: (drain bootstrapping for gate and source bootstrapping for substrate):

$$v_G = v_A + \frac{v_X}{2},\ v_B = V_{BB} + \min(v_X, v_Y) \tag{3.67}$$

Case 4 (drain bootstrapping for gate and substrate):

$$v_G = v_A + \frac{v_X}{2},\ v_B = V_{BB} + \frac{v_X}{2} \tag{3.68}$$

Fig. 3.12 shows plots of R_{XY} vs v_X , and I_X vs v_X for all the above four cases, with $V_{BB} = -$ 2 V, and the values of v_A ranging from 2.5 V to 4 V. From Fig. 3.12, it could be inferred that for case 4 i.e. SD bootstrapping of both gate and substrate terminals, the curves of resistance R_{XY} remain constant compared to other cases. The curves of current I_X in case 4 are linear compared to the other cases for similar values of v_A applied, i.e. I_X is proportional to the v_X applied.

The precision LF-VCR circuit as shown in Fig. 3.4 was bread boarded and tested to examine the properties of precision linear floating VCR with source drain (SD) bootstrapping of the gate and substrate terminals. Two matched MOSFETs M1 and M2 with independent substrate terminals are used. For this practical testing the non-inverting terminal of op amp U5 is connected to ground (v_{C3} = 0 V). As the common mode voltage v_{CM} is added to both the gate and substrate terminals of both the MOSFET, the voltages v_{B1} and v_{G1} at the substrate and gate terminal respectively of M1 is given as

$$v_{B1} = V_{BB} + v_{CM} \tag{3.69}$$

$$v_{G1} = v_A + v_{CM} \tag{3.70}$$

The voltages v_{B2} and v_{G2} at the substrate and gate terminal respectively of M2 is given as

$$v_{B2} = V_{BB} + \frac{v_{C1}}{2} \tag{3.71}$$

$$v_{G2} = v_A + \frac{v_{C1}}{2} \tag{3.72}$$

As shown in Fig. 3.13, R_{XY} vs v_{DM} plots for the above cases by sweeping drain to source voltage v_{XY} from negative to positive values with the constraints mentioned in (3.43). As given in (3.38), the resistance across X and Y terminals R_{XY} can be controlled by external control voltages v_{C1}, v_{C2} and v_{C3}, and the resistance R_1. In this practical testing, R_{XY} is simulated for the resistance values of 1 kΩ, 0.8 kΩ, and 0.5 kΩ by varying v_{C1} and v_{C2} accordingly, and setting v_{C3} = 0 V and R1 = 1 kΩ, with external common mode voltage fixed to zero (v_{CM} = 0 V). The calculated value of resistance R_{XY} is matched with the measured R_{XY}. It can also be noted from Fig. 3.13 that the R_{XY} remain same for different combinations of v_{C1} and v_{C2} for each set of plots.

3.5 Effect of mismatch in device parameters

The resistance R_{XY} across the X and Y terminal of the precision LF-VCR circuit described in the previous sections, has been obtained with the assumptions that the two MOFETs are matched. For devices with same dimensions and on the same chip, effect of process dependent and temperature related parameter variation will be the same. However, some mismatch may occur due to different location of the devices and dimension related tolerances. Here, an analysis is carried out to obtain an expression for relative error in R_{XY} due to such mismatches.

From the expression for R_{XY} in (3.37), we can write

$$R_{XY}^{-1} = k_1\left(\frac{v_{C3}-v_{C2}}{(v_{C1}-v_{C3})k_2R_1} + V_{TO2} - V_{TO1} - (\alpha_2-\alpha_1)V_{BB}\right) \tag{3.73}$$

The mismatch in the MOSFETs can result in mismatch in the values of V_{TO1} and V_{TO2}, k_1 and k_2, α_1 and α_2. For matched MOSFET with $V_{TO1} = V_{TO2}$, $k_1 = k_2$, and $\alpha_1 = \alpha_2$, the resistance is the same as $R_{DS2,}$ as given in (3.29) and is taken as the error free value of R_{XY} as

$$R_{XYO} = \frac{v_{C1}-v_{C3}}{v_{C3}-v_{C2}}R_1 \tag{3.74}$$

Considering the parameters of the MOSFET M2 as the reference values, the mismatch in the parameters of the MOSFET M1 with those of M2 are given as $\Delta V_T = V_{TO1} - V_{TO2}$, $k_1 = k_2(1+\delta)$, and $\Delta\alpha = \alpha_1 - \alpha_2$. The expression for R_{XY} in (3.37) in terms of that for R_{XYO} in (3.74) can be rewritten as

$$R_{XY}^{-1} = R_{XYO}^{-1}(1+\delta) + k_2(1+\delta)(-\Delta V_T + \Delta\alpha V_{BB}) \tag{3.75}$$

The resistance R_{XY} having $\in$ as the relative error with reference to R_{XYO} can be given as

$$R_{XY} = R_{XYO}(1+\in) \tag{3.76}$$

From the above two equations, the relation between $\in$ and the parameter mismatches can be expressed as the following:

$$(1+\in)^{-1} = (1+\delta)[1 + k_2(-\Delta V_T + \Delta\alpha V_{BB})R_{XYO}] \tag{3.77}$$

Ignoring the second degree error terms, the error is given as

$$\in \approx -\delta + k_2(-\Delta V_T + \Delta\alpha V_{BB})R_{XYO} \tag{3.78}$$

Taking $\Delta\alpha = 0$ for the transistor pair on the same chip, the magnitude of the relative error in R_{XY} can be expressed as

$$|\in| = |\delta| + k_2 R_{XYO}|\Delta V_T| \tag{3.79}$$

From (3.22), R_{XYO} can be given as

$$R_{XYO} = \frac{1}{k_2(v_A - V_{TO2} - (\alpha_2 - 1)V_{BB})} \tag{3.80}$$

Using (3.79) and (3.80), the magnitude of the relative error can be expressed as

$$|\in| = |\delta| + \frac{|\Delta V_T|}{|v_A - V_{TO2} - (\alpha_2 - 1)V_{BB}|} \tag{3.81}$$

From the above equation, the error $\in$ increases as v_A decreases i.e. the precision of the circuit degrades for realizing a higher value resistance.

The device parameters for five different quad n-channel MOSFET ICs (ALD1106) were measured. Each ALD1106 chip has four MOSFETs with a common substrate terminal. For the purpose of device parameter measurement, the MOSFETs were diode connected to keep them in saturation region, and the drain current i_D corresponding to the applied drain-to-

source voltage v_{DS} with V_{BS} = 0 V was measured. The mean values for the 20 transistors (5 chips each with 4 transistors) were

k = 0.661 mA/V^2 and V_{TO} = 0.557 V.

The maximum parameter mismatches for two devices on the same chip were as the following:

Mismatch in V_{TO} : $|\Delta V_T|$ = 0.015 V

Mismatch in k : $|\delta|$ = 0.018

Considering the devices across the 5 chips, the maximum parameter mismatches were

Mismatch in V_{TO} : $|\Delta V_T|$ = 0.101 V

Mismatch in k : $|\delta|$ = 0.088

Thus we see that the parameter mismatches for the devices on the same chip are about one tenth of those for devices across the chips.

With the threshold voltage V_{TO2} = 0.557 V, substrate bias V_{BB} = 0 V, and control voltage v_A = 4 V, the error $|\in|$ given by (3.81) is calculated as the following:

$|\in|$ = 0.022, for devices on the same chip

0.117, for devices on different chips

Thus, the maximum error in the resistance R_{XY} is estimated as 2.2% for the devices on the same chip and as 11.7% for the devices on different chips.

Chapter 4

BIOIMPEDANCE SIMULATOR

4.1 Introduction

Several circuits were developed in our lab to implement the bioimpedance simulator. The bioimpedance simulator developed by Manigandan [27] uses a fixed value resistor to obtain basal impedance which is connected parallel to analog switch for square wave variation of resistance. The circuit was redesigned by Naidu [28] by including microcontroller for controlling the analog switches. Venkatchalam [29] replaced analog switch with a digital potentiometer for providing resistance variation as sinusoidal, or other waveform in discrete steps. Patil [30] designed the simulator by extending the frequency range so that the simulator can be used in other applications of bioimpedance measuring instruments e.g. impedance glottography. The simulator designed by Desai [31] used digital potentiometer to achieve change in the resistance, and combinations of analog switches and different values of fixed resistance to set different basal resistance. All these simulators provide resistance variations in discrete steps. As the signal conditioning and signal processing in many impedance measuring instruments involves differentiation of the sensed signal, it is desirable to provide the resistance variation in continuous form. Holani [32] designed the circuit to obtain the variable resistance using matched JFET pair, used as a voltage controlled resistor (VCR) by controlling the voltage at the gate terminal of JFET. The circuit was able to generate resistance variation in continuous form. The basal resistance was obtained by selecting fixed value resistors by analog switches. The parameters for simulator i.e. frequency and amplitude of variable resistance, and basal value resistance were set using PC based GUI. Debbarma [33] also designed the simulator circuit using matched JFET pair, and included wireless transmission of parameters to simulator from PC using Bluetooth module. He also investigated VCR circuits using matched MOSFET pair. Based on these earlier developments, the bioimpedance simulator is designed to provide continuous variation in the simulated resistance in a precise manner and with wirelessly setting of the simulation parameters.

4.2 Bioimpedance simulator

The bioimpedance simulator comprises of four circuit blocks: resistance variation circuit, controller circuit, Bluetooth module, and power circuit, as shown in Fig. 4.1. The resistance is realized across the XY terminal using VCR circuit providing variable resistance R_v connected in parallel with a fixed resistance R_o across the XY terminals. The VCR circuit realizes the variable resistance R_v, which varies in accordance with the control signals

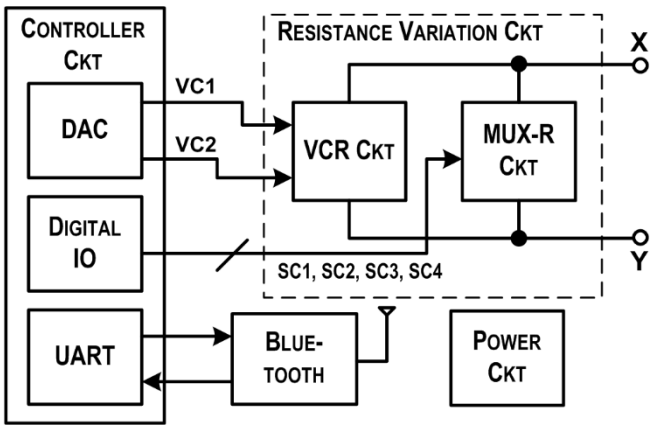


Fig. 4.1 Block diagram of bioimpedance simulator

v_{C1} and v_{C2}, from the DAC outputs of the controller circuit. The basal resistance R_o is realized using a series combination of fixed value resistances and an analog multiplexer (MUX). The select lines viz. SC1, SC2, SC3 and SC4 of MUX are connected to the digital IO pins of the controller circuit. Using these select lines, MUX selects a series combination of fixed value resistors to provide R_o. The parameters of the simulator such as amplitude and frequency of control voltages v_{C1} and v_{C2}, and value of R_o are transferred wirelessly to the Bluetooth module of simulator, using the GUI based controlling program on a PC or other computing device with a Bluetooth wireless interface. The power supply circuit uses a 5V DC source to provide power supply to the resistance variation circuit, controller circuit, and Bluetooth module. These blocks are described in the subsequent sections.

4.3 Resistance variation circuit

he resistance variation circuit comprises of the VCR circuit and the MUX circuit connected in parallel across the X and Y terminals. The time-varying resistance R_v is in parallel to basal resistance R_o. R_v is realized using VCR circuit, implemented using MOSFET pair and R_o is realized using MUX and fixed value resistor network. VCR and MUX circuits are described in the following subsections.

4.3.1 Voltage controlled resistor (VCR) circuit for setting variable resistance R_v

The variable resistance R_v is set across XY terminal using matched MOSFET pair. The schematic of VCR is shown in Fig. 4.2. It uses two ICs ALD1106 (Analog Linear Devices) [35] as M1A and M2A. Each IC has four MOFET devices with common substrates. Since our circuit requires independent MOSFET devices with independent substrates, two such ICs are used, with one transistor used from each. This means that the two devices may

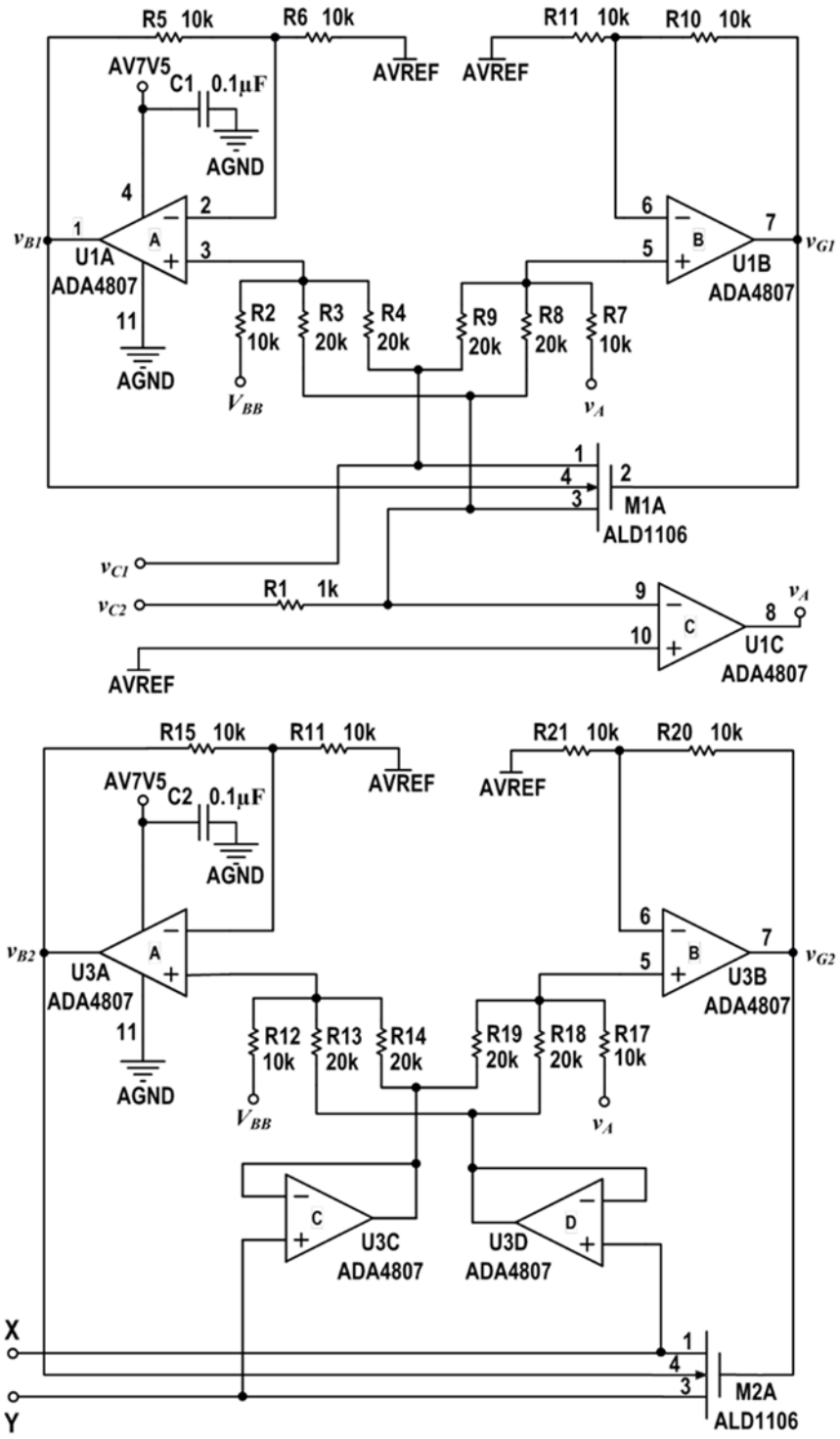


Fig. 4.2: VCR circuit using matched MOSFET pair

not a matched pair, introducing some errors. The control signals v_{C1} and v_{C2} are applied to control the drain-to-source resistance of M1A. The drain-to-source resistance of MOSFET M2A is the variable resistance R_v across the X and Y terminals. The op amp U1C forms a

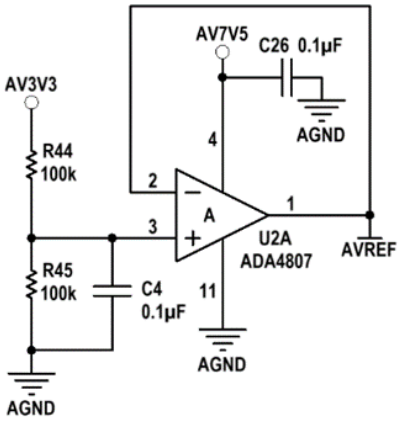


Fig. 4.3: Reference bias voltage AVREF generator

negative feedback loop with M1A. The op amp used is IC ADA4807 (Analog Devices) [40] as U1, U2 and U3 is a rail-to-rail input and output quad op amp with −3 dB bandwidth of 28 MHz for gain = +1 and V_{OUT} = 2 V p-p, slew rate of 225 V/µs, and typical quiescent supply current of 1 mA. The source and drain terminal voltages of M1A (A_{VREF} and v_{C1}) and M2A (v_X and v_Y) are added with the output voltage v_A of U1C to obtain the voltage at gate terminals v_{G1} and v_{G2} of M1A and M2A respectively, for the purpose of source-drain (SD) bootstrapping. The voltages v_{G1} and v_{G2} are given as

$$v_{G1} = v_A + \frac{v_{C1} + v_{C3}}{2} - A_{VREF} \tag{4.1}$$

$$v_{G2} = v_A + \frac{v_X + v_Y}{2} - A_{VREF} \tag{4.2}$$

Similarly, SD bootstrapping is used for body substrate terminal by adding source and drain terminal voltages to obtain the voltage at substrate terminals v_{B1} and v_{B2} of M1A and M2A with V_{BB}. The voltages v_{B1} and v_{B2} are given as

$$v_{B1} = V_{BB} + \frac{v_{C1} + v_{C3}}{2} - A_{VREF} \tag{4.3}$$

$$v_{B2} = V_{BB} + \frac{v_X + v_Y}{2} - A_{VREF} \tag{4.4}$$

To implement the bootstrapping, the op amps U1A, U1B for M1A, and U3A, U3B for M2A are used as voltage adders. The control voltages v_{C1} and v_{C2}, and op amp output voltages are with respect to the reference potential A_{VREF}. As the external voltage input applied across the X and Y terminal is limited between 0 to 3.3 V, A_{VREF} is set as 1.65 V i.e.

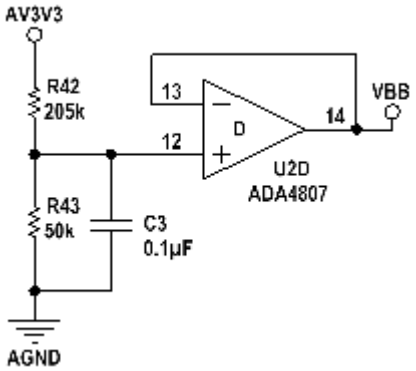


Fig. 4.4: Voltage for body substrate terminal V_{BB} generator

half of 3.3 V. Potential divider with equal valued resistors R44 and R45, and op amp U2A connected as voltage follower is used to obtain A_{VREF}, as shown in Fig. 4.3. The capacitor C4 is used to filter supply noise. The voltage V_{BB} is set as 0.65 V with reference to GND and −1 V with reference to A_{VREF}. It is obtained using potential divider resistors R42 and R43, and op amp U2D connected as voltage follower as shown in Fig. 4.4. The capacitor C3 is used to filter supply noise.

The variable resistance R_V across the X and Y terminals is given as

$$R_{XY} = \frac{(v_{C1} - A_{VREF})}{(A_{VREF} - v_{C2})} \times R1 \tag{4.5}$$

Practical tests were performed using MOSFET keeping V_{BB} as −1 V with reference to A_{VREF}, v_{C3} as A_{VREF}, v_{C2} as −1 V, v_{C1} as 1 V both with reference to A_{VREF}, and R1 = 1 kΩ. The value of R_v obtained using these values in (4.1) is 0.5 kΩ. The measured v_A value was 5.25 V. As mentioned in the previous chapter, that for lower value of R_v (R_{XY}) the value of output voltage v_A of U1C is higher. Thus, considering these constraints, the supply for op amps was chosen to be 7.5 V.

4.3.2 Analog Multiplexer circuit for setting basal resistance R_o

An analog multiplexer (MUX) is used to set the basal resistance R_o across the X and Y terminals. The resistance R_o is obtained by connecting series combination of fixed value resistors which are selected by the MUX select lines. As shown in Fig. 4.5, two 4:1 analog multiplexers IC ADG1604 (Analog Devices) [35] are used as U10 and U11. This IC can operate from 3.3 V to 16 V single supply with rail-to-rail operation. In the current design, a

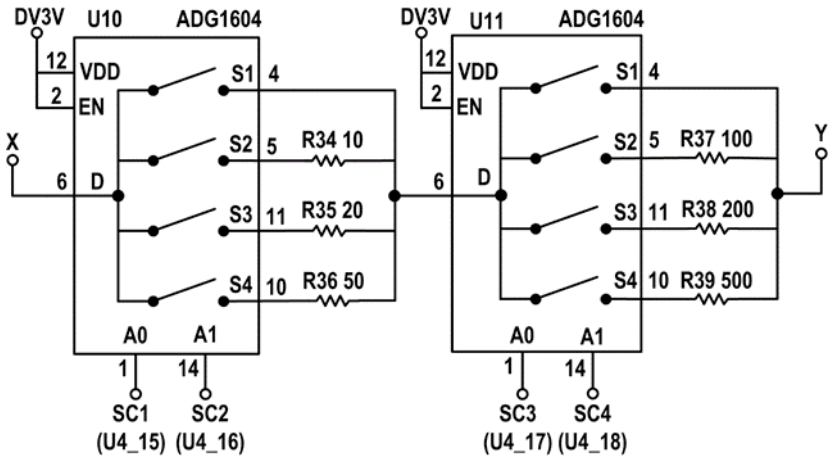


Fig. 4.5: MUX circuit with resistance combination

supply of 3.3 V is used. The internal switches of the multiplexer have a typical on-resistance of 1 Ω. The voltage levels at select lines of multiplexer are compatible with 3.3 V logic levels. The select lines SC1, SC2, SC3, and SC4 of multiplexer are connected to the IO pins RB6 (U_15), RB7 (U_16), RB8 (U_17), RB9 (U_18) of microcontroller as shown in Fig. 4.5. The basal resistance R_o is selected via the microcontroller which uses the select lines to select one of the four internal switches (S1, S2, S3, and S4) of the multiplexer. Fixed value resistors are connected at one end of the internal switches in multiplexer. With four select lines SC1 and SC2 of U10, and SC3 and SC4 of U11, 16 possible combinations of basal resistance R_o can be obtained across the X and Y terminals. Table 4.1 shows the sixteen combinations of the four select lines, with select line high shown as logic '1' and low as logic '0'. For each combination, the corresponding internal switch selected for U10 and U11, and the simulated basal resistance R_o are shown.

4.4 Controller circuit

The controller circuit is designed using 16-bit digital signal controller IC dsPIC33FJ128GP802 (Microchip) [41] as U4, with on chip audio DAC, and internal UART. Its supply voltage is 3.3 – 3.6 V. The microcontroller DAC is used to generate control signals v_{C1} and v_{C2} for the VCR circuit. Internal UART for serial interface with Bluetooth module, and digital IO pins are used for generating the control signals for select lines SC1, SC2, SC3, and SC4 of MUX circuit as shown in Fig. 4.6. The digital supply pin VDD is connected to the digital 3.3 V supply (DV3V3) and the analog supply pin AVDD is connected to the analog 3.3 V supply (AV3V3) with decoupling capacitors C6 and C7, respectively. Capacitors C8

Table 4.1. Values of R_o for different values of select line inputs of MUX

MUX select lines				Switch selected		R_O (Ω)
SC4	SC3	SC2	SC1	U11	U10	
0	0	0	0	S1	S1	0
0	0	0	1	S1	S2	10
0	0	1	0	S1	S3	20
0	0	1	1	S1	S4	50
0	1	0	0	S2	S1	100
0	1	0	1	S2	S2	110
0	1	1	0	S2	S3	120
0	1	1	1	S2	S4	150
1	0	0	0	S3	S1	200
1	0	0	1	S3	S2	210
1	0	1	0	S3	S3	220
1	0	1	1	S3	S4	250
1	1	0	0	S4	S1	500
1	1	0	1	S4	S2	510
1	1	1	0	S4	S3	520
1	1	1	1	S4	S4	550

and C9 are connected in parallel at VCAP pin to stabilize the on chip regulator of the U4. The $\overline{\text{MCLR}}$ pin of U4 is connected to pin 1 of the connector J1 for resetting U4 with logic 0, and for programming and debugging using R22 and C5 with logic '1'. C5 is discharged using R23 to limit the current drawn in the event of MCLR breakdown. The programming clock (PGEC1) and programming data pins (PGED1) of U4 are connected to the pin 4 and 5 of J1 respectively. The on chip audio DAC of U4 has left and right channels with each having positive and negative outputs. The digital samples of the waveform are pre-stored in the on-chip memory of the microcontroller which are output through the DAC. With sampling frequency f_s, and number of samples stored N, the analog output waveform frequency is $f_o = f_s / N$. DAC uses internal interpolation filter at a sampling rate of 256 f_s during digital-to-analog conversion. Fig. 4.7 shows two differential amplifiers to provide the control voltages v_{C1} and v_{C2} with a gain of 2 and their inputs connected to DAC outputs (v_{C1}^{+}, v_{C1}^{-}, v_{C2}^{+}, v_{C2}^{-}) and also acts as first order lowpass filter for the DAC outputs. The differential output is given as

$$v_{C1} = A_{VREF} + \alpha_1 (v_{C1}^{+} - v_{C1}^{-}) \tag{4.2}$$

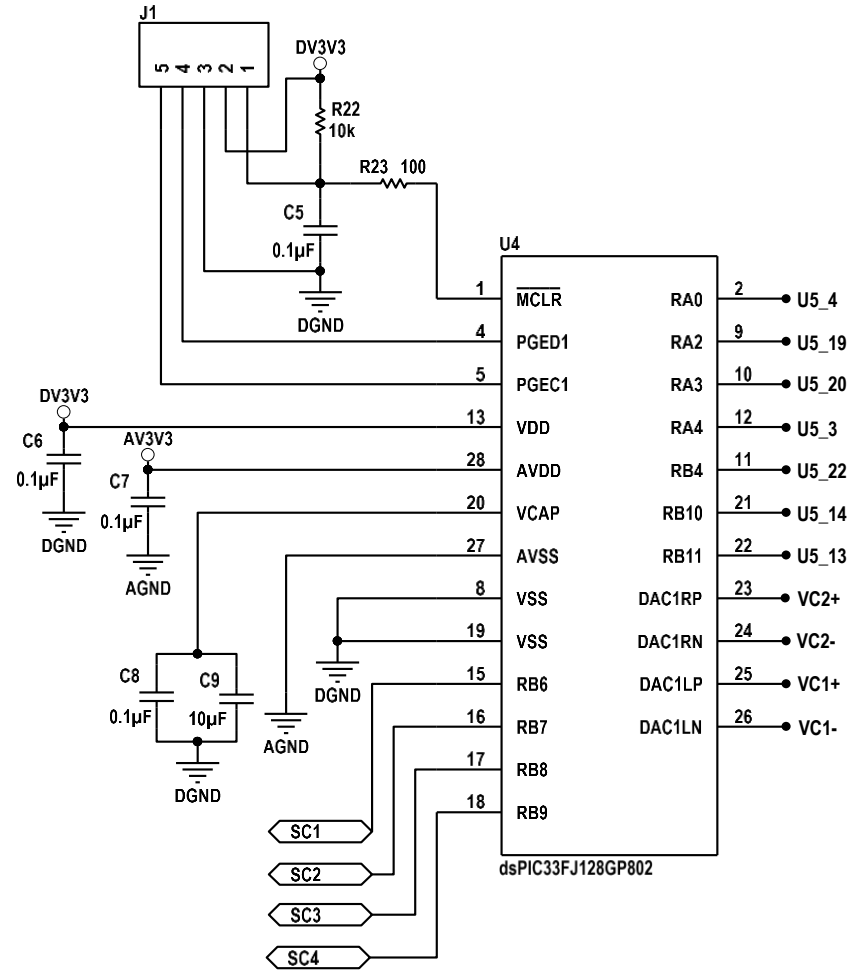


Fig. 4.6: Controller circuit

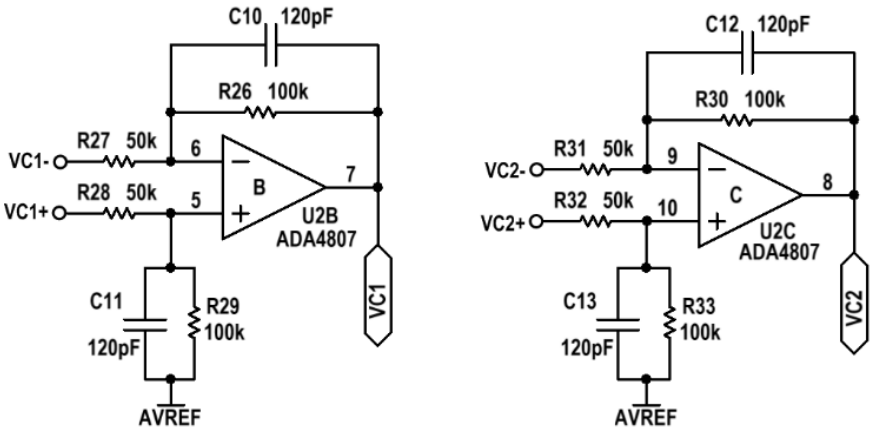


Fig. 4.7: Differential amplifier circuit

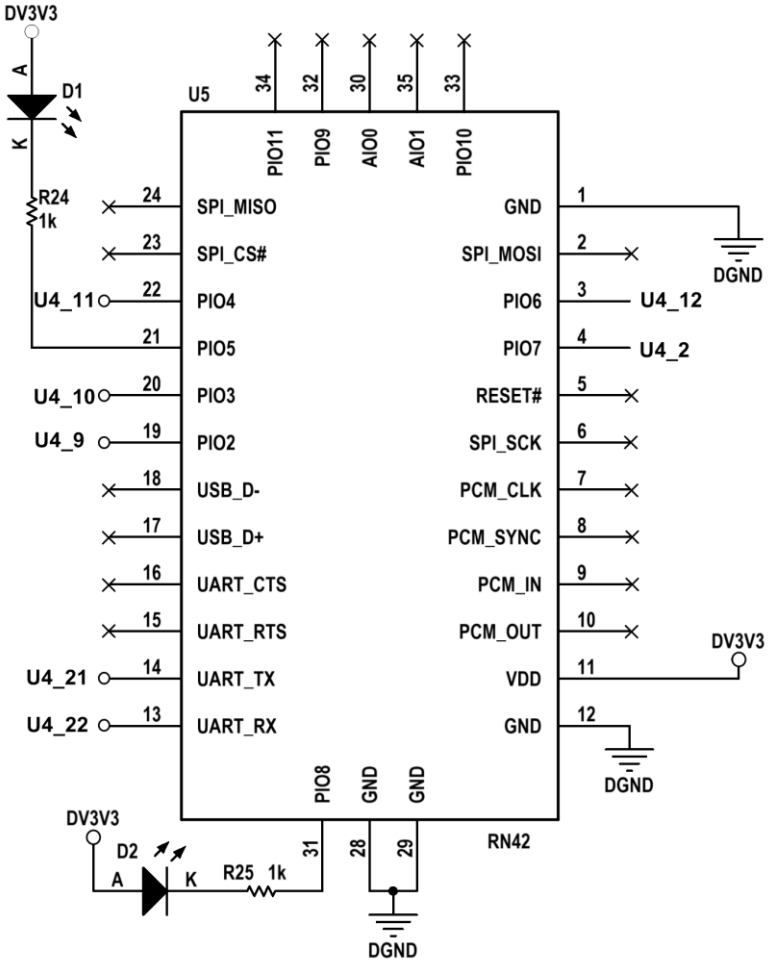


Fig. 4.8 Bluetooth circuit

$$v_{C2} = A_{VREF} + \alpha_2 (v_{C2}^{+} - v_{C2}^{-}) \tag{4.3}$$

The resistor values, for providing differential gain $\alpha_1 = \alpha_1 = 2$ for v_{C1} and v_{C2}, respectively, are selected as

$R_{27} = R_{28} = R_{31} = R_{32} = 50$ kΩ, $R_{26} = R_{29} = R_{30} = R_{33} = 100$ kΩ

Assuming the output waveform having spectral components up to f_m, the cut-off frequency f_c of the lowpass filter should be selected as $f_m << f_c << 256 f_s - f_m$ to smoothen the output waveform without distorting it. Since $256 f_s >> f_m$, the condition for the range of f_c can be taken as $10 f_m < f_c < 25.6 f_s$. Thus, the cut-off frequency is given as $f_c \approx 10 f_m$, and for the sampling frequency it is given as $f_s > (2 f_m, f_c / 25.6)$. With the resistors R_{26}, R_{29}, R_{30}, and R_{33} selected as 100 kΩ, and capacitors C_{10}, C_{11}, C_{12}, and C_{13} selected as 120 pF shown in

Fig. 4.7, the cut-off frequency f_c is 13.2 kHz. Thus, with this cut-off frequency, the frequency f_o up to 1.32 kHz of output waveform can be smoothened faithfully.

4.5 Bluetooth module

Bluetooth is used to wirelessly receive the simulation parameters from a PC or other computing device using a graphical user interface (GUI). The Bluetooth module is connected to the UART pins of the microcontroller U4 for serial communication to receive the parameters sent by the PC as shown in Fig. 4.8. Bluetooth module RN42 (Roving Networks) [42] is used with 3.3 V digital supply (DV3V3) with reference to DGND. LED D1 is connected to pin PIO5, with its blink speed indicating connection status as discoverable mode, command mode and connected mode. The resistor R24 is connected to limit the current through LED D1. LED D2 is connected to PIO8 to indicate the status of UART transmission and receiving activity. Pin PIO2 gives the status as high if the Bluetooth is connected and low otherwise. UART transmitting (UART_TX) and receiving pin (UART_RX) are connected to the RB10 and RB11 pins of U4 for serial communication. Pin PIO7 of U5 is used to set the default baud rate of 115.3 kbps.

4.6 Power Circuit

The op amps, controller circuit and the Bluetooth module are powered by separate regulators. The power circuit with 3.3 V and 7.5V labelled as AV3V3 and AV7V5 respectively for analog operation, and 3.3 V labelled as DV3V3 for digital operation is shown in Fig. 4.8. The analog module of U4 is powered with AV3V3 with reference to AGND and digital module of U4 is powered by DV3V3 with reference to DGND. Op amps U1, U2 U3 are powered by AV7V5 with respect to AGND and the Bluetooth module is powered by DV3V3 with respect to DGND. The current requirements of these are estimated based on the requirement of individual components used in the simulator and are shown in Table 4.2.

To electrically isolate the simulator from AC mains and to reduce the external pickups, the circuit is powered by an isolated 5 V DC supply, from a rechargeable power bank with 5 V output is used. The output of the power bank is connected via USB mini port J2 on the simulator board as shown in Fig. 4.9.

A power bank uses a 4.2 V rechargeable battery and a switching regulator to provide 5 V DC output. This output has significant high frequency ripple, with the ripple amplitude and frequency of ripples varying from power bank to power bank. Removal of ripples is achieved by connecting an LC filter at the output of J1 as shown in Fig. 4.9 using inductor L1 and capacitor C14 giving filtered output voltage labelled as V_p. The op amp supply voltage is obtained using a combination of a charge pump doubler and a linear adjustable regulator ICs.

Table 4.2. Estimation of current requirements of the blocks of the bioimpedance simulator

Supply voltage	Component	Current Requirement (mA)
AV7V5	U1: ADA4807	4.4 mA
	U2: ADA4807	4.4 mA
	U3: ADA4807	4.4 mA
	Total	13.2 mA
AV3V3	U4: DSPIC33FJ128GP802	9.0 mA
DV3V3	U5: RN42	50 mA
	U4: DSPIC33FJ128GP802	40 mA
	Total	90 mA

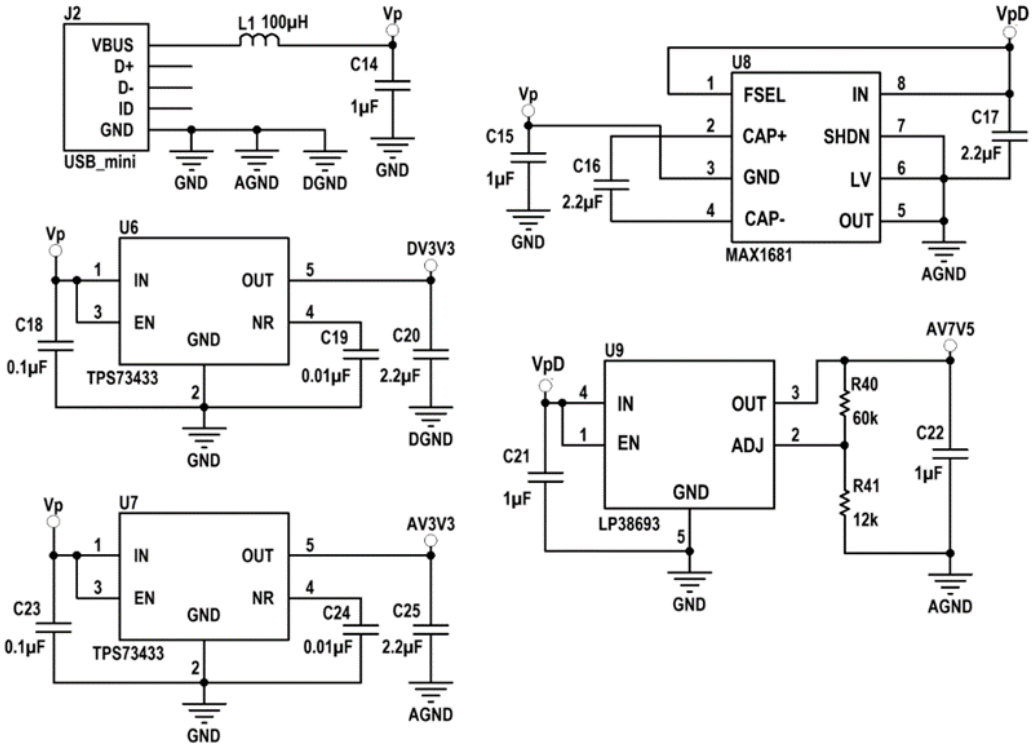


Fig. 4.9: Power supply circuit

The charge pump-based voltage doubler IC MAX 1681 (Maxim Integrated) [36] as U8 doubles the input voltage ranging of 2.0 – 5.5 V to the output voltage with a drop of 400 mV at 125 mA output current with typical 10 mA of supply current required for the IC itself. The unregulated output voltage of U8 is labelled as V_{pD} and it can have value of 3.6 to 10.6 V. To regulate the output of U8, the linear adjustable regulator IC LP38693 (Texas Instruments) [37] as U9 is used with input voltage range of 2.7 – 10 V and low dropout voltage of 250 mV at 500 mA with adjustable output range from 1.25 V to 9 V. The output voltage is set using

external resistors R40 and R41 resulting in a regulated output voltage of 7.5 V labelled as AV7V5 which is provided to the supply pins of op amps U1, U2 and U3. The supply for analog and digital modules of simulator i.e. 3.3 V is obtained using two ICs U6 and U7 respectively. Linear regulator IC TPS73433 (Texas Instruments) [38] has been used. It has fixed output voltage of 3.3 V with a low dropout voltage of 250 mV at 125 mA output current, and quiescent current of 44 µA. The regulated outputs from the two ICs labelled as AV3V3 and DV3V3 are provided to analog and digital modules respectively.

4.7 Microcontroller Program

The two main purposes of the microcontroller in the bioimpedance simulator are to set the basal resistance, and to vary the resistance of VCR circuit. As mentioned in Section 4.3.2, the basal resistance is realized using analog MUX and resistors connected in series combination at the output. The digital IO pins of the microcontroller are connected to the select lines of analog MUX which in turn selects the internal switches of MUX. The microcontroller can be programmed to write the binary values (1 or 0) to set the digital IO pins logic HIGH or LOW values, which is provided to the select lines. Sixteen possible combinations of 4-bit binary values can be given at IO pin to set sixteen values of resistances from 0 to 550 Ω. To vary (or control) the resistance of VCR, analog control waveforms need to be provided. As mentioned in Section 4.4, the DAC outputs are connected to the differential amplifiers, whose outputs provide the control voltages v_{C1} and v_{C2}. The microcontroller program can be used to change the characteristics of the control waveforms such as amplitude, frequency, offset, and shape of the waveform.

The frequency of waveform can be changed by either changing the sampling frequency f_s of DAC, or by selecting the number of samples N in one period. The sampling frequency can be set by modifying the internal registers of the microcontroller i.e. Auxiliary control register (ACLKCON), and DAC1 control register (DAC1CON) which operates on the controller system clock. The frequency of the output waveform can be changed by either performing interpolation or decimation on the samples N stored. In this case decimation method is used, where the samples are dropped to change from low frequency to high. Setting sampling frequency f_s with three different values of 64 Hz, 640 Hz and 6.4 kHz, and fixing the number of samples N = 640, the output waveform frequency $f_o (f_s / N)$ values can be varied from 0.1 Hz to 100 Hz. The DAC module has FIFO buffers of four-word length for both the channels (left and right) and a default buffer, for temporary storage. It outputs the samples for conversion at a fixed sampling frequency. If the FIFO becomes empty, the value in default buffer is used for conversion.

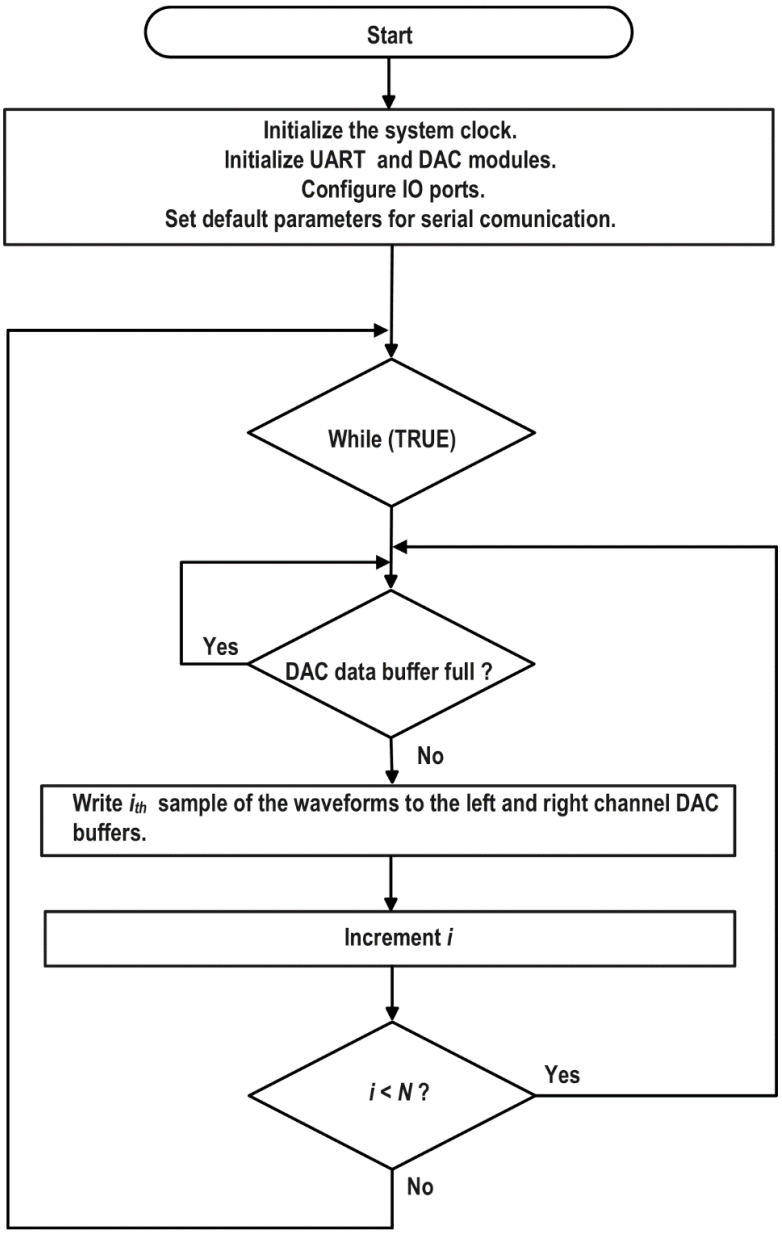


Fig. 4.10: Flow chart of main function

To perform the above operations using the microcontroller, a program is written in embedded C using MPLAB X IDE. The program includes a main function and three interrupt service routines (ISRs). The three ISRs are 'U1RXInterrupt' for receiving the simulation parameters using the UART interrupt, 'DAC1LInterrupt' to control the left DAC channel, and 'DAC1RInterrupt' to control the right DAC channel. The main function includes initialization of the system clock, UART module, DAC module, and infinite loop to continuously provide samples to the DAC module. The TX (transmitting) pin and RX (receiving) pin of the UART is connected to the RX and TX pins of the Bluetooth module for serial communication

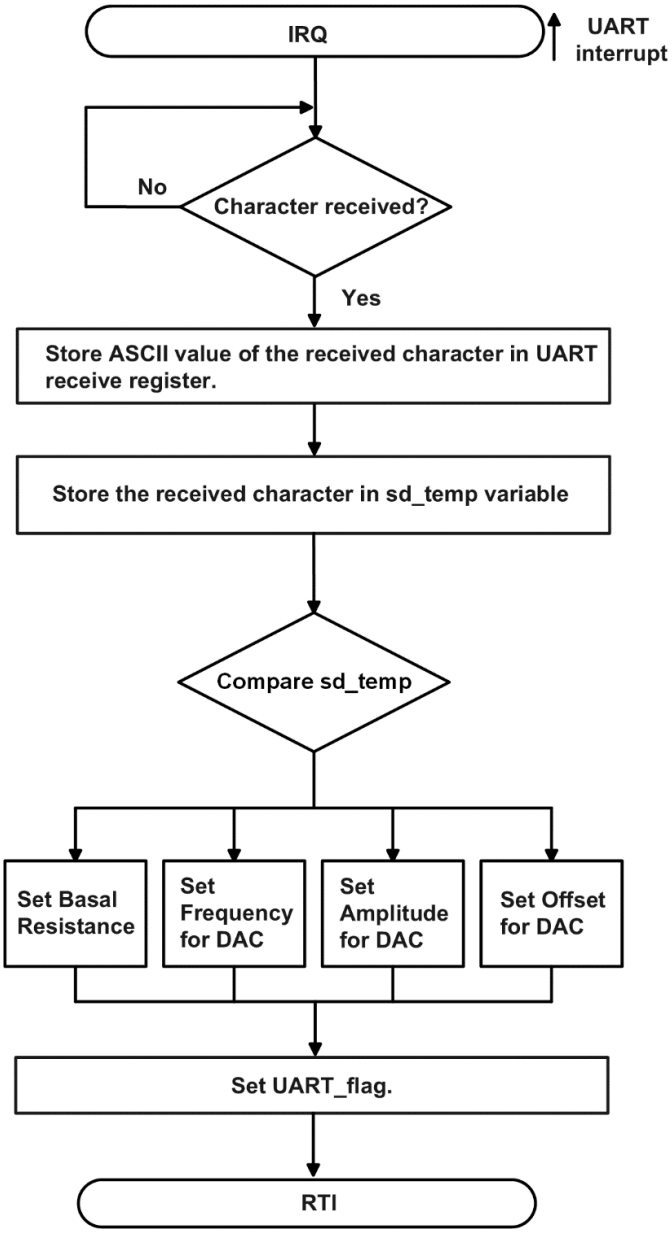


Fig. 4.11: Flow chart of U1RXInterrupt ISR

between them. ASCII commands sent wirelessly using PC based GUI are received by the Bluetooth, and are transmitted to the UART module of the microcontroller. The UART module generates the interrupt whenever it receives command and invokes the 'U1RXInterrupt' ISR. The ISR 'U1RXInterrupt' is written to provide select line values of analog MUX through digital IO pins of microcontroller to set the basal resistance based on the ASCII command received. It is also written to set the amplitude, frequency, offset, and shape of the waveform corresponding to the ASCII commands received.

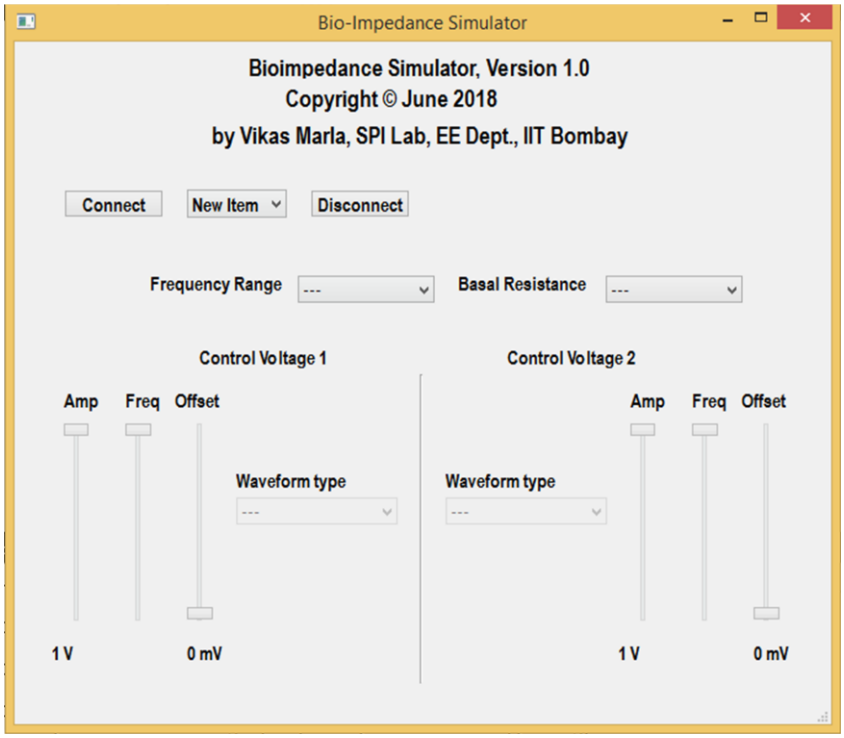
Fig. 4.10 shows the flowchart of the main function. It sets the system clock using its internal default FRC (fast RC) oscillator source, and whose frequency f_{clk} is programmed to be at 37 MHz. It initializes the UART and DAC module, and configures the IO ports using TRIS

bits. An infinite loop continuously sends samples to the DAC buffer to convert into analog output waveform. The DAC buffer is checked each time if it is empty or full, and generates an interrupt whenever it is empty. The variable '*i*' is the index of the samples which increments with value stored in variable 'count'. Thus, by changing the value of the variable 'count', the increment steps of samples could be varied. This operation will cause the intermediate samples to be dropped (decimation operation) and thus the frequency of the converted analog waveform can be changed. The samples are sent continuously to DAC buffer with increment of 'count' upto total number of samples *N*, after which *i* is initialized to zero and the increment is started again.

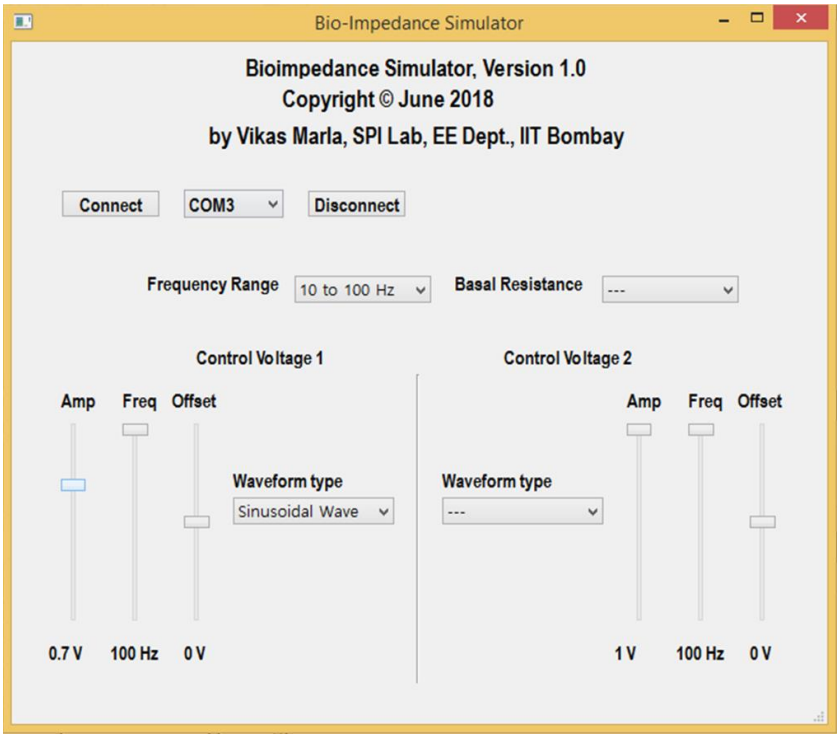
Fig. 4.11 shows the flowchart of 'U1RXInterrupt' ISR. When the UART receives an ASCII character it generates the interrupt 'U1RXInterrupt', and stores the character in the UART receiver register. At the interrupt, when the ISR is called, it is programmed to store the contents of the UART receiver register in a local variable 'sd_temp'. The variable 'sd_temp' is compared with different conditions in controller program, and correspondingly operations are performed. The operations performed could be setting the basal resistance, and setting the amplitude, frequency, offset, and shape of the output waveform. The above operations are performed in real-time, as the commands are sent from the PC based GUI. When the command is sent for setting the basal resistance, the output waveform of the DAC is not affected. However, when the command is to change the frequency by changing the sampling frequency f_s, or to change the shape of the waveform, the DAC operation is halted temporarily and reinitialized. However, to change the amplitude, offset, or the frequency by decimation, the DAC operation does not halt, and change occurs in real time.

4.8 PC-based GUI for Real-Time Parameter Setting

A PC-based GUI named 'bio_sim' has been developed in QT framework for setting of simulation parameters such as basal resistance, and frequency range, waveshape, offset, and amplitude of the control waveforms of the bioimpedance simulator circuit. The GUI program communicates with the Bluetooth module interfaced with microcontroller in the simulator circuit over a serial COM port of the PC. Bluetooth module of simulator needs to be paired with Bluetooth of the PC before any connection. The program is initiated by running an executable file, and GUI is appeared on the screen, and a screen shot of initial appearance of GUI is shown in Fig. 4.12 (a). After pairing, a COM port of the PC is provided to the paired Bluetooth module, which is identified by Bluetooth device setting option. The GUI has a drop-drown list of available COM ports, among which the assigned one needs to be chosen. Serial communication is established over the assigned COM port and serial data transfer takes place at a rate of 115200 kbps. After choosing the appropriate COM port, by clicking on the



(a)



(b)

Fig. 4.12: PC based GUI program "bio_sim": (a) Screen shot of initial appearance of GUI, (b) Screen shot of GUI with parameter setting

‘Connect’ button, a connection is established between the simulator and PC, and the ‘Disconnect’ button is used to disconnect the connection. Four dropdown list with labels ‘Basal Resistance’, ‘Frequency Range’, and Waveform type (two labels) are used for selecting the parameters of basal resistance, frequency range, and shape of the waveforms respectively. Six slider controls (three for each DAC channel) with labels ‘Amp’, ‘Freq’, and ‘offset’ for setting the parameters of waveforms such as amplitude, frequency, and offset respectively. Fig. 4.12 (b) shows a screen shot of GUI with some selected parameters as described above. Each time a value is changed in drop down menu, or in slider controls, an ASCII character is sent from PC over the Bluetooth to simulator. The received ASCII character is sent to the microcontroller through the UART module, with an interrupt generated. The program of the microcontroller identifies the ASCII character and perform the corresponding operations of parameters of simulator.

Chapter 5

TEST RESULTS

5.1 Introduction

The bioimpedance simulator constitutes of two major components i.e. resistance variation circuit (VCR) and basal resistance. The DC response and AC response of the VCR circuit was tested by providing control waveforms with the change in its frequency, amplitude, offset, and shape of waveform. The testing of power supply was also carried out.

5.2 Validation of VCR Circuit

To test and validate the VCR circuit, the circuit shown in Fig. 3.4 was breadboarded and tested. Two ICs ALD1106 (Analog Linear devices) [39] were used as MOSFETs M1 and M2. The op amp ICs TL084 (Texas Instruments) [43] were used as adders, buffers, and to provide control voltage v_A. The VCR circuit was tested using an external dc voltage source as in Fig. 5.1 and using an external ac source as in Fig. 5.5. By setting v_{C2} = – 1 V, v_{C3} = 0 V, and v_{C1} as a control input to the VCR circuit by varying its control parameters i.e. amplitude, waveform, frequency, and offset. As given in (3.38), the resistance R_{XY} across X and Y terminals with above voltages set and R_1 = 1 kΩ, R_{XY} is given as

$$R_{XY} = (v_{C1} / (-v_{C2}))R_1 \tag{5.1}$$

The circuit shown in Fig. 5.1 is connected to test the DC response of the VCR circuit. A DC voltage source V_{S1} = 5 V with series resistance R_S = 10 kΩ, is connected across the X and Y terminals. The voltage across X and Y terminals v_{XY} is given as

$$v_{XY} = V_{S1}\frac{R_{XY}}{R_{XY} + R_S} \tag{5.2}$$

With $R_S >> R_{XY}$, v_{XY} is given as

$$v_{XY} = (R_{XY} / R_S)V_{S1} \tag{5.3}$$

From (5.1) and (5.3), v_{XY} is given as

$$v_{XY} = (v_{C1} / (-v_{C2}))(R_1 / R_S)V_{S1} \tag{5.4}$$

which is given as

$$v_{XY} = 0.5v_{C1}$$

The DC response of the VCR circuit is observed using oscilloscope, and the screen shot image of the waveforms are shown in Figures 5.2, 5.3, and 5.4. The three waveforms shown

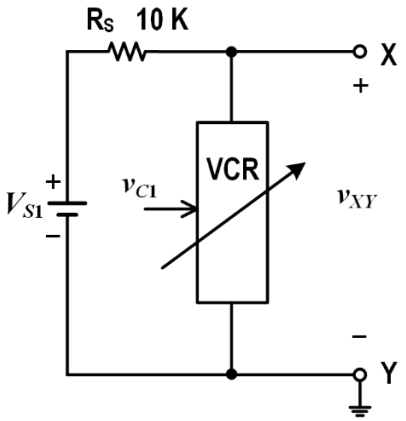


Fig. 5.1 Circuit for testing the VCR response using external DC source V_{S1} = 5 V and source

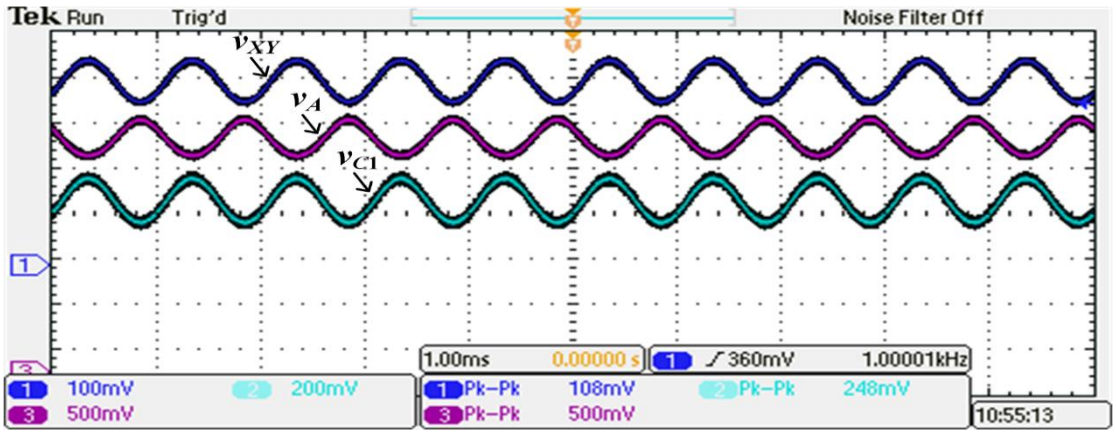


Fig. 5.2 Waveform of voltage v_{XY} across X and Y terminal, with v_{C1} = 200 mV (p-p) applied as sine wave, and with external DC source V_{S1} = 5 V

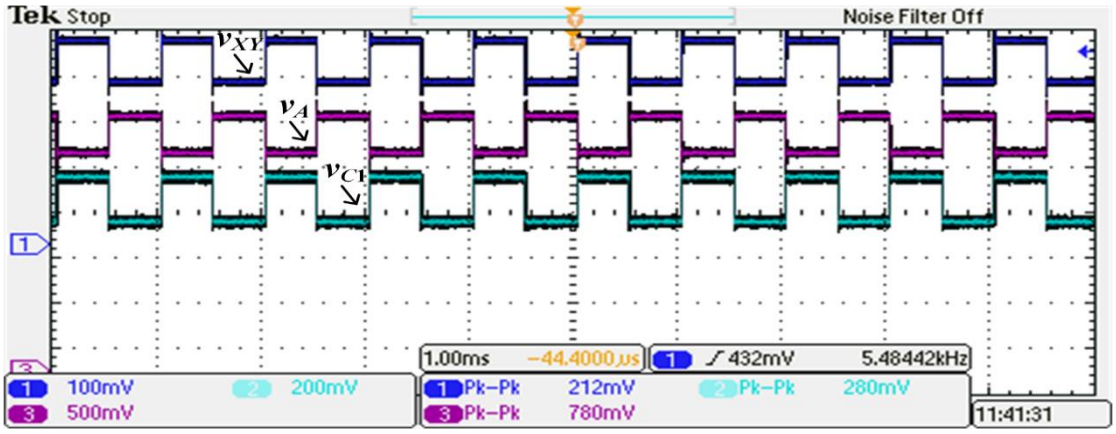


Fig. 5.3 Waveform of voltage v_{XY} across X and Y terminal, with v_{C1} = 200 mV (p-p) applied as square wave, and with external DC source V_{S1} = 5 V

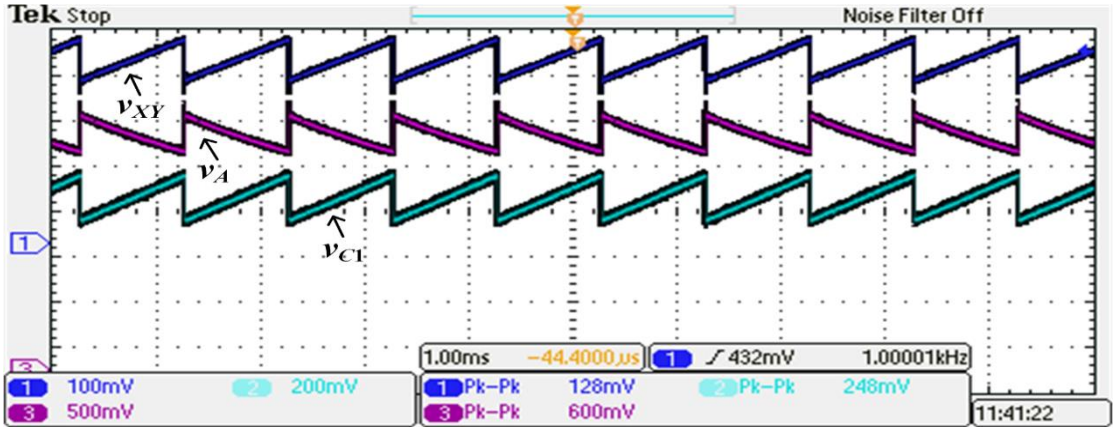


Fig. 5.4 Waveform of voltage v_{XY} across X and Y terminal, with v_{C1} = 200 mV (p-to-p) applied as triangular wave, and with external DC source V_{S1} = 5 V

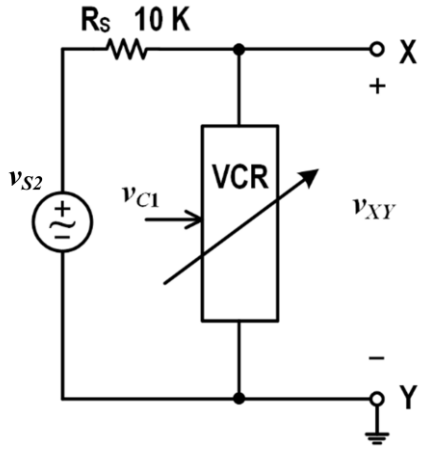


Fig. 5.5 Circuit for testing the VCR response using external sinusoidal source v_{S2} = 1 V (peak to peak) and source resistance R_S = 10 kΩ

simultaneously are the external control input v_{C1}, output of opamp A1 v_A as in Fig. 3.4, and the voltage across X and Y terminals v_{XY}. The waveforms shown in Fig. 5.2 is due to v_{C1} applied as sine wave, Fig. 5.3 is due to v_{C1} applied as square wave, and Fig. 5.4 is due to v_{C1} applied as triangular wave. As shown in Figures 5.2, 5.3, and 5.4, the shape of the output waveform v_{XY} is following the shape of the control input waveform v_{C1}. For the p-p amplitude of v_{C1} applied as 200 mV with DC offset of 800 mV of frequency of 1 kHz, the p-p amplitude of v_{XY} is obtained as 100 mV, which is in accordance with (5.4). It can also be noted that the waveform of v_A is inverted with respect to the waveforms of, which proves that v_A is inversely proportional to v_{C1}, in accordance with (3.32).

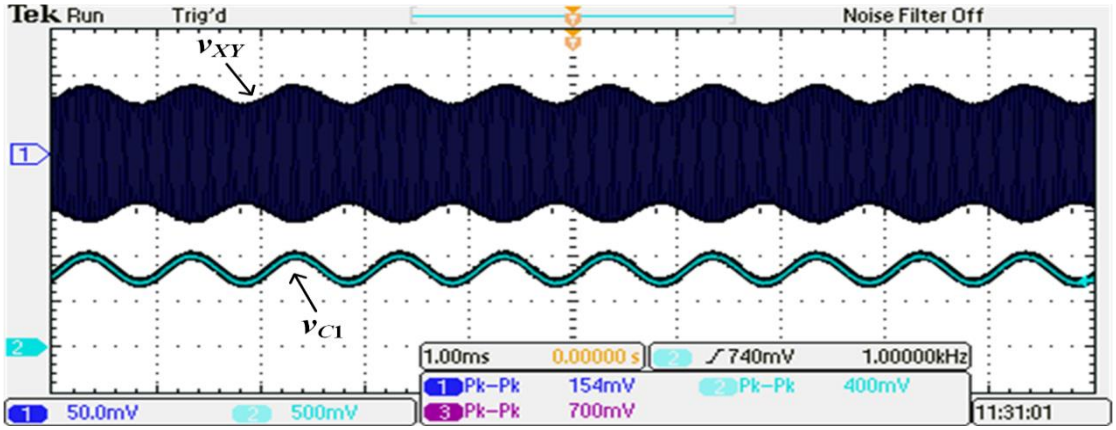


Fig. 5.6 Waveform of voltage v_{XY} across X and Y terminal, with v_{C1} = 400 mV (p-p) applied as sine wave, and with external sinusoidal source v_{S2} = 1 V (p-p)

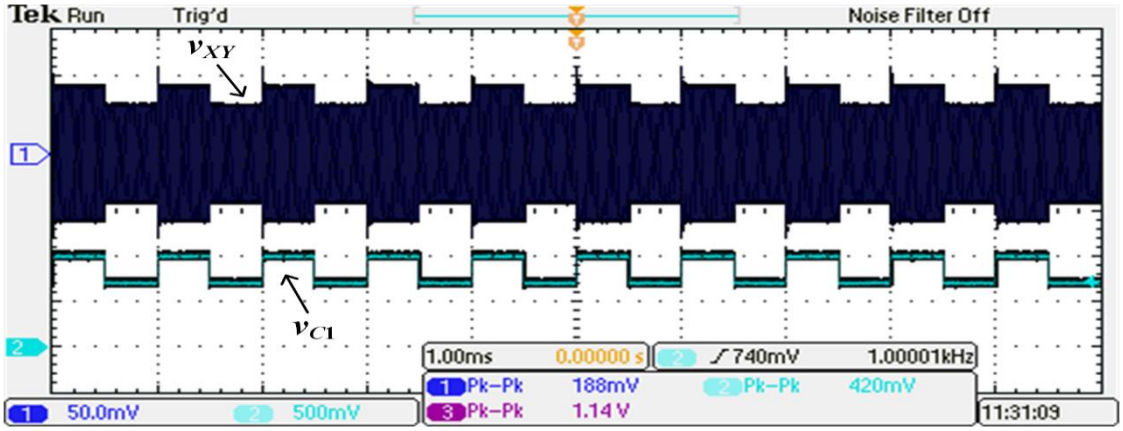


Fig. 5.7 Waveform of voltage v_{XY} across X and Y terminal, with v_{C1} = 400 mV (p-p) applied as square wave, and with external sinusoidal source v_{S2} = 1 V (p-p)

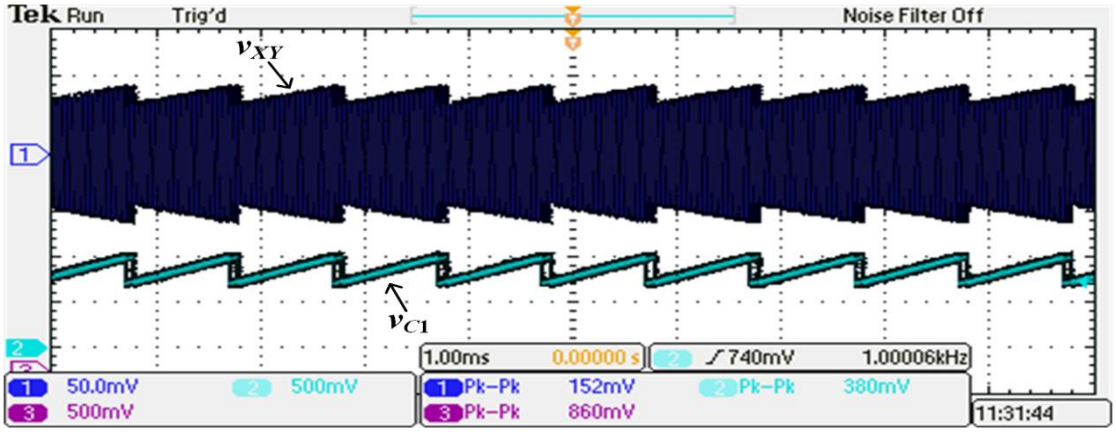


Fig. 5.8 Waveform of voltage v_{XY} across X and Y terminal, with v_{C1} = 400 mV (p-p) applied as triangular wave, and with external sinusoidal source v_{S2} = 1 V (p-p)

The circuit shown in Fig. 5.5 is connected to test the AC response of the VCR circuit. An AC voltage source v_{S2} as sinusoidal source of 1 V (p-p) and frequency of 20 kHz, with a series resistance R_S of 10 kΩ, is connected across the X and Y terminals. From (5.4), the voltage across X and Y terminals v_{XY} is given as

$$v_{XY} = 0.1 v_{C1} v_{S2}.$$

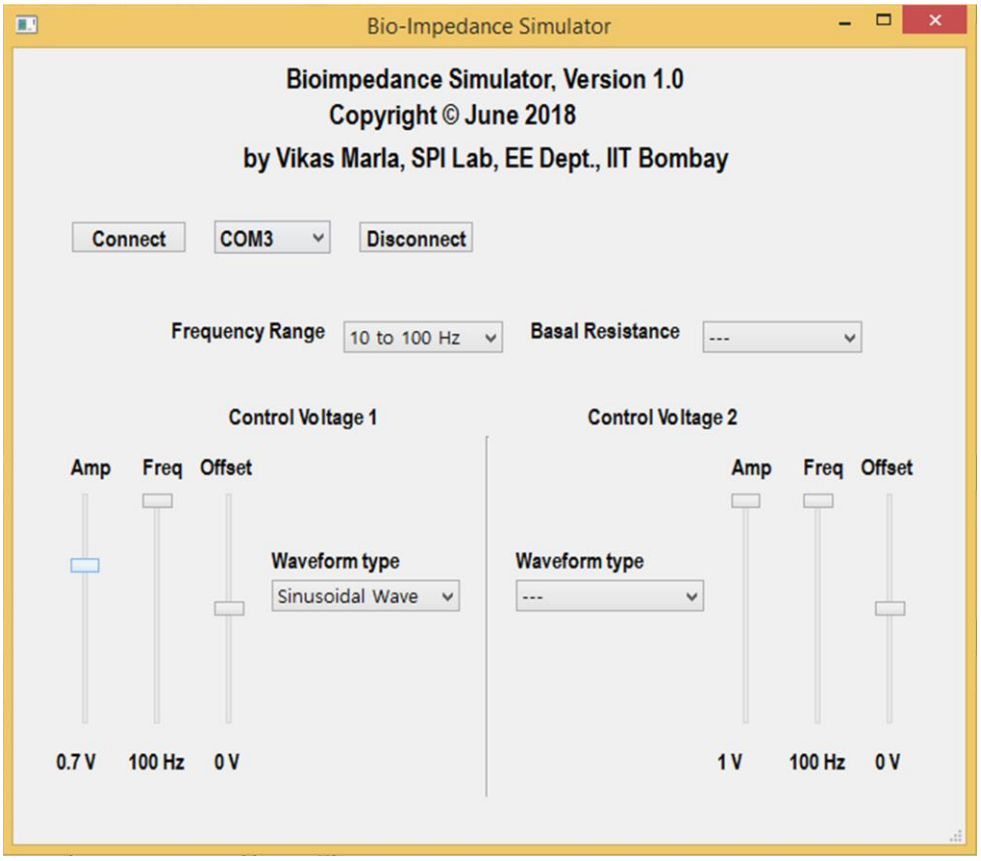
Thus, the voltage waveform v_{XY} obtained is the amplitude modulation of v_{S2} by v_{C1}. The waveforms are observed using oscilloscope, and the screen shots images are shown in Figures 5.6, 5.7, and 5.8, for v_{C1} as a sine, square and triangular wave respectively. The two waveforms shown simultaneously are the external control input v_{C1}, and the voltage across X and Y terminals. As shown in Figures 5.6, 5.7, and 5.8, the output waveform v_{XY} is the amplitude modulation of v_{S2} by v_{C1}. With the p-p amplitude of v_{C1} applied as 400 mV with DC offset of 800 mV, the p-p amplitude of v_{XY} is obtained as 150 mV.

5.3 Validation of the Power Supply circuit

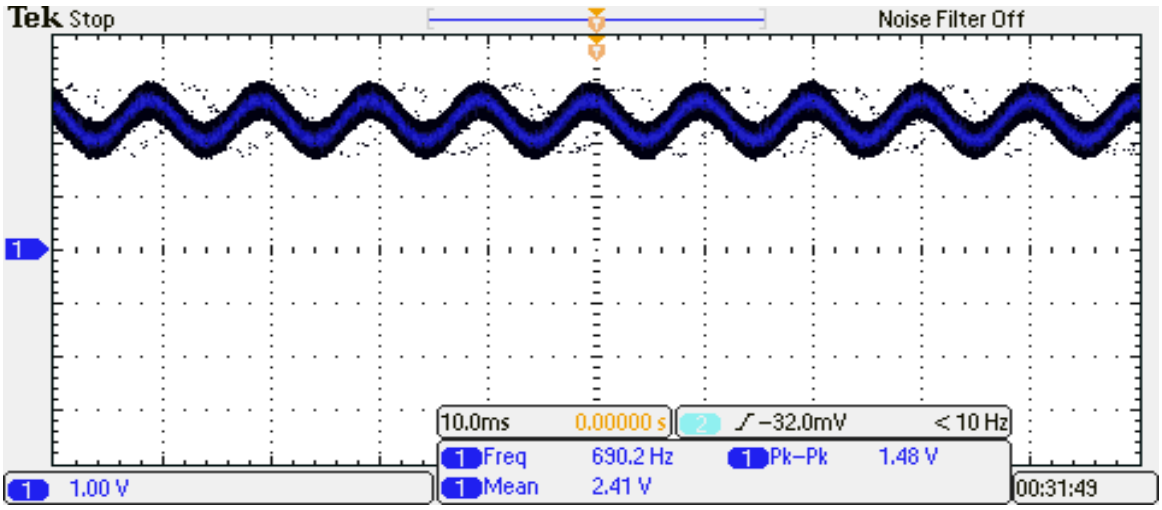
The power supply circuit shown in Fig. 4.9 is designed to provide two 3.3 V and 7.5 V supplies. To test the power supply circuit, a 5 V DC source V_P is applied as input, and output voltages of various ICs as shown in Fig. 4.9 is observed on both multimeter and oscilloscope. The output voltages DV3V3 and AV3V3 of two Linear regulator ICs TPS73433 U6 and U7 were tested, and the measured value was obtained to be DC voltage of 3.298 V for DV3V3, and 3.294 for AV3V3. With the input voltage V_P = 5 V given as input to a charge pump-based voltage doubler IC (MAX 1681) U8, the measured value of output voltage V_{PD} was obtained to be 10.012 V, and the measured value of output voltage AV7V5 was 7.485 V. However, significant ripples were observed to be superimposed on all the above output voltages. For DV3V3 and AV3V3, the p-p ripples were 130 mV. For V_{PD}, it was 242 mV. For AV7V5, it is 198 mV. The above ripple is mainly due to the switching operation of the charge pump IC, since the frequency of the spikes in the ripple waveforms is equal to the switching frequency of the charge pump IC. Thus, the power supply circuit has to be redesigned by either changing the PCB design, or output capacitors, or the IC itself.

5.4 Validation of op amp outputs

Multiple op amps (IC ADA4807) were used in the design of bioimpedance simulator. As mentioned in Chapter 4, the op amps were used in VCR as adders, buffers and to obtain control voltage v_A, and in controller circuit as a differential amplifier to obtain v_{C1} and v_{C2}. The output voltages of all the voltages were tested to validate them. As shown in Fig. 4.4, the voltage buffer U2D used to obtain the substrate bias V_{BB} was tested, and DC voltage value

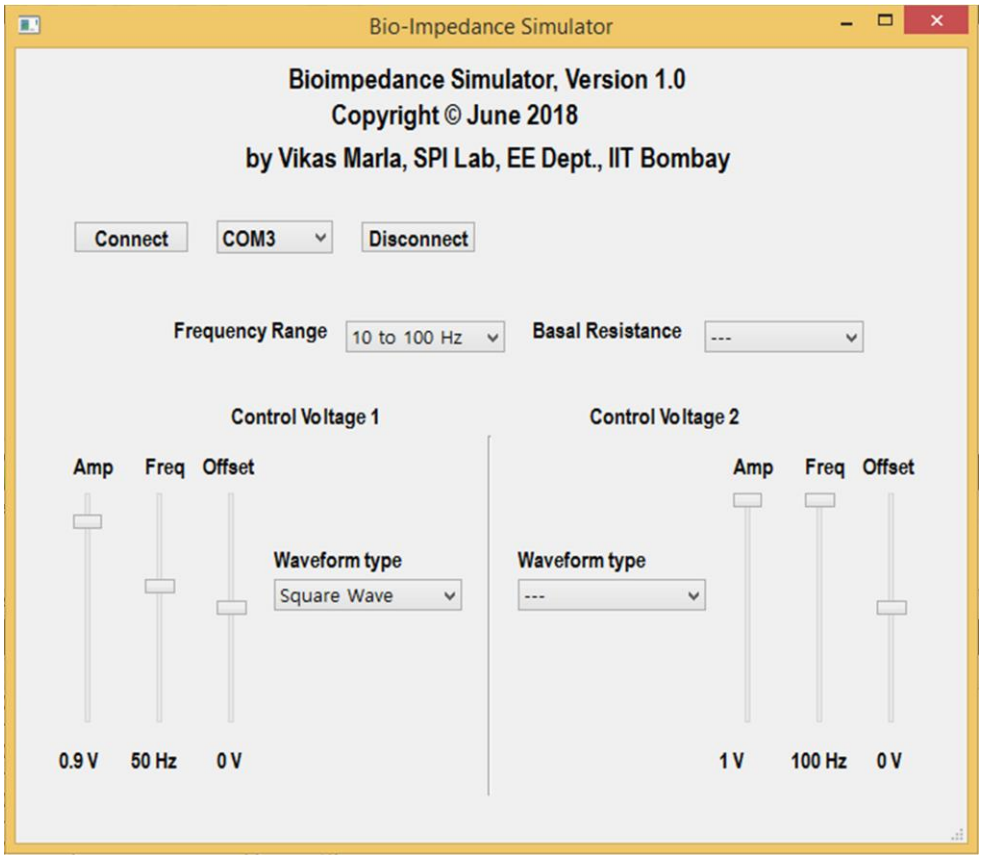


(a)

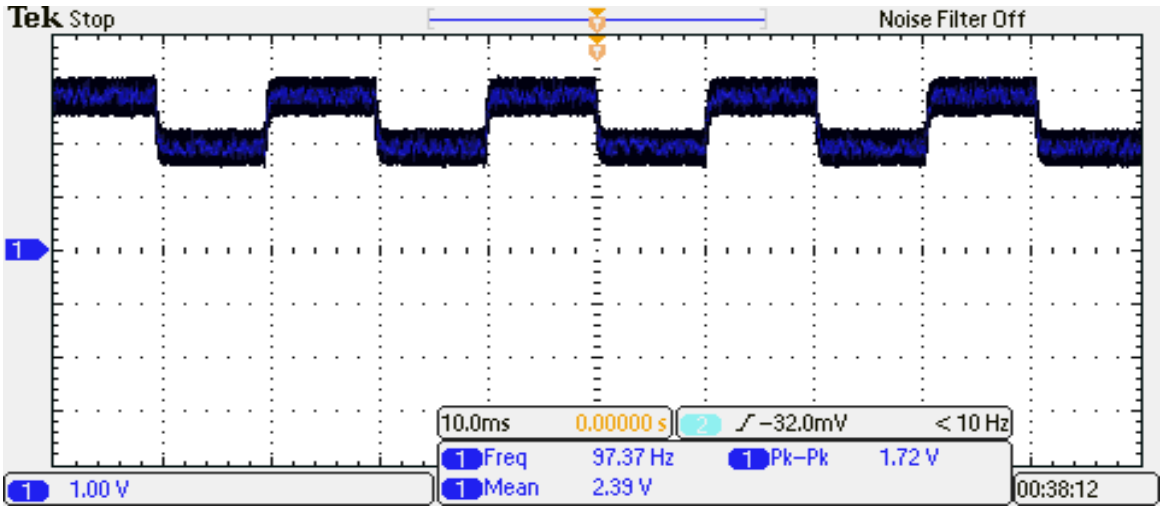


(b)

Fig. 5.9 Control voltage signal v_{C1} with its parameters (a) Screen shot of PC-based GUI setting parameters for v_{C1}, (b) Generated control waveform v_{C1} for the VCR circuit with sinusoidal signal of p-p voltage of 1.4 V, frequency 100 Hz, and offset 0 V

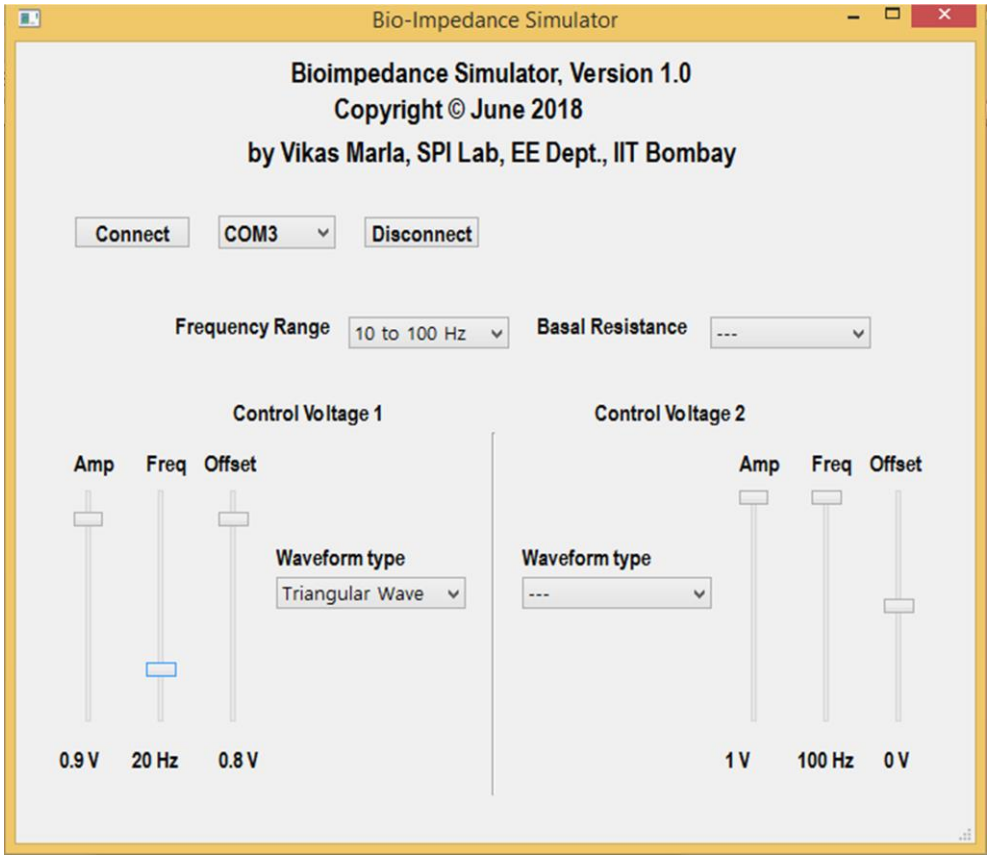


(a)

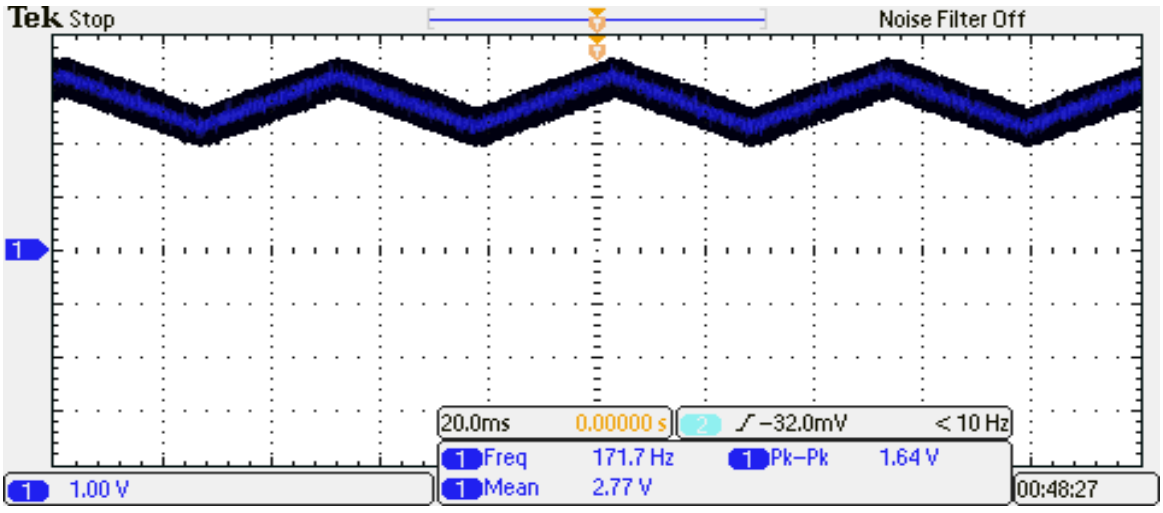


(b)

Fig. 5.10 Control voltage signal v_{C1} with its parameters (a) Screen shot of PC-based GUI setting parameters for v_{C1}, (b) Generated control waveform v_{C1} for the VCR circuit with square waveform of p-p voltage of 1.8 V, frequency 50 Hz, and offset 0 V.



(a)



(b)

Fig. 5.11 Control voltage signal v_{C1} with its parameters (a) Screen shot of PC-based GUI setting parameters for v_{C1}, (b) Generated control waveform v_{C1} for the VCR circuit with triangular waveform of p-p voltage of 1.8 V, frequency 20 Hz, and offset 0.8 V.

obtained was 0.645 V which is in accordance with the design. Similarly, the voltage buffer U2A as shown in Fig. 4.3 used to obtain reference bias A_{VREF} for the VCR circuit was tested. The DC voltage value obtained was 1.676 V which is in accordance with the design. However, it was noticed that the oscillations of high frequency of 33 MHz was superimposed on A_{VREF}. In the PCB design layout, the terminal A_{VREF} was designed to be a plane which formed a capacitive load for the voltage buffer U2A output. And it is mentioned in the datasheet of IC ADA4807 [39], that the op amp connected as voltage follower with a capacitive load at its output will lead oscillations due to resonance. Since, A_{VREF} acts as reference potential for the entire VCR circuit, these oscillations were further amplified at the output of other op amps. Thus, the op amp part of the circuit needs to be redesigned by either changing the PCB layout design, or replacing the IC component itself which can be used as voltage follower without any oscillations formed.

5.5 Validation of Controller Circuit

The controller circuit shown in Fig. 4.6. has the microcontroller DSPIC33FJ128GP802 interfaced with the RN42 Bluetooth module. The connection between PC based GUI and the Bluetooth module is tested and validated by observing the status of LEDs. The PC based GUI is used to set the basal resistance, and to provide the two control waveforms (v_{C1} and v_{C2}). Each parameter received by the Bluetooth of simulator from GUI is sent to the microcontroller, which sends the parameter to the VCR circuit. Figures 5.9 to 5.11 shows the control waveforms v_{C1} whose parameters are set by the PC based GUI with its screen shots shown. It may be noted that all the waveforms in Figures 5.9 to 5.11 have noise and ripples superimposed on them, which is due to the problems discussed in the previous sections of this chapter.

Chapter 6

SUMMARY AND CONCLUSION

The project objective was to develop a bioimpedance simulator for testing and calibration of the impedance measuring instruments. Simulator is required to simulate the continuous time varying impedance and basal impedance. For this purpose, a simulator has been designed comprising of four blocks: resistance variation circuit includes time-varying impedance and fixed value basal impedance, controller circuit to generate the control signals to the resistance variation circuit, Bluetooth module wirelessly receive the parameters of the resistance variation sent from PC, and power circuit to provide power supply to the simulator.

After studying earlier VCR circuits, an analysis of several VCR circuits has been carried out. By simulation and practical testing, it has been found that a matched-pair MOSFET with independent substrate terminals with S-D bootstrapping (feedback technique), and with self-tracking can be used to realize a floating VCR with linear range of operation extended and make its resistance independent of device parameters.

The time-varying resistance realized using MOSFET based voltage controlled resistor (VCR) with n-channel matched pair of MOSFETs with independent substrate terminals. The controller circuit is devised using a microcontroller with on-chip DAC for obtaining the control waveforms to VCR to obtain time-varying resistance, digital outputs to select the internal switches of analog multiplexer for setting the basal resistance, and UART to receive the control parameters from the Bluetooth which in turn receives from PC based GUI or any other computing device wirelessly. The power supply circuit has been designed using charge pump based voltage doublers, and linear regulators to provide analog and digital 3.3 V supply, and 7.5 V supply for op amps. However, after testing the power supply circuit, a significant amount of ripple was observed requiring power supply circuit to be redesigned. The op amps were used in the VCR circuit as adders and voltage followers to realize S-D bootstrapping, connected in negative feedback to realize self-tracking, used as a differential amplifier to provide control waveforms to VCR, and used as buffers to provide substrate bias and reference potential for the circuit. However, after testing the VCR circuit, oscillations were observed at output of op amps, along with the ripples due to power supply circuit.

While all the blocks for the bioimpedance simulator and associated software have been developed and validated, the source of the noise and oscillation need to be located, and the board need to be redesigned and tested.

APPENDIX A

SCHEMATIC OF BIOIMPEDANCE SIMULATOR

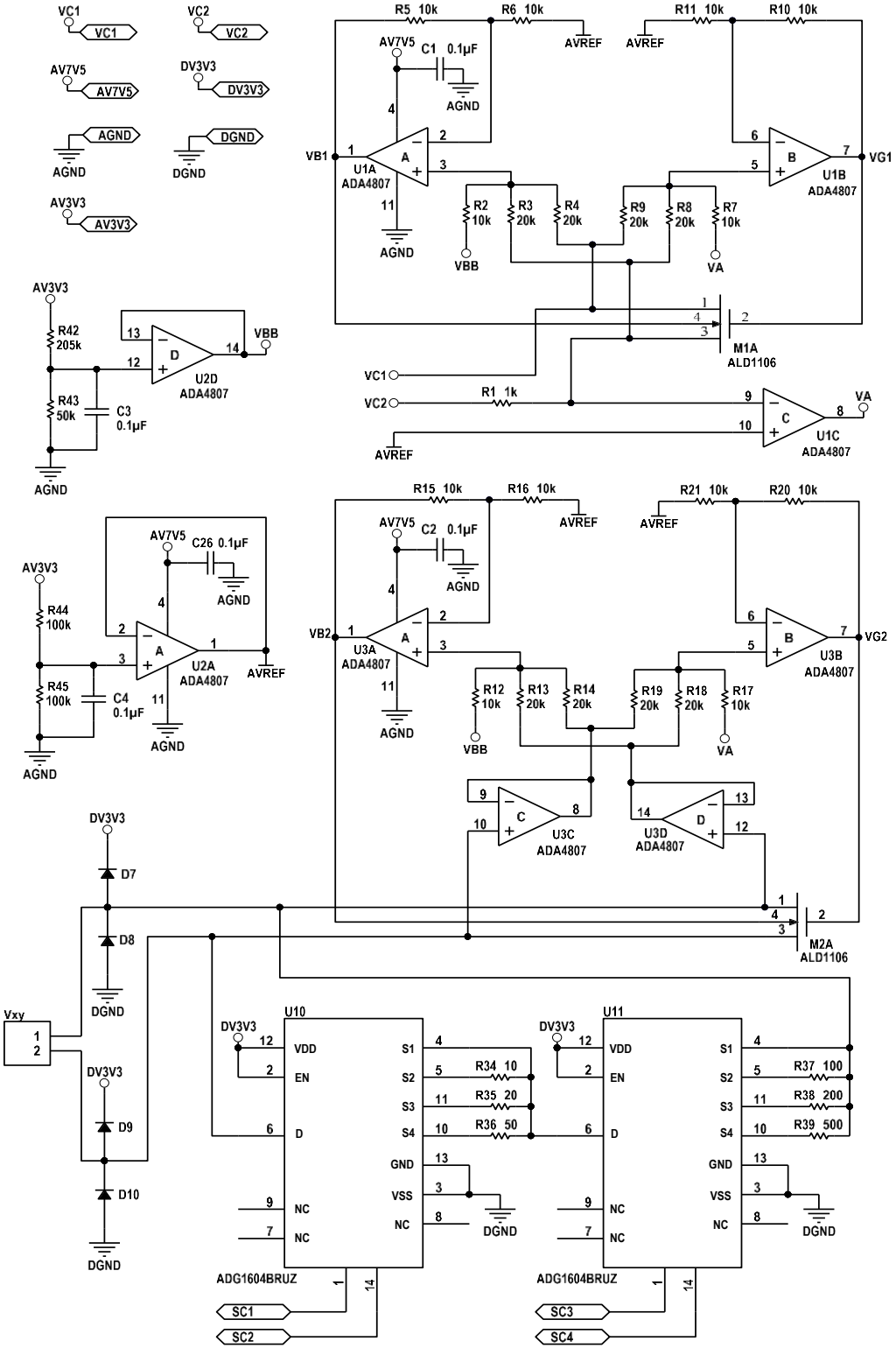


Fig. A.1: Schematic sheet-1 : The resistance variation circuit

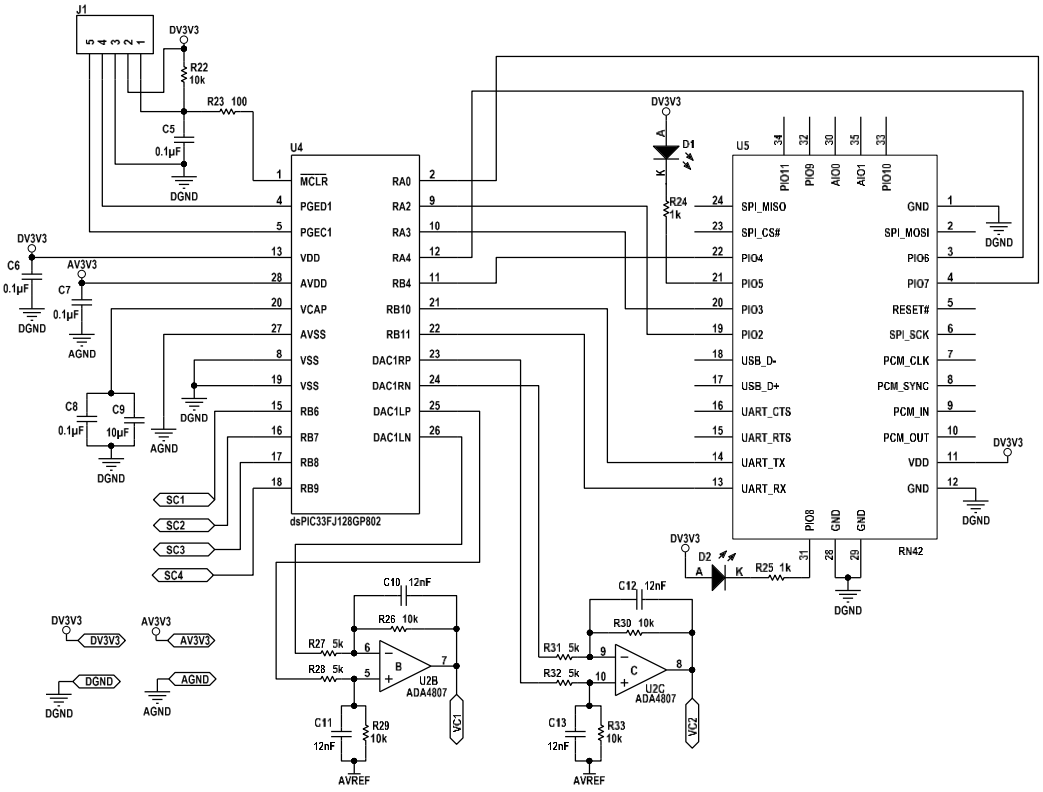


Fig. A.2: Schematic sheet-2 : The controller circuit with Bluetooth module

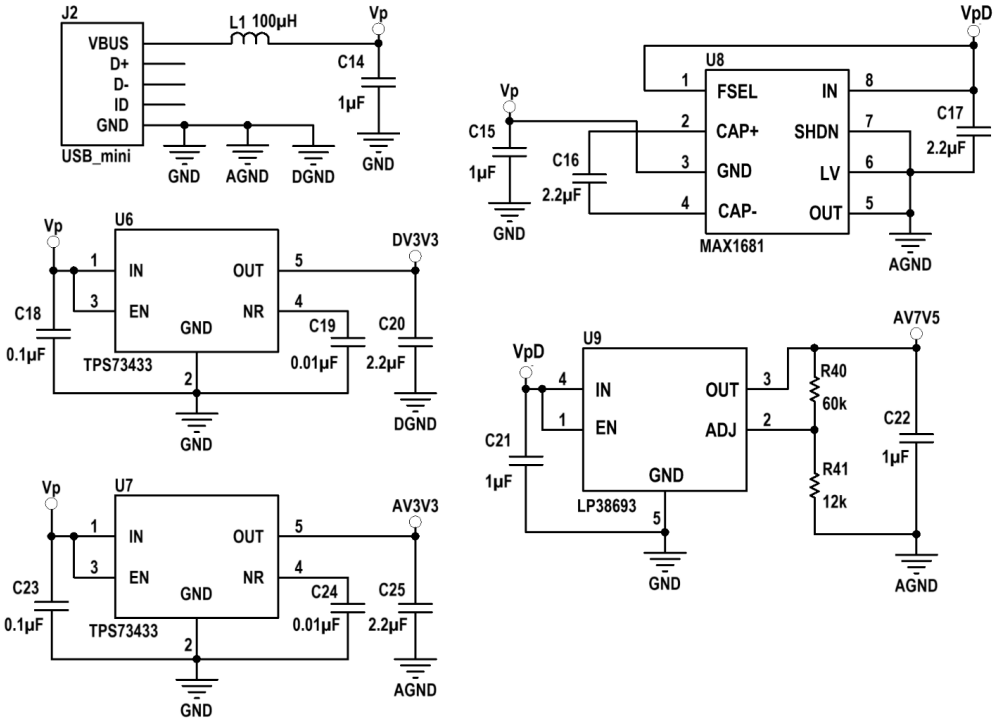


Fig. A.3: Schematic sheet-3 : The power circuit.

APPENDIX B

PCB LAYOUT

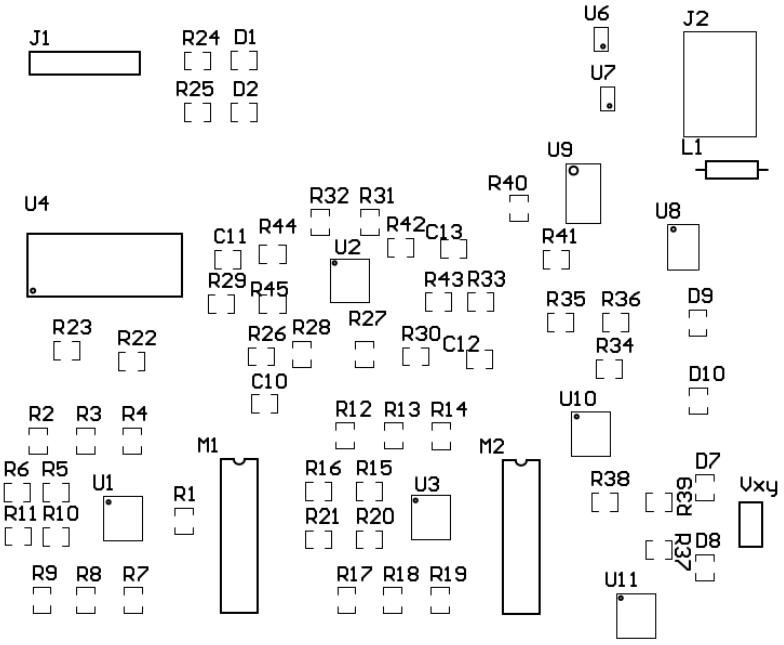


Fig. B.1: PCB layout-1 : Top overlay of the design.

Fig. B.2: PCB layout-2: Bottom overlay of the design.

APPENDIX C
COMPONENT LIST FOR BIOIMPEDANCE SIMULATOR

Table C.1: Component list for the bioimpedance simulator

Component designator	Component description	Part Number / Value	Quantity
C19, C24	Capacitor, ceramic, chip	0.01 μF	2
C10, C11, C12, C13	Capacitor, ceramic, chip	12 nF	4
C1, C2, C3, C4, C5, C6, C7, C8, C18, C23, C26	Capacitor, ceramic, chip	0.1 μF	6
C14, C15, C21, C22	Capacitor, ceramic, chip	1 μF	5
C9	Capacitor, ceramic, chip	10 μF	1
C16, C17, C20, C25	Capacitor, ceramic, chip	2.2 μF	4
R1, R24, R25	Resistor	1 kΩ	3
R41	Resistor	2 kΩ	1
R3, R4, R8, R9, R13, R14, R18, R19, R26, R29, R30, R33	Resistor	20 kΩ	12
R2, R5, R6, R7, R10, R11, R12, R15, R16, R17, R20, R21, R22, R27, R28, R31, R32, R41	Resistor	10 kΩ	18
R43	Resistor	50 kΩ	1
R44, R45	Resistor	100 kΩ	2
R42	Resistor	200 kΩ	1

R34	Resistor	10 Ω	1
R35	Resistor	20 Ω	1
R36	Resistor	50 Ω	1
R23, R37	Resistor	100 Ω	2
R38	Resistor	200 Ω	1
R39	Resistor	500 Ω	1
U9	Adjustable voltage regulator	LP38639	1
U4	IC, Microcontroller	DSPIC33FJ128GP80	1
U5	Bluetooth Module	RN42	1
M1, M2	IC, MOSFET	ALD1106	1
D1, D2	LED	LED	2
D7, D8, D9, D10	Diode	Diode	4
J2	USBMINI	USBMINI	1
J1	Connector, 5 Pin	DEBUG	1
XY	Connector, 2 Pin	XY Terminal	1
U1, U2, U3	Op amp	ADA4807	3
U6, U7	3.3 V fixed regulator	TPS73433	2
U8	Charge pump voltage doubler	MAX1681	2
U9	Adjustable linear regulator	LP38693	1
U10, U11	4:1 analog multiplexer	ADG1604BRUZ	2

REFERENCES

[1] S. Grimnes and O. G. Martinsen, *Bioimpedance and Bioelectricity Basics*, 2nd ed., Oxford, UK, Elsevier, 2008.

[2] H. P. Schwan and C. F. Kay, "Specific resistance of body tissues," *Circulation Research*, vol. 4 (6), pp. 664−670, 1956.

[3] R. P. Patterson, "Fundamentals of impedance cardiography*," IEEE Eng. Med. Biol. Mag.*, vol. 8 (1), pp. 35–38, 1989.

[4] Z. Lababidi, D. A. Ehmke, R. E. Durnin, P. E. Leaverton, and R. M. Lauer, "The first derivative thoracic impedance cardiogram," *Circulation Research*, vol. 41 (4), pp. 651–658, 1970.

[5] L. E. Baker, "Applications of impedance technique to the respiratory system," *IEEE Eng. Med. Biol. Mag.*, vol. 8 (1), pp. 50–52, 1989.

[6] H. H. Woltjer, H. J. Bogaard, and P. M. J. M. de Vries, "The technique of impedance cardiography," *Euro. Heart J.*, vol. 18 (9), pp. 1396–1403, 1997.

[7] D. P. Bernstein and H. J. M. Lemmens. "Stroke volume equation for impedance cardiography." *Med. Biol. Eng. Comput.*, vol. 43 (4), pp. 443-450, 2005.

[8] Kubicek et al., "Development and evaluation of an impedance cardiac output system." *Aerospace Med*., vol. 37 (12), pp. 1208-12, 1966.

[9] B. Sramek, "Noninvasive continuous cardiac output monitor." U.S. Patent 4450527, May 22, 1984.

[10] L. E. Baker, "Applications of impedance technique to the respiratory system," *IEEE Eng. Med. Biol. Mag.*, vol. 8 (1), pp. 50–52, 1989.

[11] Medis, "NICCOMO – non-invasive continuous cardiac output monitor," Available online, medis.company/cms/uploads/PDF/niccomo.pdf, accessed: June 9, 2016.

[12] Philips, "Phillips ICG – impedance cardiography," Available online, incenter.medical.philips.com/doclib/enc/fetch/2000/4504/577242/577243/577247/582646/583147/PM_-_ICG_Brochure.pdf, accessed: June 9, 2016.

[13] M. Ulbrich et al., "A thorax simulator for complex dynamic bioimpedance measurements with textile electrodes," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9 (3), pp. 412–420, 2015.

[14] S. M. M. Naidu, U. R. Bagal, P. C. Pandey, S. Hardas, and N. D. Khambete, "Detection of characterisitc points of impedance cardiogram and validation using Doppler echocardiography," in *Proc. IEEE INDICON*, Pune, India, 2014.

[15] J. Millman and C. C. Halkias, *Integrated Electronics*, 2nd ed., New York: McGraw Hill, pp. 322−327, 2010.

[16] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 5th ed., New York: Oxford University Press, pp 248–259, 2004.

[17] M. Ismail and T. Fiez, *Analog VLSI: Signal and Information Processing*, New York: McGraw-Hill, 1994, pp. 13−22.

[18] Y. Tsividis, *Operation and Modelling of the MOS Transistor*, 2nd ed., Singapore:WCB/McGraw Hill, 1999.

[19] R. Senani, "Realisation of linear voltage-controlled resistance in floating form," *Electronics Letters*, vol. 30 (23), pp. 1909−1911, Nov. 10, 1994.

[20] T. L. Clarke, "FET pair and op amp linearize voltage controlled resistor," *Electronics Letters*, pp. 111, Apr. 28, 1977.

[21] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Trans. Circuits Syst.*, vol. 48 (7), pp. 876−884, Jul. 2001.

[22] R. Senani and D. R. Bhaskar, "A simple configuration for realizing voltage-controlled impedances', *IEEE Trans. Circuits Syst.*, vol 39 (1), pp. 52-59, Jan. 1992.

[23] G. Moon, M. E. Zaghloul, and R. W. Newcomb, "An enhancement-mode MOS voltage-controlled linear resistor with large dynamic range," *IEEE Trans. Circuits Syst.*, vol. 37 (10), pp. 1284−1288, Oct. 1990.

[24] J. Fort, "MOS resistor with second or higher order compensation," U. S. Patent 8 067 975, Nov. 29, 2011.

[25] J. K. Greason, “Voltage-controlled resistance element with superior dynamic range,” U.S. Patent 5 264 785, Nov. 23, 1993.

[26] A. Bilotti, “Operation of a MOS transistor as a variable resistor,” *IEEE Proc. Letters*, pp. 1093−1094, Aug. 20, 1966.

[27] N. S. Manigandan, “Development of hardware for impedance cardiography,” M. Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2004

[28] N. K. S. Naidu, “Hardware for impedance cardiography,” M. Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2005.

[29] L. Venkatachalam, “Development of hardware for impedance cardiography,” M. Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2006.

[30] B. B. Patil, “Instrumentation for impedance cardiography,” M. Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2009.

[31] M. D. Desai, “Development of an impedance cardiograph,” M.Tech. dissertation, Biomedical Eng., IIT Bombay, Mumbai, India, 2012.

[32] R. Holani, “A bioimpedance simulator for impedance cardiography,” M.Tech. dissertation, Biomedical Engg., IIT Bombay, Mumbai, India, 2014.

[33] S. Debbarma, "A bioimpedance simulator," M.Tech. dissertation, Biomedical Engg., IIT Bombay, Mumbai, India, 2016.

[34] G. Bret, “Circuit with a voltage-controlled resistance,” US patent publication No. US 5300834A, Sep. 6, 1989.

[35] Analog Devices, “4:1 Multiplexer," Available online, www.analog.com/media/en/ technical-documentation/data-sheets/ADG1604.pdf, downloaded on Aug. 24, 2017.

[36] Maxim Integrated, “125mA, Frequency-selectable, switched-capacitor voltage converters,” Available online, datasheets.maximintegrated.com/en/ds/MAX1680-MAX1681.pdf, downloaded on Sep. 23, 2017.

[37] Texas Instruments, "500-mA Low-dropout CMOS linear regulators," Available online,

www.ti.com/lit/ds/symlink/lp38693-adj.pdf, downloaded on Sep. 2, 2017.

[38] Texas Instruments, "250mA, Low quiescent current, ultra-low Noise, high PSRR low-dropout linear regulator," Available online, www.ti.com/lit/ds/symlink/tps73433-q1.pdf, downloaded on Aug. 31, 2017.

[39] Analog Linear Devices, "Quad n-channel matched pair MOSFET array, "Available online, www. aldinc.com/pdf/ALD1116.pdf, downloaded on Jan. 17, 2017.

[40] Analog Devices, "1 mA, 180 MHz, rail-to-rail input/output amplifiers," Available online, www. analog.com/media/en/technical-documentation/data-sheets/ADA4807-1_4807-2_4807-4.pdf, downloaded on Aug. 30, 2017.

[41] Microchip, "High-performance, 16-bit digital signal controllers," Available online, ww1.microchip. com/downloads/en/DeviceDoc/70292E.pdf, downloaded on Aug. 12, 2017.

[42] Roving Networks, "RN42/RN42N Class 2 Bluetooth Module," Available online, ww1. microchip.com/downloads/en/DeviceDoc/rn-42-ds-v2.32r.pdf, downloaded on Aug. 14, 2017.

[43] Texas Instruments, “TL084 JFET-Input operational amplifier,” Available online, http://www.ti.com/lit/ds/symlink/tl082.pdf, downloaded on Jun. 26, 2018.

ACKNOWLEDGEMENT

I would like to express my gratitude towards my project guide Prof. P. C. Pandey for his invaluable time, guidance and support. I would also thank Mr. Nandakumar Pai for all the valuable time, suggestions and support he gave me for this project. I am also very thankful to Mr. Vidyadhar kamble for helping me in procuring various electronic components. I also thank to all my SPI labmates Natraj, Hirak, Nitya, Yogesh, Shibham, Saketh, Prachir, Omer, and Susmi for their constant support.