An Impedance Cardiograph Using Synchronous Demodulation and Integrated Baseline Correction

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by

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ABSTRACT

Impedance cardiography is a noninvasive technique for estimating the stroke volume and cardiac output by sensing the thoracic impedance, which has a basal impedance of 20−200 Ω with 0.1−2% time-varying component related to variation in the blood volume during the cardiac cycle. The instrumentation for impedance measurement generally comprises injection of a high-frequency low-amplitude current (20−100 kHz, < 5 mA) in the thorax region through a pair of electrodes, sensing the resulting voltage using another pair of electrodes, amplitude demodulation to extract the impedance signal, and separation of the time-varying component and its differentiation to get the impedance cardiogram (ICG). The project objective is to develop an impedance cardiograph using synchronous demodulation with integrated baseline correction to improve the demodulation sensitivity, noise rejection, and ripple rejection, and to reduce the circuit complexity for body-wearable applications.

The present design is realized using the impedance converter IC TI/AFE4300 having a DDS for sinusoidal excitation voltage with settable frequency, and an impedance measuring circuit using synchronous demodulation with in-phase and quadrature (I/Q) outputs; a microcontroller and additional circuit blocks consisting of balanced V/I converter, voltage sensing amplifier with improved CMRR, and a baseline correction arrangement. A V/I converter with balanced current output is used for stray-insensitive excitation.The voltage across the electrode pair is amplified by a sensing amplifier, with an instrumentation amplifier configuration along with a common-mode negative feedback for enhanced CMRR. The baseline correction is performed before the synchronous demodulation by subtracting a sinusoidal voltage obtained from the excitation source with digitally controlled amplitude to improve the resolution of impedance measurement. In order to allow independent control on the amplitude of the current excitation and the baseline correction signal, two digital potentiometer ICs are used. A microcontroller is used for setting all the measurement parameters, reading the measured impedance, and transferring the data wirelessly via Bluetooth to an external device like a PC for processing and visualization.

CONTENTS

LIST OF ABBREVIATIONS

Abbreviation	Explanation
ADC	analog to digital converter
AGND	analog ground
ASCII	american standard code for information interchange
CMRR	common-mode rejection ratio
CO	cardiac output
COM	communication
CS	chip select
DAC	digital-to-analog converter
DDS	direct digital synthesizer
DFT	discrete Fourier transform
DGND	digital ground
DR	digtial receiver
ECG	electrocardiogram
EDV	end-diastolic volume
EMG	electromyogram
ESV	end-systolic volume
FWR	full-wave rectifier
GND	ground
GUI	graphical user interface
I/Q	in-phase and quadrature
IC	integrated circuit
ICG	impedance cardiogram
INA	instrumentation amplifier
IO	input-output
ISR	interrupt service routine
LDO	low dropout
MDAC	multiplying digtial-to-analog converter
OTA	operational transconductance amplifier
PC	personal computer
PCB	printed circuit board
PGA	programmable gain amplifier
PLL	phase-locked loop
PTH	plating through hole
RLD	right-leg drive

SAR	successive approximation register
SCLK	serial clock
SDIN	serial data input
SDOUT	serial data output
SMD	surface-mount technology
SNR	signal-to-noise ratio
SPDT	single-pole double-throw
SPI	serial peripheral interface
STE	serial enable
SV	stroke volume
UART	universal asynchronous receiver and transmitter
USB	universal serial bus
V/I	voltage-to-curretnt converter

LIST OF SYMBOLS

Symbol	Explanation
A_c	common-mode gain
A_d	differential gain
AV3V3	analog supply of 3.3 V
AVREF	reference voltage in the VCR circuit
DV3V3	digital supply of 3.3 V
f_{clk}	input clock frequency of TI/AFE4300
F_{CY}	instruction clock cycle frequency
g_m	trans-conductance
I_{DC}	demodulated in phase voltage
i_L	load current
Q_{DC}	demodulated quadrature voltage
R_L	load resistance
T_{LVET}	left ventricular ejection time
V_{bc}	baseline correction signal
V_{DAC_OUT}	output voltage of the DAC
V_{DEMOD}	output of the baseline correction amplifier
Z_0	basal component of thoracic impedance
$z(t)$	time-varying component of thoracic impedance
α_2	resistance ratio of the digi pot 1
β_2	resistance ratio of the digi pot 2
ρ	resistivity

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Chapter 1

INTRODUCTION

1.1 Background

Bio-impedance is the electrical impedance of the biological materials like tissues, blood, muscles, body fluids, etc. [1]−[5]. Its measurement is helpful in the diagnosis of abnormalities in the human body by calculating certain physiological parameters. The blood has the highest conductivity among all the biological materials and variation in the amount of blood in the thorax during the cardiac cycle causes variation in the thoracic impedance. Impedance cardiography (ICG) is a noninvasive technique for sensing the variation of thoracic impedance during the cardiac cycle and estimating the stroke volume, cardiac output, and a few other cardiovascular indices, which may be useful in the diagnosis of cardiac disorders. The thoracic impedance consists of a basal value and a time-varying component, which is considered to be related to the blood volume in the thorax. Typically, the basal impedance of the thorax is around 20−200 Ω, and the time-varying component is 0.1−2% of the basal impedance. In impedance cardiography technique, a current of low amplitude (< 5 mA) and high frequency (20−100 kHz) is injected through a pair of electrodes into the thorax region and the resulting amplitude-modulated voltage is sensed using another pair of electrodes. The sensed voltage is demodulated to extract the impedance signal [1]. ICG serves as an alternative to other stroke volume measuring techniques like thermodilution, Fick's method, and Doppler echocardiography. Some of the commercially available ICG instruments are 'Niccomo' from Medis Non-invasive cardiac output monitor [9] and 'ICG Model 862146' from Philips [10].

1.2 Project Objective

The project objective is to develop an instrument for impedance cardiography combining the advantages of several earlier designs and exploring novel circuits for signal acquisition and demodulation. The hardware for impedance cardiography consists of a current source, two electrode pairs with one pair for current injection and the other for voltage sensing, impedance detector, differentiator, and ECG extraction circuit. The current source consists of a waveform generator and a voltage-to-current (V/I) converter. The impedance detector includes a voltage sensing amplifier, demodulator, and an amplifier for baseline correction. The ECG extractor low-pass filters and amplifies the signal on the voltage sensing electrodes to get an ECG signal, which is different from the commonly used ECG leads, but is used for ECG-R peak detection to serve as a reference for processing of the ICG signal. The main aim of this project is to develop an impedance cardiograph, with the integration of synchronous demodulation and tracking-based baseline correction to improve the demodulation sensitivity, noise rejection, and ripple rejection, and to reduce the circuit complexity for body-wearable applications.

A circuit based on the impedance converter IC TI/AFE4300 is designed and tested for acquiring the time-varying impedance signal. The impedance sensing chip AFE4300 helps in reducing circuit complexity as it has an internal direct digital synthesizer (DDS) for generating a sinusoidal waveform with amplitude stability, a circuit for impedance measurement using synchronous demodulation, and a 16-bit sigma-delta ADC. The impedance converter IC does not have provision for separating the basal and time-varying components of the impedance signal. To develop an instrument with the flexibility of selecting the excitation current and measuring the time-varying component with a high resolution, additional analog circuits are designed. It consists of a balanced V/I converter, voltage sensing amplifier with improved CMRR, and a baseline correction arrangement. The voltage-controlled balanced current source is used for injecting current into the thorax using the current electrode pair and it avoids the need for a transformer. The instrumentation amplifier configuration with a common-mode feedback to the input of the first stage is used as voltage sensing amplifier, in order to improve the overall CMRR for picking up the voltage across the voltage electrode pair. A dynamic tracking-based baseline correction technique is used to improve the modulation index and thereby the sensitivity for time-varying impedance. The ECG monitoring is carried out using the IC TI/ ADS1298 chip. The design uses a microcontroller for generating the controls for the current source and baseline correction for acquiring the signal. It is used for setting the measurement parameters, reading the measured impedance and ECG via a serial peripheral interface (SPI), transferring the data to the external device via Bluetooth and for dynamic baseline correction with settable sensitivity. For body-wearable applications, the measured time-varying impedance is sent wirelessly via Bluetooth to an external device like PC for processing and visualization.

1.3 Report Outline

The basics of impedance cardiography and some of the impedance cardiography systems developed earlier are described in the second chapter, the design approach and description of hardware and software for impedance cardiograph are presented in the third chapter, and the test results are presented in the following chapter. The last chapter provides a summary and conclusion of the work. Supplementary information on the design is provided in the appendices.

Chapter 2

BASICS OF IMPEDANCE CARDIOGRAPHY

2.1 Cardiac cycle and stroke volume

The cardiac cycle is the period between two consecutive heartbeats. It consists of a phase of relaxation (diastole) and a phase of contraction (systole). The stroke volume (SV) is the blood volume ejected by the left ventricle during one cardiac cycle [7] and it is the difference between the end-diastolic volume (the blood volume inside the ventricle after the ventricular diastole) and the end-systolic volume (the blood volume left inside after the ventricular systole). The cardiac output (CO) is the blood volume ejected from the left ventricle in one minute, and may be calculated as product of the mean SV and the heart rate (HR). Measurement of SV and CO can play a vital role in the diagnosis and treatment of several disorders of the cardiovascular system.

2.2 Impedance cardiography

The measurement of electrical impedance offered by the biological materials such as blood, tissue, bone, muscle, etc. can be used to monitor the change in impedance due to physiological changes and to calculate some of the physiological parameters related to this change. The impedance is monitored by using a pair of electrodes for applying an excitation in the form of current to the body segment and picking up the resulting voltage waveform which gets amplitude modulated due to variations in the impedance [1]−[5]. Demodulation of voltage waveform gives the signal corresponding to the impedance of body segment. The impedance can also be monitored by applying a voltage and measuring the resultant current. However, the voltage-driven measurement is less preferred as it does not permit a direct control of the injected current. Generally, a tetrapolar electrode configuration, with the outer pair of electrodes for current injection and the inner pair for voltage pick-up, is used to reduce the effect of tissue-electrode interface impedance on the picked-up voltage.

Impedance cardiography is a noninvasive method for estimating the stroke volume and cardiac output by sensing the variations in the thoracic impedance during the cardiac cycle. During ventricular ejection, the total volume of the blood in the thorax increases. As the blood has a lower resistivity compared to bone, muscles, and other tissues, the thoracic impedance decreases due to the blood inflow into the thorax. The impedance is sensed by injecting a current of high-frequency and low amplitude (20−100 kHz, < 5 mA) through a pair of electrodes and picking up the voltage developed across another pair of electrodes placed inside the current electrodes [1], [2].

Due to variation in the thoracic impedance, the sensed voltage gets amplitude modulated. Its envelope represents the variations in the thoracic impedance during the cardiac cycle. The stroke volume and cardiac output can be estimated from the impedance waveform using appropriate models and equations.

The frequency of the excitation current is generally 20−100 kHz [1], [2], [5]. The use of high frequency reduces the electrode-tissue interface impedance. It helps in the separation of the impedance related voltage from other bio-electric signals such as ECG and EMG. It is also helpful in suppressing the carrier-related ripple in the demodulated output. The upper limit on the frequency is limited by parasitic impedances. Also, at a higher frequency (> 500 kHz), the current does not penetrate deep in the thorax and the time-varying component of the impedance signal decreases. The excitation current should be kept at a low level to avoid the possibility of any physiological effects. Earlier designs used current of less than 5 mA. For body-wearable applications, lower current of 0.1 mA is preferable.

In the frequency band of 20−100 kHz, the thoracic impedance is almost resistive. It consists of a basal impedance and a time-varying component superimposed on the basal impedance. The basal impedance is due to organs, muscle, bone, etc., and remains constant with time. The time-varying component is mainly contributed by the variation in the thoracic blood volume during the cardiac cycle. Impedance variation due to respiration and motion also contribute to the time-varying component. Typically, the basal impedance of the thorax is around 20−200 Ω, and the change in impedance is typically 0.1−2% of the basal impedance [6].

2.3 Electrode configuration

Electrodes constitute an interface between the electronic current in the measuring circuit and the ionic current in the tissues. For noninvasive measurements, silver/silver-chloride electrodes are most commonly used to avoid electrode polarization. The type and placement of electrodes are important in impedance cardiography. The impedance measurement can be carried out using two or four electrode configurations. In the two-electrode configuration, the same set of electrodes is used for current injection and voltage sensing [6]. In this electrode arrangement, the changes in the contact impedance of either electrode will create an error in the sensed voltage [2]. In the four-electrode or tetrapolar electrode configuration, two outer electrodes are used for injecting current into the thorax, and the inner two electrodes placed in the region enclosed by the current electrodes are used for picking up the voltage developed across the thorax. The current injecting pair of electrodes are placed across the thorax with one electrode placed at the base of the neck, and the other placed at the xiphoid level [6]. It should be placed in such a way that the current density across the thoracic region remains uniform in order to estimate the stroke volume accurately.

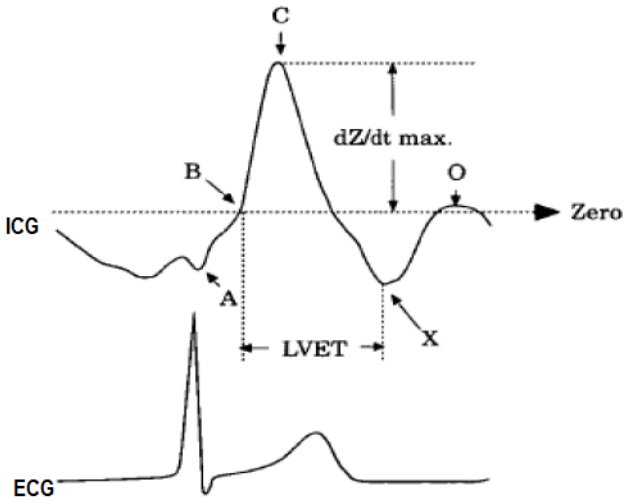


Figure 2.1: ICG waveform [1]

Because of the high input impedance amplifier, used for voltage sensing, the measured voltage is not affected by the contact impedance of the electrodes. It is observed [6] that the current density distribution is non-uniform near the electrodes and become approximately uniform as one goes away from current injecting electrodes. The voltage sensing electrode should be placed in such a way that the region between them has approximately uniform current density and includes the region contributing to the variation in the thoracic impedance during the cardiac cycle. Use of tetrapolar electrode configuration is now well established in impedance cardiography.

Spot and band are the two types of electrodes which are commonly used in impedance cardiography. Band electrodes provide more uniform current density with lesser waveform variability [2], but they are difficult to apply in clinical settings, expensive, and also uncomfortable to wear. The spot electrode can be placed easily and result in lower motion artifacts, but the corresponding current density is nonuniform, which can results in error in the measurement.

2.4 Models and Equations

The demodulated impedance $Z(t)$ has a basal component Z_0 and a time-varying impedance $z(t)$ superimposed on it. ie, $Z(t) = Z_0 + z(t)$. The negative first derivative of the impedance waveform, i.e $-dZ/dt$ or $-dz/dt$, is known as the impedance cardiogram (ICG) [1], [2]. The ICG and ECG waveforms are shown in Figure 2.1 The points on the ICG waveform marked as the A, B, C, X, and O points are the characteristic points and are related to various cardiac activities. The ECG waveform acts as a reference for the ICG signal. The A point is the downward deflection due to the atrial contraction. The B point is related to the aortic valve opening. The C point is the peak occurring during systole due to increased blood flow in the aorta. The X point coincides with the closure of the aortic valve. The O point is the diastolic upward deflection, the maximum of which

coincides with mitral valve opening snap [7]. Two important parameters used in the stroke volume estimation are the left ventricular ejection time T_{LVET} and the ICG peak $(-dZ/dt)_{\max}$. The time duration between the B and X points is known as the left ventricular ejection time (T_{LVET}). The product of $(-dZ/dt)_{\max}$ and T_{LVET} is used for calculating the stroke volume.

To relate thoracic impedance to the stroke volume, Kubicek et al. [5] proposed a parallel column model. The thorax is modeled to have conducting material with basal impedance Z_0 connected in parallel with a cylindrical column with variable impedance having uniform cross-sectional area A, length L, and resistivity ρ, as shown in Figure 2.2. The variable impedance changes as the cross-sectional area of the cylinder changes from zero to a finite value. This model assumes that there is no outflow of blood from the thorax during systole, and the volume of the variable impedance column is zero before systole [5]. Hence the maximum change in the impedance ΔZ impedance column is zero before systole [5]. Hence the maximum change in the impedance ΔZ and the maximum change in the volume ΔV can be related as,

$$\Delta V = \left(\frac{\rho L^2}{Z_O^{\,2}}\right)\Delta Z \tag{2.1}$$

Later, the Kubicek equation was modified by considering the outflow of blood from thorax during the later part of the systole. In this formula, a forward extrapolation technique is used and the extrapolated time-varying impedance ΔZ is given by the product of the ICG peak, $(-dZ/dt)_{\max}$, and the left ventricular ejection time T_{LVET}. The modified equation is given as,

$$\mathrm{SV} = \left(\frac{\rho L^2}{Z_O^{\,2}}\right)\left(-\frac{dZ}{dt}\right)_{\max} T_{LVET} \tag{2.2}$$

where SV is the stroke volume, L is the distance between voltage sensing electrodes and ρ is the blood resistivity. The major limitations of the Kubicek equation are the assumption of the thorax as a cylinder, difficulty in measurement of L and determining the resistivity of blood. An alternative equation was proposed by Sramek et al. [4], modeling the thorax as a truncated cone, replaced the resistivity value by value dependent on Z_0, L and volume V. Estimated volume is $L^3/4.25$ and L was found to be 17% of a person's height H. The Sramek equation is given as,

$$\mathrm{SV} = \left(\frac{(0.17H)^3}{4.25Z_O}\right)\left(-\frac{dZ}{dt}\right)_{\max} T_{LVET} \tag{2.3}$$

Bernstein et al. [8] gave a correction factor δ to the above equation to compensate for subject's morphological make-up. The Sramek–Bernstein [8] equation is given by,

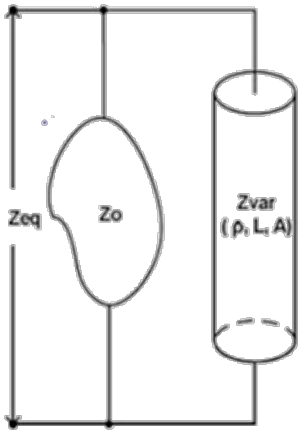


Figure 2.2: Parallel column model for thorax [5]

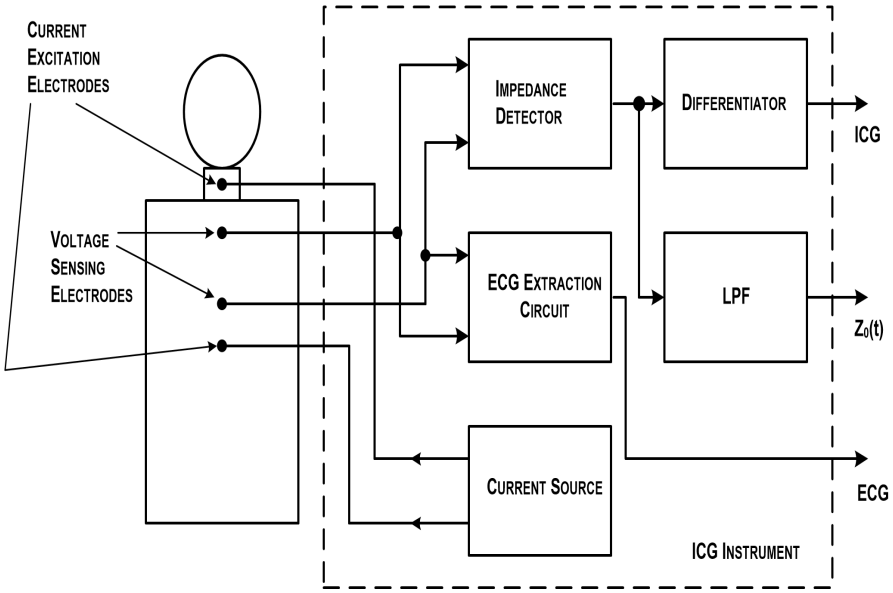


Figure 2.3: Block diagram for impedance cardiography

$$\mathrm{SV} = \delta\left(\frac{(0.17H)^3}{4.25Z_O}\right)\left(-\frac{dZ}{dt}\right)_{\max} T_{LVET} \tag{2.4}$$

2.5 Instrumentation for impedance cardiography

The basic block diagram for ICG measurement is shown in Figure 2.3. It consists of a current source, current injecting and voltage sensing electrodes, impedance detector, differentiator, and ECG extractor. The electrodes are placed on the thorax region in a tetrapolar configuration. A high-frequency, low amplitude current is injected into the thorax through the current injecting

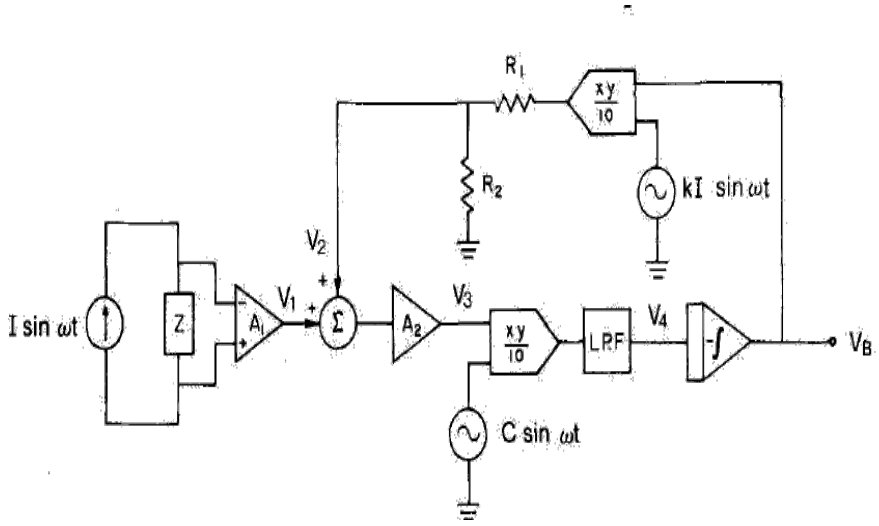


Figure 2.4: Self-balancing loop reported by Arenson et al. [11]

electrodes. The voltage developed is picked-up by the voltage sensing electrodes and is input to the impedance detector. Impedance detector comprises a high input impedance voltage sensing amplifier and a demodulator. The voltage sensing amplifier amplifies the high-frequency signal while rejecting artifacts and other interferences. Demodulator extracts the time-varying impedance signal by demodulation of the amplitude modulated carrier. The impedance signal $Z(t)$ is low-pass filtered to get the basal component Z_0 and high-pass filtered and amplified to get the time-varying component $z(t)$. The time-varying component is differentiated to get the impedance cardiogram (ICG). The ECG extraction circuit consists of an instrumentation amplifier with bandpass filtering. The ECG signal serves as a reference for the detection of characteristic points of the ICG waveform. To demodulate, the impedance detector needs to be highly sensitive to impedance variation signal and able to reduce additive noise in the sensed voltage and suppress ripples related to the excitation frequency.

In thoracic impedance measurement, the baseline varies from subject to subject and with electrode placement, subject movement, and respiration. Due to the overlapping of the signal spectrum with that of the drift, a high-pass filter cannot be used for baseline correction. An automatic cancellation of offset drift is required for avoiding saturation of the analog processing circuits. Several automatic baseline correction methods have been reported as a part of the ICG instrumentation in the literature, including self-balancing system [11], successive approximation register (SAR) based method [6], [12], etc.

Arenson et al. [11] reported a self-balancing dual channel impedance sensing using a single current excitation with a resolution of 0·002 Ω. Sensed voltage from each channel is demodulated using a phase-sensitive synchronous detector with self-balancing null detection. In the self-balancing loop, as shown in Figure 2.4, the output V_B is multiplied by excitation current and added to the sensed voltage; the resulting voltage is demodulated using a multiplier and low-pass filter,

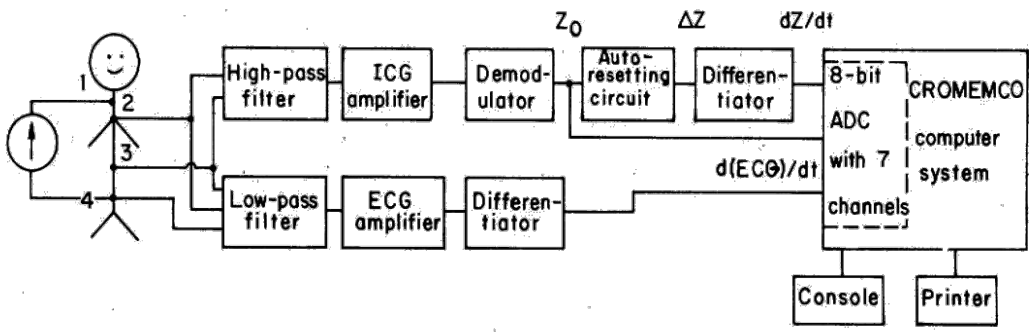


Figure 2.5: Block diagram of the ICG system as developed by Qu et al. [6]

followed by an integrator to get the output. The circuit incorporates both fine and coarse feedback loops to achieve rapid, automatic balancing of the resistive component. The fine control is set to zero during coarse balancing, and the coarse control is put on hold during fine balancing. Shankar [12] designed an automatically balancing electrical impedance sensor which utilizes two 10-bit multiplying digital to analog converters and two connected 12-bit successive approximation registers (SAR). The SAR and DAC approximate the baseline drift, which is subtracted from the input signal, and the difference is amplified to give the output. Whenever the output voltage crosses the threshold levels, a start pulse is given to SAR, and successive approximation is initiated to bring the output to near the center of the range. The automatic balancing unit will resets ΔZ within 0.5 mΩ of zero when Z exceeds 20 mΩ. To remove voltage pickups, a transformer coupling is used for excitation and the excitation current is also sensed for reference. The balanced demodulator chip LM1496 is used for extracting the impedance variations.

Qu et al. [6] developed an impedance cardiograph using spot electrodes with tetra polar electrode configuration for minimizing the effect of motion artifacts with SNR improvement of 13.6- 45.5% with reference to band electrodes at rest. The block diagram of the ICG system is given in Figure 2.5. The excitation source (5 mA, 20−100 kHz) is a Wein bridge oscillator and V/I converter. The sensed voltage is high-pass filtered (> 16 kHz) and amplified using the instrumentation amplifier. The demodulation uses a full-wave precision rectifier, and the output signal is passed through low-pass filter (< 0.72 Hz) to obtain basal impedance Z_0. A differentiator is used to generate the ICG signal from the demodulated impedance Z. The auto balancing technique is incorporated for baseline correction using SAR and two comparators. Also, an ECG sensing circuit is included as a reference for ICG. It includes low-pass filter, instrumentation amplifier, and differentiator circuit to reduce the motion artifacts. The optocoupler units are used for isolation between acquired signals (Z_0, dZ/dt, d(ECG)/dt) and PC.

Several other circuits for impedance cardiography have used a precision rectifier or a peak detector [14], [15] or a synchronous demodulator followed by a higg-pass filter [16], [17] or

integrated impedance measurement chips such as TI/AFE4300 [33] and AD/AD5933 [38], [19], [18], without incorporating a baseline correction technique to account for the drift in the baseline. Lozano et al. [17] reported an impedance sensor in which impedance signals are obtained at two frequencies by measuring both real and imaginary parts of *Z*. The excitation current, as a sum of two sinusoidal currents (0.72 mA at 110 kHz and 0.37 mA at 68 kHz), is digitally synthesized using EPROM, DAC and a V/I converter. The tuned isolation transformers are used for excitation as well as voltage sensing. The excitation current is monitored using a series resistance which provides the ADC reference. Coherent demodulation is carried out using analog multiplexers and a low-pass filter. The in-phase and quadrature components of a square wave with compensation for phase shifts act as a reference to extract the real and imaginary parts of *Z*. From the demodulated signal, Z_0 is removed using HPF (> 0.1 Hz) and $z(t)$ is amplified. The resulting signals are acquired with 12-bit ADC and are digitally processed using a PC.

Palko et al. [15] designed a device for measuring complex electrical bio-impedance. Figure 2.6 shows the block diagram of the design. The measurement is based on the tetrapolar electrode method with a current of 1 mA and 20–200 kHz generated using sinusoidal VCO and a V/I converter. The sensed voltage is given to an instrumentation amplifier. The basal impedance Z_0 is extracted using a peak detector, and the phase is estimated using a modified zero-crossing method. The excitation and sensed signals are applied to fast comparators for zero- crossing detection. The phase can be measured in the range of 0–45° with 0.1º resolution. The ECG amplifier is also included for the generation of the reference signal. The output signals after demodulation are coupled to ADC using analog isolators and then processed digitally on a PC to get the time-varying component.

Panfili et al. [14] developed a device for continuous monitoring of the cardiac output based on impedance cardiography technique with Bluetooth connectivity for sending the acquired ICG signal. The source of current excitation is a voltage oscillator (32 kHz) followed by PNP and NPN transistor pair which generates a current 20 uA peak-to-peak. The voltage developed across voltage electrodes is sensed using the instrumentation amplifier followed by a band-pass filter. The demodulation uses synchronous envelope detection by sampling at the excitation peaks. The output is low-pass filtered (1.7 Hz) to get Z_0 and band-pass filtered (0.08−15 Hz) for the time-varying component $z(t)$.

Vondra et al..[16] reported a two-channel bio-impedance monitor to measure the cardiac output into the aorta and the pulmonary artery simultaneously. The block diagram of the two-channel bio-impedance monitor is shown in Figure 2.7. The second channel is applied

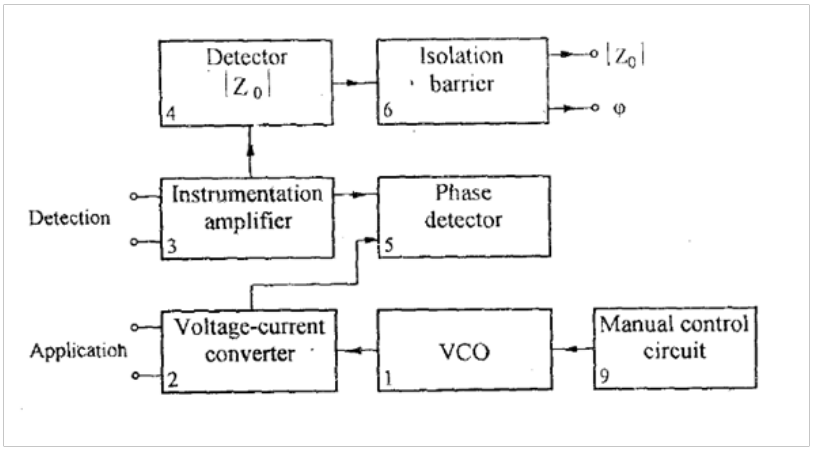


Figure 2.6: Block diagram of bio-impedance monitor as reported by Palko et al. [15]

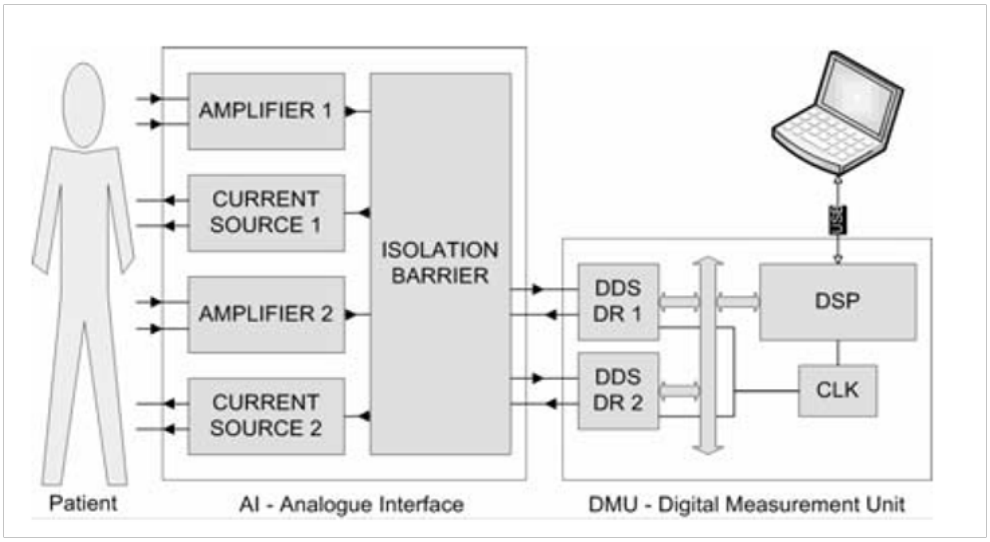


Figure 2.7: Block diagram of two channel bio-impedance monitor reported by Vondra et al. [16]

perpendicular to the perpendicular to the first one, and each channel has its own excitation frequency. Coherent demodulation technique is used for extracting magnitude and phase of the impedance. The DDS and DAC are used for excitation generation. The measured bio-impedance signal is digitized using ADC, and digital receiver (DR) block will perform mixing and down conversion. The digital measuring unit is isolated from the analog front end. The measuring unit is connected to PC by USB, and digital filtering is applied on the received signal for separation of Z_o and $z(t)$.

Ferreira et al. [19] [26] proposed a portable bio-impedance monitor for continuous impedance using the impedance network analyzer chip AD5933 [38] to reduce the overall chip count. The chip performs high-speed single frequency continuous impedance measurements with minimum estimation time. It uses a bipolar measurement configuration and does not provide an

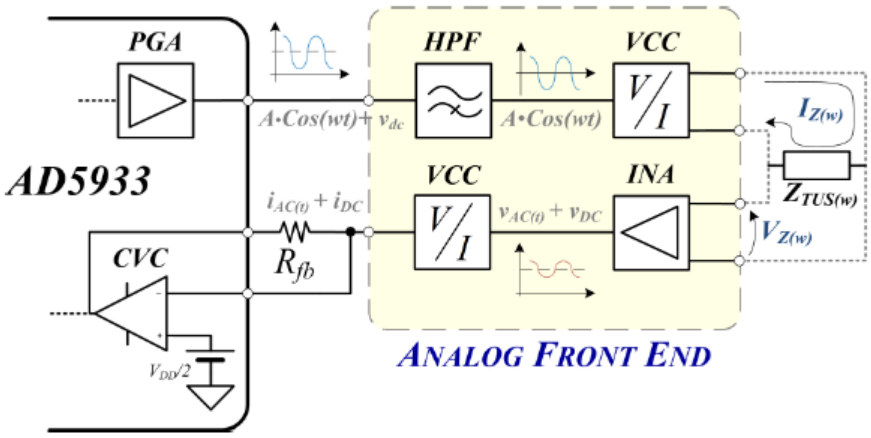


Figure 2.8: Block diagram of Analog front end (AFE) [19]

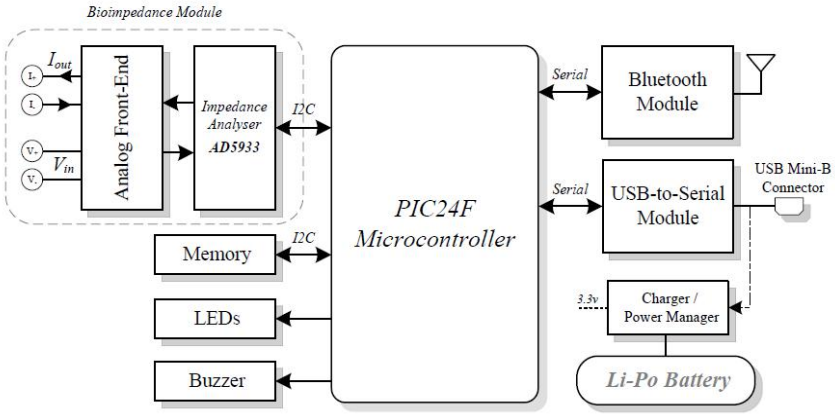


Figure 2.9: Functional block diagram of portable bio-impedance monitor as reported by Ferreira et al. [19]

integrated baseline correction mechanism which limits the measurements of small impedance variations superimposed on a basal component. Hence a 4-electrode analog front end consisting of two parts, one for current excitation and the other for voltage sensing is designed as shown in Figure 2. 8. The chip has a DDS core to synthesize the frequency int the range 1–100 kHz sinusoidal waveform.. In the excitation part, the voltage output of AD5933 is converted to current (400 uA, 100 kHz) using a V/I converter. The sensing part consists of an instrumentation amplifier and V/I converter before applying to demodulator chip. For measuring the complex impedance digital synchronous demodulation is carried out by calculating 1024-point DFT of sampled values of the sensed voltage. It gives the real and imaginary part of complex impedance in two's complement form, and the demodulated signal can be acquired at a sampling frequency of up to 200 Hz. For transferring data to PC, Bluetooth connectivity is used. The functional block diagram of the design is shown in Figure 2.9. The impedance converter IC is designed for voltage driven

measurements of impedance from 1 kΩ to 10 MΩ. As most of the bio-impedance measurements involve less than 1kΩ impedance and current excitation, additional circuits are needed.

Weyer et al. [18] reported a wearable impedance cardiography device using the impedance measuring chip TI/AFE4300, microcontroller TI/MSP430, and ECG chip TI/ADS1298. The AFE4300 has a current excitation unit, and two demodulation units such as full-wave rectifier and in-phase/quadrature (I/Q) synchronous demodulator. The current excitation unit consists of a 10-bit direct digital synthesizer (DDS), 6-bit DAC, and low-pass filter (< 150 kHz). The demodulation block includes a differential amplifier, synchronous demodulator, and 16-bit ADC with settable sampling frequency. It has a set of 8 simultaneous sampling, 24-bit, sigma-delta ADCs with built-in programmable gain amplifiers (PGA). Both the chips use SPI interface to read the conversion data, and read from and write to the registers. For the estimation of basal impedance Z_o, full-wave rectifier followed by low-pass filter is used. For time-varying component $z(t)$, the in-phase quadrature synchronous demodulator block is used. The microcontroller MSP430 is used to acquire the ICG and ECG over SPI from AFE4300 and ADS1298 and pass to Bluetooth via UART. The relative error in Z measurement is less than 1%.

2.6 Some hardware designs developed at IIT Bombay

Several ICG instruments have been developed as part of M. Tech. projects at IIT Bombay. Some of the specific blocks of the design are reviewed in the following subsections.

2.6.1 Current source

Current source should have high amplitude stability as any variation in amplitude will lead to noise in the sensed voltage. It is generally realized using an oscillator to generate a voltage at the desired frequency and a V/I converter. Wein bridge oscillator with a stabilization loop using peak detector and error amplifier [20], voltage-controlled oscillator (VCO), precision function generator [21], direct digital synthesizer (DDS) [23], [24], [25], etc. have been used as voltage sources. DDS provides excellent waveform stability, and permits programmable frequency and phase shift. A digital potentiometer IC [24] can be used for amplitude control.

The V/I converter used to convert the sinusoidal voltage signal into a current for excitation should have high output impedance so that variation in the tissue-electrode impedance and the thoracic impedance does not affect the current injected into the thorax. Also, the current should not be effected by common mode pick-ups and stray capacitances. The commonly used V/I converter is an inverting op amp amplifier with the load connected in the feedback, as shown in Figure 2.10 with I1 and I2 as the current electrodes. The injected current is

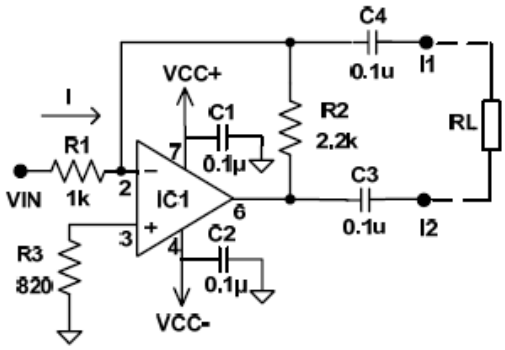


Figure 2.10: V/I converter with the load connected in feedback [25]

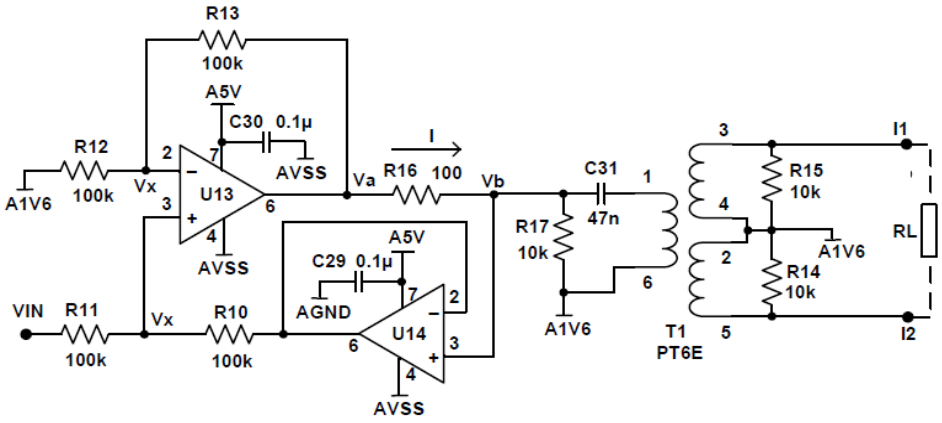


Figure 2.11: Modified Howland current source with centre tapped pulse transformer [24]

$$I \approx V_{in} / R_1 \tag{2.5}$$

The resistor R2 is provided to limit the dc gain of the circuit to avoid saturation due to dc errors. The major drawback of this circuit is that one of the terminals is at virtual ground and therefore the terminal voltages are not balanced with respect to the ground and it may lead to common mode pickup and stray currents. The stray capacitance at the inverting input terminal may cause instability. Balanced current source using pulse transformer [22], transformer-less balanced current source [20], and modified Howland current source [25], [24] have been reported as solutions for this problem. Figure 2.11 shows a modified Howland current source using single-supply op amp circuit and pulse transformer for balanced output. The output current is given as

$$I = V_{in} / R_{16} \tag{2.6}$$

For high output impedance, the resistance ratios R_{13}/R_{12} and R_{10}/R_{11} have to be matched.

In the design by Desai [23], a V/I converter was realized using operational trans-conductance (OTA) amplifier OPA861 IC from Texas Instruments as shown in Figure 2.12. In this

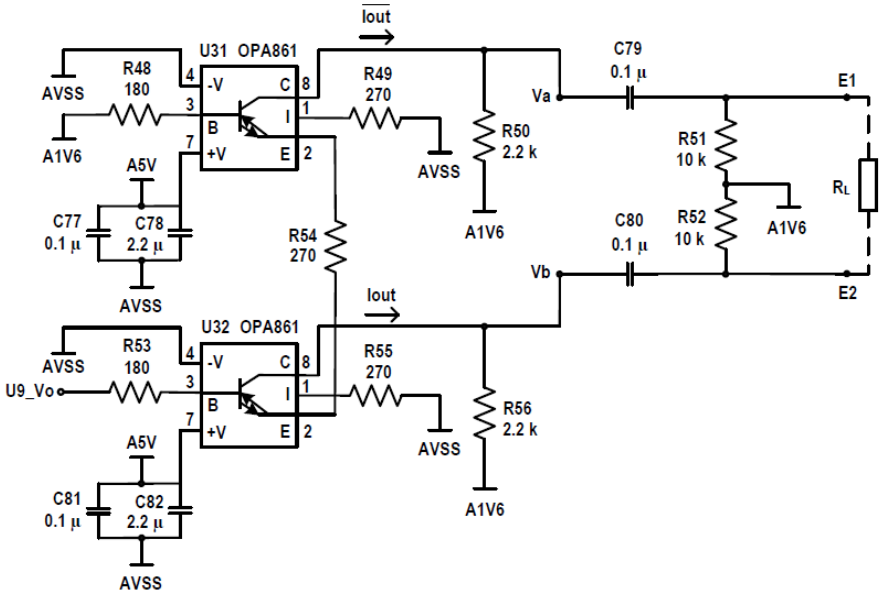


Figure 2.12: V/I converter using trans-conductance amplifier [24]

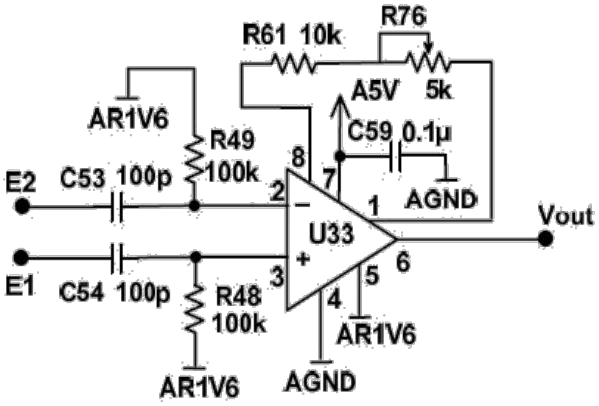


Figure 2.13: Voltage sensing amplifier using INA155 [24]

circuit, two OTA ICs are used to provide complementary current outputs. With balanced complementary outputs, the need for transformer is avoided. The output current is given as

$$I = \alpha(V_{\text{in}} - V_{ref}) / (R_{54} + (2/ g_m) \quad (2.7)$$

where α is the current transfer ratio of the collector current to the emitter current (nearly 1), of the OTA, g_m is the OTA trans-conductance, R_{54} is the emitter resistance, V_{ref} is the A1V6 point (1.6 V above analog ground) and V_{in} is the voltage at U9_Vo. The resistors R48 and R4, being in series with high input impedances, do not play any role in determining the current. The real difficulty is that any difference in the current transfer ratio of the two OTAs results in an imbalance in I_{out} and $\overline{I_{out}}$. The resistors R50, R56, R51, and R52 are used to reduce the effect of this imbalance, but decrease the output impedance of the V/I converter.

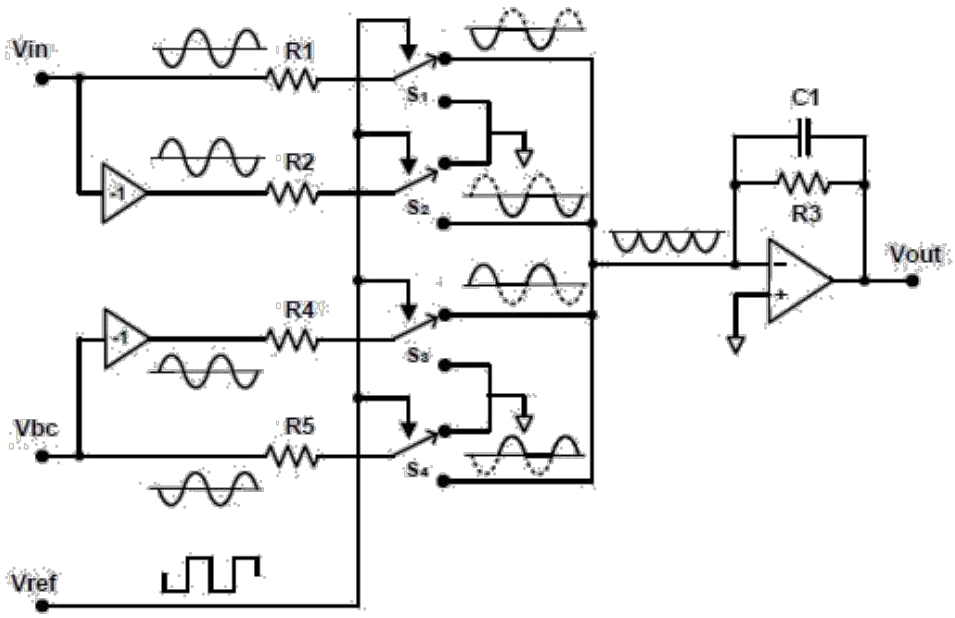


Figure 2.14: Synchronous demodulation using current steering with base line correction [24]

2.6.2 Voltage sensing amplifier

The voltage sensed by the voltage sensing electrode pair is amplified by a differential input amplifier with high input impedance, high CMRR, and high-pass (cutoff frequency > 10 kHz) filtering for rejecting low-frequency bioelectric signals and other artifacts. Instrumentation amplifier INA155 IC from Texas Instruments has been used in [19], [24] as a voltage sensing amplifier, as shown in Figure 2.13. The high-pass filter at the front end helps in rejecting pick-ups.

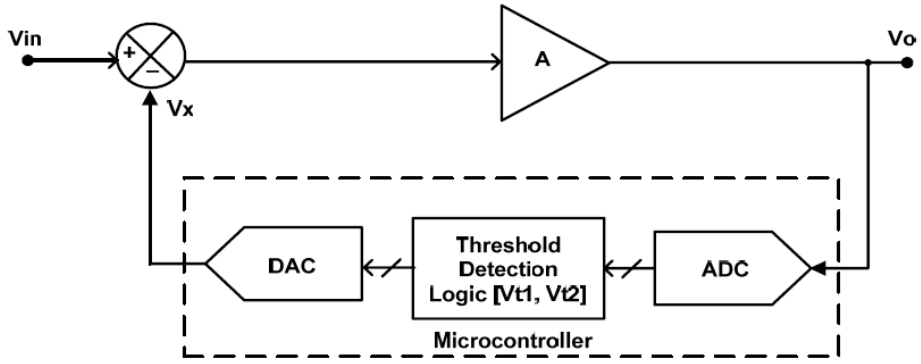
2.6.3 Demodulator

In order to extract the time-varying component, the sensed voltage is demodulated after amplification by the voltage sensing amplifier. The time-varying component of the thoracic impedance is 0.1−2% of the basal impedance, and the sensed voltage has correspondingly low modulation index. The demodulator circuit should provide high noise rejection and carrier ripple rejection without introducing distortion in the detected output.

A combination of a diode-based asynchronous full-wave precision rectifier and low-pass filter was used in the design by Manigandan [22] and Naidu [27] to extract the envelope rejecting the carrier ripple. Use of low-pass filter introduces phase distortion. Other designs include the voltage-clamp amplifier IC based demodulation by Naidu [14], vector lock-in amplifier with synchronous detection by Sarvaiya [21], slicing amplifier based demodulation by Patil [25], synchronous demodulation scheme using current steering with baseline correction by Mishra [24], and synchronous demodulation using OTAs by Desai [23].

In the slicing amplifier based demodulation as reported earlier by Fourcin [28], the sensitivity is improved by slicing the top of the amplitude modulated voltage up to the modulation depth and then amplifying the sliced signal prior to synchronous detection. Patil [25] implemented this demodulation scheme using two voltage clamp amplifiers, one as full wave rectifier and the other as slicing amplifier. But this method increases the carrier ripple and the noise in the output. For ripple rejection, the synchronous sampling method is used in [25]. i.e., the sliced signal is sampled at carrier peak, and the value is held until the next peak. As noise can corrupt all samples of the waveform, sampling at carrier peaks does not reduce the noise. Asynchronous peak detector demodulation also gives poor results because the presence of noise can alter the actual peak location. Hence the major issues faced by the demodulation circuits are carrier ripple, sensitivity, and noise. Noise can be removed by synchronous demodulation. Sensitivity can be improved by amplifying the signal either by high-pass filtering the demodulated output or after baseline correction. Low-pass filtering and sampling at peaks after synchronous demodulation are the solutions for carrier ripple removal.

Synchronous demodulation scheme using current steering with baseline correction was proposed by Mishra [24], as shown in Figure 2.14, to solve the three issues to a large extent. Here resistors R1, R2 are used in series with the input of the SPDT switches S1and S2 to convert an input voltage to current so that it is either steered to the analog ground or to op amp inverting terminal which is at virtual ground. Switches are controlled by a clock (Vref) which is synchronous with the sinusoidal current source. The input signal Vin is given directly to the switch S1, and the inverted Vin is given to the switch S2. Hence the current entering at the inverting terminal of the op amp is an inverted full-wave rectified signal. The rectified signal is then inverted and low-pass filtered by the op amp with R3 and C1 in feedback, to get the final demodulated output. Since the rectification is synchronous, only those components in Vin are passed which are in phase with the clock signal Vref. Hence this approach has better noise and interference rejection capability. The voltage across the switches always remains zero as it is connected to either virtual ground or analog ground. As a result, there is no noise due to transients caused by voltage switching. As this approach is based on synchronous current steering, it does not result in any sharp transitions both at input and output terminals of the op amp. Hence the circuit performance is not affected by the slew rate of the op amp. Each SPDT used here is realized using two analog switches with complementary controls and hence charge injections through the two controls approximately cancel each other. A baseline correction mechanism is integrated in this demodulation scheme by introducing a sinusoidal voltage (Vbc) so that the restriction on the gain (R3/R1) can be relaxed and sensitivity can be improved. The switches S3and S4 operate in the same fashion as the switches



S1 and S2, with their control polarities reversed. As a result, the full-wave rectified signal at the output will be of 180° phase shift and hence gets subtracted from the rectified signal. A large gain can be used in low-pass filter to increase the sensitivity. Any carrier ripple present at the demodulated output can be rejected by sampling at peaks of the carrier signal using an ADC. Hence this synchronous demodulation scheme using current steering with high-speed analog switches and au

Figure 2.15: Tracking based baseline correction [31]

correction logic is also implemented to compensate phase shift between a square wave and sensed voltage [24]. Although the scheme is very attractive, its implementation in [24] did not provide satisfactory result. The basic problem with the implementation was a large chip count.

In the design by Desai [23], the op amps used in the earlier design [24] were replaced by a pair of OTAs to convert the sensed voltage into a current. The use of OTAs reduces the error caused due to the phase shifts in the op amps, and particularly the inverting amplifier. The demodulation circuit involves a complementary pair of current realized using two OTAs. The actual implementation was not successful due to a large chip count and PCB layout related problems.

2.6.4 Baseline correction circuit

The drift in the basal component Z_o due to breathing, electrode placement, offset drift in analog signal conditioning circuits, body movements, and other motion artifacts can lead to saturation of the analog processing circuits and reduction in the input dynamic range of the data acquisition circuits. High-pass filtering of the demodulator output using analog filtering introduces distortions in the signal due to frequency response and nonlinear phase shift of the filter. This problem can be solved to a large extent by using digital filter with linear phase response, but that is feasible only if the baseline signal can be acquired using an ADC without crossing its input range. For an effective use of the ADC precision, the large drift in the signal should be removed by using

a baseline correction circuit. After amplification of the sensed signal, we can divide it into two channels. In the first channel, the signal is low-pass filtered to extract the drift component. In the second channel, one signal is delayed using an analog time delay circuit [42]. Then the drift is subtracted from the delayed signal. This method requires the delay of analog time delay circuit equal to the delay introduced by low-pass filtering. Also, there are chances of saturation in the first amplifier stage itself.

A baseline correction circuit based on successive approximation register (SAR) has been presented in [6], [12]. The SAR method requires *n* clock cycles for an *n*-bit SAR, and the signal is not usable during that interval. Tracking was used in [31] for faster correction of the baseline to keep the signal within the input range of the ADC, as shown in Figure 2.15. In this method, the circuit tracks whether the input signal is lying between two predefined threshold levels. Whenever the signal goes out of the range, an up/down counter increases or decreases its count depending upon the direction in which the signal is drifting. The counter output is given to a DAC which generates the required correction voltage that has to be subtracted from the input signal. If the output goes above the upper threshold, the counter is increased by a step and hence the DAC output is increased by ΔV_c. Similarly, if the output goes below the lower threshold, the counter is decreased by one step and the DAC output is decreased by ΔV_c. The correction voltage V_c is given by,

$$V_c(t_n) = \begin{cases} V_c(t_{n-1}) + \Delta V_c, & V_c\left(t_{n-1}\right) > V_{th} \\ V_c(t_{n-1}) - \Delta V_c, & V_c\left(t_{n-1}\right) < V_{tl} \\ V_c\left(t_{n-1}\right), & \text{otherwise} \end{cases} \tag{2.8}$$

The output signal is sampled by ADC and the appropriate data are output to DAC to generate the correction voltage. As the baseline correction algorithm is implemented using a microcontroller, the thresholds can be changed easily.

In the demodulation technique using synchronous demodulation scheme using current steering [24], no separate hardware is required for tracking and correction of baseline drift. i.e., the baseline correction can be implemented in the demodulator itself. The amplitude of the baseline correction signal is controlled by a digital potentiometer; microcontroller updates the wiper once the demodulator output crosses the predefined thresholds.

2.6.5 ECG extractor and differentiator

ECG signal is extracted from the voltage sensing electrodes, and the R-peaks of ECG are used as reference in ICG processing. In the designs by Manigandan [22] and Naidu [27], the ECG extraction comprises a low-pass filter with 40 Hz cutoff at the input of an instrumentation amplifier to reject the high-frequency carrier. The instrumentation amplifier amplifies the low-frequency

ECG signal and cancels any common mode pick-up. The output is filtered by a cascade of a low-pass filter and a high-pass filter having having cutoff frequencies 20 Hz and 1.6 Hz, respectively, to get the ECG signal [24].

The demodulator output $Z(t)$ is differentiated to obtain the ICG signal. Either an analog differentiator reported by Patil [25] and Mishra [24] or a digital differentiator [23] can be used for this purpose.

2.6.7 Electrode contact impedance indicator

It indicates the lack of proper contact between the skin and the electrodes. When the contact is not proper, the demodulator output will saturate as the impedance is very high. Either a comparator is used to compare between demodulated output and output corresponding to normal impedance or the ADC output of demodulator output can be compared with a threshold value in the software itself which eliminates the hardware as reported by Mishra [24]. The microcontroller can indicate the improper contact by glowing an LED.

Chapter 3

IMPEDANCE CARDIOGRAPH DESIGN: HARDWARE AND SOFTWARE

3.1 Introduction

The hardware of an impedance cardiograph consists of a current source, two electrode pairs with one pair for current injection and the other for voltage sensing, impedance detector, differentiator, and ECG extraction circuit. The current source consists of a waveform generator and a voltage-to-current (V/I) converter. The impedance detector includes a voltage sensing amplifier, demodulator, and an amplifier for baseline correction. The baseline corrected output of the demodulator is applied to the differentiator, which outputs the ICG signal. The ECG extractor low-pass filters and amplifies the signal on the voltage sensing electrodes to get an ECG signal, which is different from the commonly used ECG leads, but is usable for ECG-R peak detection to serve as a reference for processing of the ICG signal. Several circuits [6], [11]−[19] have used a precision rectifier or a synchronous demodulator followed by a high-pass filter or baseline correction for separating the time-varying component. We present a circuit using synchronous demodulation and integrated baseline correction [31] to improve the noise suppression and ripple rejection, with a low chip count for the ambulatory recording of ICG signal.

The design approach for synchronous demodulation with integrated baseline correction is shown in Figure. 3.1. A synthesizer with settable frequency 'F' provides excitation voltage with amplitude controlled by 'A1'. A V/I converter provides the excitation current to the electrode pair I1-I2. The voltage across the electrode pair V1-V2 is amplified by a sensing amplifier. A difference amplifier with the sensed voltage and a settable fraction of the excitation voltage, controlled by 'A2', as the inputs is used as the baseline correction amplifier. The resulting voltage is applied to the synchronous demodulator with the excitation as the reference for improving noise suppression. The demodulated output is sampled at a sub-multiple of the excitation frequency for improved ripple rejection. A microcontroller with internal ADC is used for outputting the excitation controls 'F' and 'A1' and the baseline correction control 'A2', signal acquisition and differentiation of the impedance signal, and outputting the signals.

For a low chip-count circuit, the design approach of Figure. 3.1 is realized using the impedance converter IC 'TI/AFE4300' [33], [34], having a DDS for sinusoidal excitation voltage with settable frequency, an impedance measuring circuit using synchronous demodulation with in-phase and quadrature (I/Q) outputs, and a 16-bit ∑-Δ ADC with settable sampling frequency; a microcontroller; and a few additional circuit blocks, as shown in Figure. 3.2. The impedance converter IC does not have provision for separating the basal and time-varying components of the

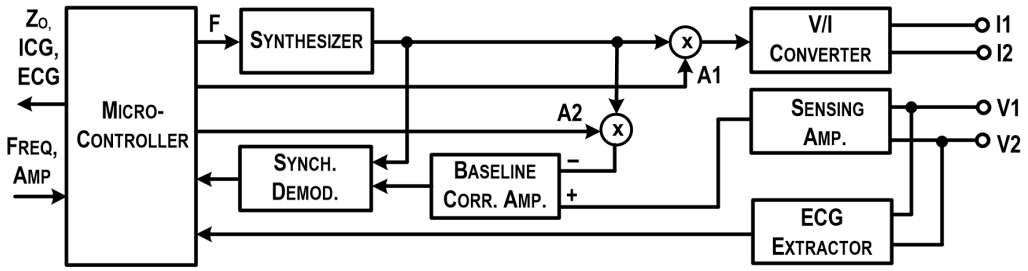


Figure 3.1: Design approach

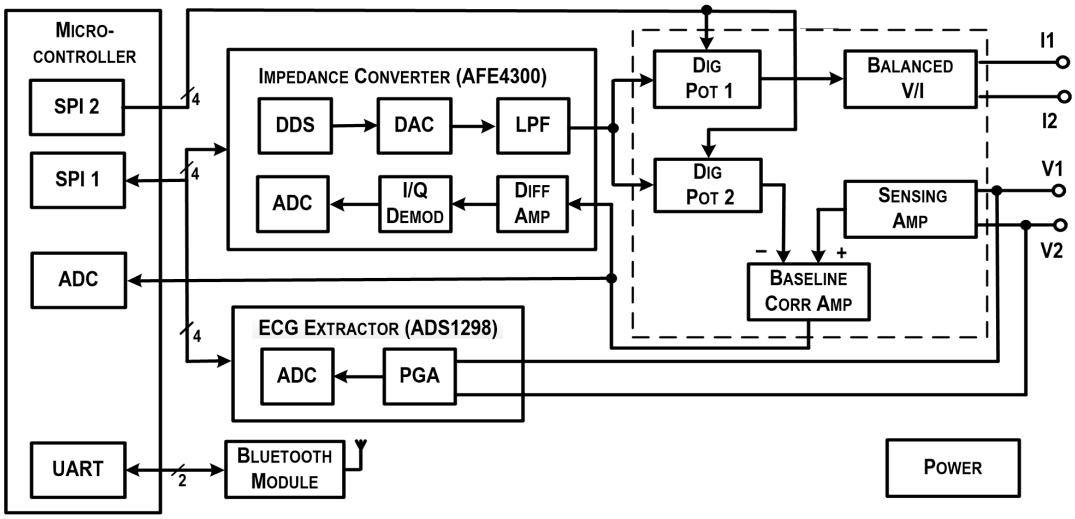


Figure 3.2: Block level schematic of the impedance cardiograph.

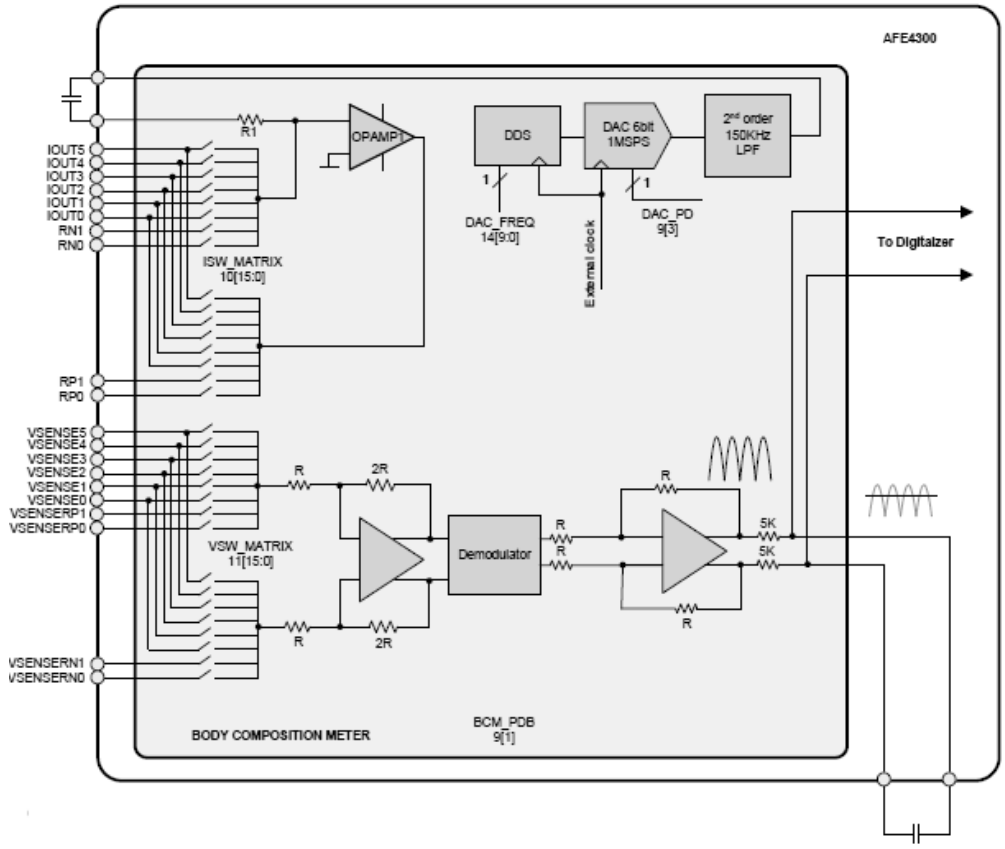
impedance signal. To develop an instrument with the flexibility of selecting the excitation current and measuring the time-varying component with a high resolution, additional analog circuits are designed. It consists of a balanced V/I converter, voltage sensing amplifier with improved CMRR, and a baseline correction arrangement.

In the block level schematic shown in Figure 3.2, the excitation circuit has a digital potentiometer 'Dig Pot 1' and a V/I converter with a balanced current output for injecting stray-insensitive excitation current into the thorax using the electrode pair I1-I2, which avoids the need for a transformer. The voltage across the electrode pair V1-V2 is amplified by a sensing amplifier, with an instrumentation amplifier configuration along with a common-mode negative feedback for enhancing the CMRR. The output is given to a difference amplifier ‘Baseline Corr Amp’ with the excitation voltage with its amplitude controlled by a digital potentiometer 'Dig Pot 2' as the second input. The resulting output is input to the I/Q demodulator of the impedance converter chip to extract the time-varying component of the impedance signal. Here, the demodulation is in the analog domain. The carrier ripple present in the demodulated output is rejected by sampling the output using the on-chip sigma-delta ADC of the impedance converter with sampling instant

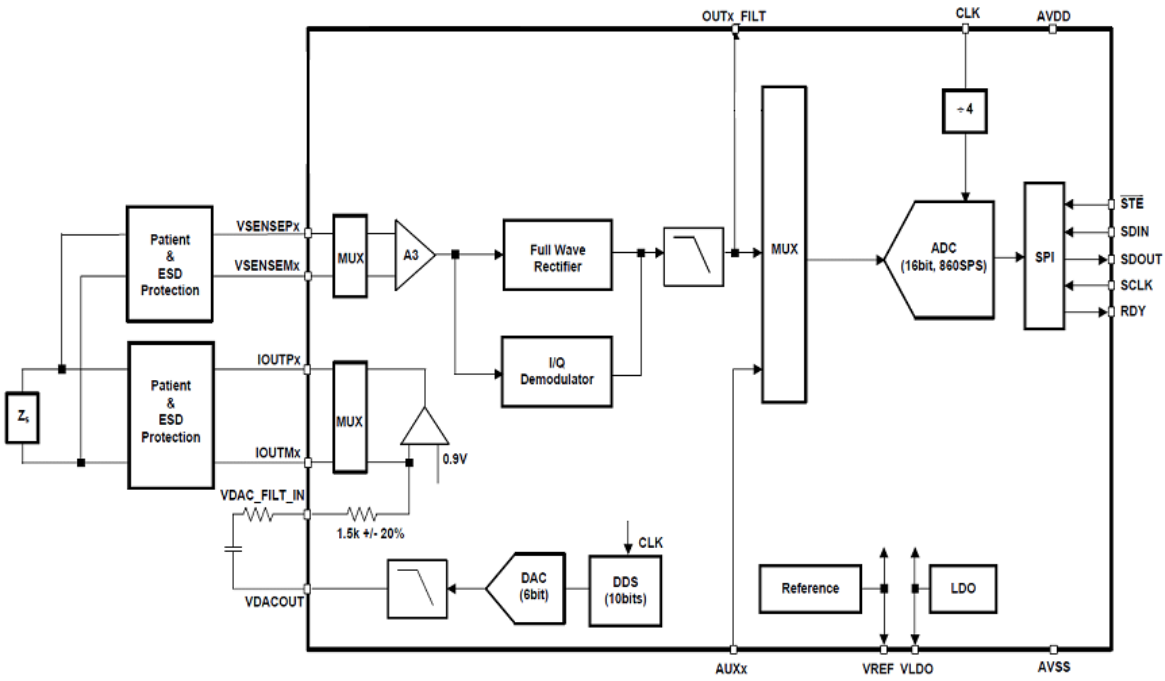
synchronized with the peaks of the carrier signal. The hardware also has an ECG extractor using 'TI/ADS1298' [35] to get the ECG signal from V1-V2. It has eight simultaneous sampling, 24-bit, sigma-delta ADCs with built-in programmable gain amplifiers (PGA). A microcontroller 'Microchip/dsPIC33' [32] is used for setting the frequency of the synthesizer, setting the V/I output by controlling 'Dig Pot 1', reading the measured impedance and ECG via a serial peripheral interface (SPI), baseline correction by monitoring the sensed impedance and controlling 'Dig Pot 2', and data transfer via Bluetooth. The measured time-varying impedance is sent wirelessly via Bluetooth to an external device like a PC for processing and visualization.

3.2 Impedance converter TI/AFE4300

The core of the proposed design is the impedance converter IC AFE4300 [33] from Texas Instruments. It is a four-electrode impedance measuring device that enables multiple impedance measurement configurations through its internal multiplexers. The device allows either a full-wave rectifier (FWR) or a synchronous in-phase and quadrature phase (I/Q) demodulator to perform a single frequency or multi-frequency impedance measurements over 1−150 kHz, by applying a sinusoidal current. The use of synchronous demodulation can provide output with higher SNR. The functional block diagram of the impedance converter IC is shown in Figure 3.3. In the excitation unit as shown in Figure 3.3 (a), an internal direct digital synthesizer (DDS) generates a sinusoidal digital pattern with a frequency obtained by dividing a clock of 1 MHz with a 10-bit counter. The digital pattern drives a 6-bit 1-MSPS DAC. The output of the DAC is filtered by a second order low-pass filter with 150 kHz cutoff frequency to remove high-frequency images, followed by a series external capacitor to block the dc current and avoid dc current injection [34]. The DDS frequency can be modified by the registers and can be swept in accordance with the set parameters. The DAC output is converted into current using inverting op amp amplifier with the load connected in the feedback. The output of the filter drives a resistor connected to inverting terminal of the single-ended V/I converter, setting the amplitude of the current. The nominal DAC output voltage is 1.05 $V_{PP,}$ and the nominal value of the resistor is 1.5 kΩ, resulting in excitation current of 247.5 μArms. With the maximum voltage swing at the excitation electrodes of 1 V_{PP}, the maximum impedance in the op amp feedback path is approximately 1175 Ω. The excitation current may be reduced by connecting an external resistor in series with the 1.5 kΩ between V_{DAC_OUT} and $V_{DAC\_FILT\_IN}$ for extending the range of the measured impedance. Current is output through an analog multiplexer that allows the selection of up to six different contact points (IOUT0−IOUT5). The same multiplexer allows the connection of two external impedances for calibration (RN1, RN0, RP1, RP0). There are two set of switches which can be programmed independently for



(a): Excitation and demodulation units in T1/AFE4300



(b): Impedance measurement using TI/AFE4300 [33]

Figure 3.3: Functional block diagram of Impedance converter IC TI/AFE4300 [33]: (a): Excitation and demodulation units in T1/AFE4300, (b) Impedance measurement using TI/AFE4300.

connecting the load impedance across any two points out of the points IOUT0−IOUT5. The first set of switches routes IOUTNx to the negative input of the V/I converter op amp and the second set of switches routes IOUTPx to the output of op amp closing the loop. The amplitude of the injected current $i(t)$ is given as

$$i(t) = (V_{max}/R)\sin(\omega_c t) \tag{3.1}$$

where V_{max} is the amplitude of the sinusoidal output at V_{DAC_OUT}, R is the series combination of 1.5 kΩ and the external resistor, and ω_c is the angular frequency of the excitation signal. The corresponding voltage drop across the impedance is measured by another pair of electrodes, followed by a differential amplifier of gain 2. A second set of multiplexers connects the differential amplifier across the load impedance. Similar to the selection of current injecting points, there are two set of switches which can be programmed independently that allows the connection of load impedance across any two points out of the points VSENSE0−VSENSE5. The first set of switches routes VSENSENx to the negative input of the differential amplifier and the second set of switches routes VSENSEPx to the positive input of the differential amplifier. The same set of switches allows the connection of two calibration resistors across VSENSERP1, VSENSERP0, VSENSERN1, and VSENSERN0. The voltage signal $V(t)$ measured across the VSENSE terminals is given as

$$v(t) = A|Z|\sin(\omega_c t + \theta) \tag{3.2}$$

where Z and θ are the magnitude and phase of the impedance, respectively, and A is the amplitude of the excitation current, given as

$$A = (V_{max}/R) \tag{3.3}$$

In the impedance measuring IC, the impedance can be measured from the amplitude modulated signal using two modes: the full-wave rectifier (FWR) mode and the I/Q mode. In the FWR mode, a full-wave rectification is performed on the differential amplifier output followed by low-pass filtering. The detected envelope, corresponding to the time-varying impedance, is routed to the 16-bit sigma-delta ADC which operates at a modulation frequency of 250 kHz with an f_{CLK} of 1 MHz. The decimation rate of the single order sinc filter can be programmed to provide data rates from 8 to 860 samples/s. The internally generated reference signal of 1.7 V is used for the conversion. The output format of the ADC is 2's complement binary. The FWR output is proportional to the magnitude of impedance, and the proportionality factor can be obtained through calibration with two external impedances.

$$V_{DC} = \frac{2}{T}\int A|Z|\sin(\omega_c t + \theta)\,dt = \frac{2A|Z|}{\pi}\cos\theta \tag{3.4}$$

For obtaining both the real and imaginary parts of the impedance using this mode, two different frequency measurements have to be done. The I/Q mode uses in-phase and quadrature-phase

synchronous demodulation to get the real and imaginary components of the impedance. It can be used to compute both the magnitude and the phase with a single frequency measurement.

The circuit for current injection is the same for both the impedance measurement modes, and the difference between them is only in the demodulation technique. The I/Q demodulator has $v(t)$ as the input signal and outputs two dc values (I_{DC} and Q_{DC}). The local oscillator (LO) signals for the mixers are generated from the same clock driving DDS/DAC and are of the same phase and frequency as the sinusoidal $i(t)$. The LO signals control the switches on the in-phase (I) path directly, and control the switches on the quadrature (Q) path with 90° phase shift. This type of switching using analog switches is equivalent to multiplying the sensed signal v(t) by a square wave signal swinging from -1 to +1. The square wave can be expanded using Fourier series and can be expressed as,

$$v_{LO}(t) = \frac{4}{\pi}(\sin(w_o t) + \frac{1}{3}\sin(3w_o t) + \frac{1}{5}\sin(5w_o t)....) \tag{3.5}$$

The voltage at the output of the I-path is given as,

$$v_{OI}(t) = A|Z|\frac{4}{\pi}(\sin(w_o t+\theta)\sin w_o t + \frac{1}{3}\sin(3w_o t)\sin(w_o t+\theta) + \frac{1}{5}\sin(5w_o t)\sin(w_o t+\theta)+...) \tag{3.6}$$

Similarly, the voltage at the output of the Q-path can be written as,

$$v_{OQ}(t) = A|Z|\frac{4}{\pi}(\sin(w_o t+\theta)\cos w_o t + \frac{1}{3}\cos(3w_o t)\sin(w_o t+\theta) + \frac{1}{5}\cos(5w_o t)\sin(w_o t+\theta)+..) \tag{3.7}$$

The following trigonometric expansions can be used for expanding $v_{OI}(t)$ and $v_{OQ}(t)$

$$\sin(w_o t+\theta)\sin w_o t = -\frac{1}{2}\cos(2w_o t+\theta) + \frac{1}{2}\cos\theta \tag{3.8}$$

$$\sin(w_o t+\theta)\cos w_o t = \frac{1}{2}\sin(2w_o t+\theta) + \frac{1}{2}\sin\theta \tag{3.9}$$

After low-pass filtering, all the terms beyond the cutoff frequency of the low-pass filter at the output of the mixers are removed. Hence,

$$V_{IDC} = \frac{2A|Z|}{\pi}\cos\theta \tag{3.10}$$

$$V_{QDC} = \frac{2A|Z|}{\pi}\sin\theta \tag{3.11}$$

From V_{IDC} and V_{QDC} the impedance magnitude |Z| and phase θ can be calculated as,

$$\theta = \arctan\frac{V_{QDC}}{V_{IDC}} \tag{3.12}$$

$$|Z| = \frac{1}{K}\sqrt{{V_{IDC}}^2 + {V_{QDC}}^2} \tag{3.13}$$

For computing the value of *K*, a two-point calibration has to be carried out, to account for the nonidealities in the system. Both V_{IDC} and V_{QDC} can be applied to 16-bit, sigma-delta ADC either differentially or single-ended (with respect to ground) using a multiplexer.

The IC AFE4300 operates from 2 V to 3.6 V with a maximum supply current of 20 mA. It is clocked by an external oscillator of frequency 1 MHz. It has an SPI interface, consisting of four signals, STE, SCLK, SDIN, and SDOUT. This interface is reading the conversion data, read/write register data, and thus controls the AFE4300 operation. The STE (chip select) pin selects the impedance converter IC for SPI communication and it is useful when multiple devices are sharing the same SPI bus. The SCLK pin is used to provide the clock from the master device. The SDIN pin is used along with SCLK to send the opcode commands and register data to the chip. The SDOUT pin along with the SCLK is used to read the conversion and register data from the chip. In addition to the SPI pins, the chip has the RDY pin, which indicates conversion ready in both the continuous-conversion and single-shot modes, going low for 8 μs at the end of each conversion. The data packet between the falling edge and the rising edge of the chip select pin is 24-bit long and it is serially shifted into the SDIN with the MSB first. The first 8 bits [23:16] represent the address of the register, and the last 16 bits [15:0] represent the data to be stored or read from that address. In the 8-bit address MSB part, the lower five bits [20:16] are the real address bits. The bit 21 is '0' for write operation and '1' for read operation of the register defined by the address. During read operation, the register data are output into SDOUT at the rising edge of SCLK, starting at the ninth rising edge.

3.3 Thoracic impedance measurement using AFE4300

The pin connections of the impedance converter chip AFE4300, labeled as U1, are shown in Figure 3.4. It is controlled by the 16-bit digital signal controller IC dsPIC33FJ128GP802 (Microchip) [32], labeled as U8, via serial communication. The microcontroller has two SPI modules which can support either 8-bit or 16-bit data and it acts a master device. The SCLK, SDIN, SDOUT, and STE of the AFE4300 are connected to the microcontroller pins RP13, RP12, RP15, and RB14 respectively. The microcontroller pins RP13, RP12, and RP15 are mapped to the clock input, data output, and data input, respectively of SPI-1. The input clock f_{clk} to the impedance converter U1 is generated by the microcontroller peripheral pin RP6 which is mapped to the output compare module. The RP6 pin toggles when the Timer-2 value matches the compare register value. The frequency of the current excitation is kept in the 20−100 kHz range. The frequency of the DDS is

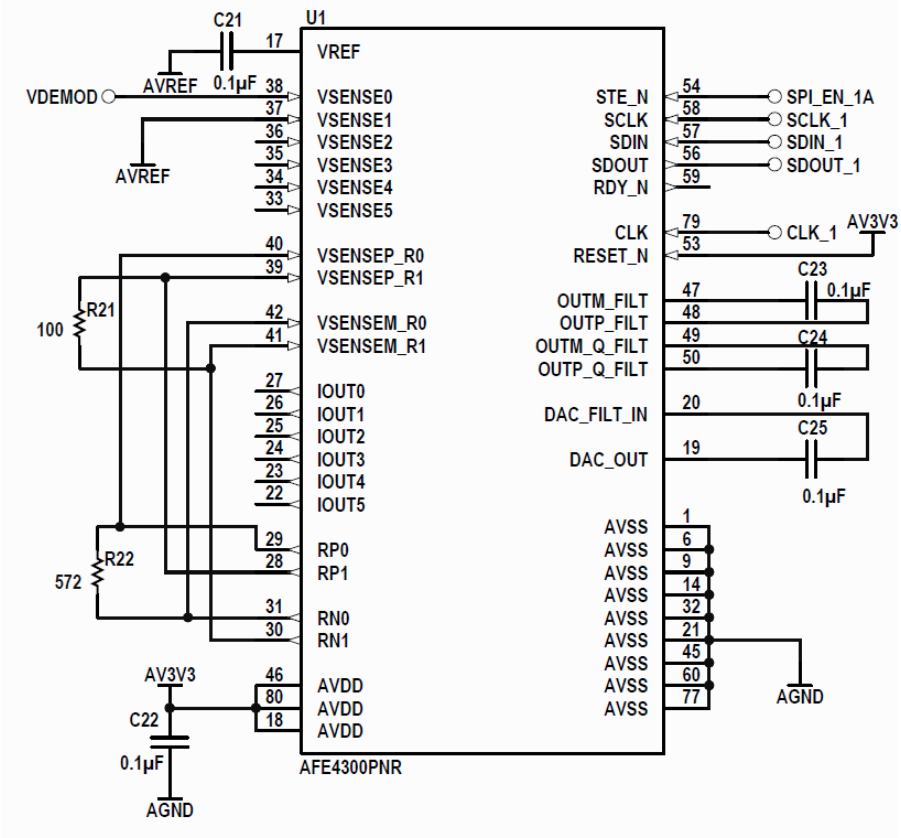


Figure. 3.4: Impedance converter IC AFE4300 connections

programmed via a 24-bit word loaded serially over the SPI-1 interface to the BCM_DAC_FREQ register. The DAC output frequency is given by

$$f_{out} = N_{freq}(f_{clk} \ / \ 1024) \tag{3.14}$$

where f_{clk} is the frequency of the device input clock, and N_{freq} is the value written in the BCM_DAC_FREQ register. The DAC frequency can be set to any value in the FWR mode. Only certain DAC BCM_DAC_FREQ frequencies which satisfy the following condition can be used for generating the phases for the mixers:

$$\begin{aligned} \text{IQ\_DEMOD\_CLK} &= f_{clk} \ / \left(\text{IQ\_DEMOD\_CLK\_DIV\_FAC}\right) \\ &= 4(\text{BCM\_DAC\_FREQ}) \end{aligned} \tag{3.15}$$

where IQ_DEMOD_CLK is the I/Q demodulator clock frequency which is internally generated from the device input clock $f_{clk.}$ It limits the frequency of operation to 8, 16, 32, 64, and 128 kHz.

Two reference resistors, Rx of 572 Ω and Ry of 100 Ω, are needed to perform magnitude and phase calibration [34] in both FWR and IQ modes. The converted voltage from the device is linear to the magnitude and is given as,

$$\text{Magnitude} = m'v + o \tag{3.16}$$

where m' is the slope, o is the offset, and v is the ADC code corresponding to the resistance. The resistances of the reference resistors Rx and Ry are measured using a multimeter. The following steps need to be taken to perform the measurement in the FWR mode:

1. Read the ADC codes R_x_ADC and R_y_ADC, corresponding to the resistors Rx and Ry, respectively, from the AFE4300 after setting the frequency and ADC sampling rate to the desired value.
2. Calculate the slope $m' = (R_x - R_y) / (R_x\_ADC - R_y\_ADC)$.
3. Calculate the offset $o = R_x - (R_x\_ADC)$.
4. Read the ADC code of unknown impedance Z_ADC and hence the magnitude $|Z|$ corresponding to the ADC code = $(m'Z\_ADC) + o$.

From the ADC codes of the IQ mode, the magnitude and phase can be calculated as the following,

$$\text{Magnitude} = \sqrt{V_{IDC}^{\ 2} + V_{QDC}^{\ 2}} \tag{3.17}$$

$$\text{Phase} = \tan^{-1}\frac{V_{QDC}}{V_{IDC}} \tag{3.18}$$

The magnitude is calibrated using a two-point calibration method using the same reference resistors Rx and Ry. The slope and offset are calculated once before the impedance measurement. The phase is compensated by subtracting the phase of the reference resistor from the phase of the measured impedance. The estimation of the phase of the reference resistor has to be done before each impedance measurement. The steps to perform the impedance measurement in the IQ mode are as the following.

1. Read the I and Q codes from the ADC for the resistors Rx and Ry from the AFE4300 after setting the frequency and ADC sampling rate to the desired value. Calculate the magnitude codes R_x_Mag_ADC and R_y_Mag_ADC for Rx and Ry, respectively, using Equation 3.17.
2. Calculate the slope $m' = (R_x - R_y) / (R_x\_Mag\_ADC - R_y\_Mag\_ADC)$.
3. Calculate the offset $o = R_x - (m' R_x\_Mag\_ADC)$.
4. Read the I and Q codes from the ADC for the unknown impedance Z and calculate its magnitude code Z_Mag_ADC using (3.17). The magnitude $|Z|$ corresponding to the ADC code is calculated as $|Z| = (m'Z\_Mag\_ADC) + o$.
5. Measure the I and Q codes from the ADC for Rx and calculate the phase using (3.18).
6. Calculate the phase of the unknown impedance using the I and Q values, and compensate the phase by subtracting the phase for the reference resistor Rx.

The steps 5 and 6 have to be repeated every time for each sample network. In Figure 3.4, the calibration resistor Rx is connected across IOUTRN1 and IOUTRP1, with IOUT RN1 connected to

the negative terminal of the op amp and IOUTRP1connected to the output of the op amp. Similarly, the calibration resistor Ry is connected across IOUTRN0 and IOUTRP0.

3.4 Need for additional analog circuits

The output excitation voltage of the DAC in the impedance converter IC is converted into current using a single-ended V/I converter (inverting op amp amplifier with the load connected in the feedback). It results in one of the electrodes at virtual ground. Hence the terminal voltages are imbalanced with respect to the ground, which may lead to common mode pickup and stray currents. Also, the stray capacitance on the virtual ground terminals may lead to instability. This problem can be solved by using a voltage-controlled balanced current source.

The second challenge is to develop an impedance cardiograph by providing baseline correction over a large range of the basal impedance, to avoid the saturation of analog processing circuits. The variable component of the thoracic impedance is usually 0.1−2% of the basal component. For sensing this component, we need to improve the resolution of the impedance converter chip. This is accomplished by incorporating a baseline correction amplifier before giving the sensed voltage to the demodulator as the impedance converter.

In the demodulation path of the IC AFE4300, the voltage waveform across the thorax is given to a difference amplifier of fixed gain. For sensing the differential voltage developed across the voltage electrode pair, an instrumentation amplifier configuration along with a common-mode negative feedback is used for enhanced CMRR. The circuit is designed for measuring the differential voltage signal with high common mode signal and avoiding saturation of the internal difference amplifier in the first stage. Hence for using AFE4300 in the impedance cardiograph, the devised additional blocks includes a balanced V/I converter, a voltage sensing amplifier with common-mode feedback, baseline correction arrangement, and digital potentiometers for independent control of the amplitude of the excitation current and the baseline correction signal.

3.5 Balanced current source with amplitude control

The current source should have high output impedance so that the tissue-electrode and thoracic impedance do not affect the excitation current. Also, it should be insensitive to common mode pick-ups, stray currents, and stray capacitances. An op amp based voltage-controlled balanced current source is proposed for providing the excitation current. This circuit is intended to eliminate the need for a transformer to get a balanced current.

The circuit is realized using a fully differential amplifier (differential input, differential output amplifier), also known as bridge-tied load (BTL) amplifier. The two outputs of a BTL

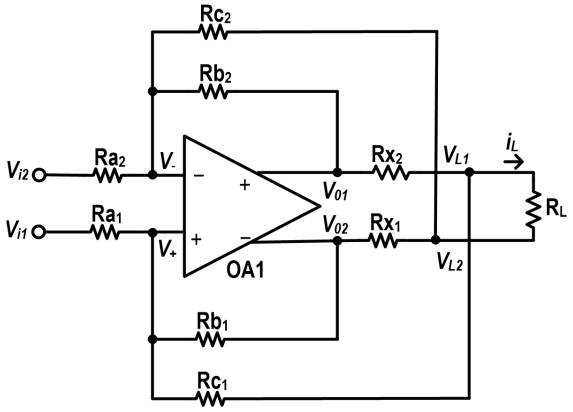


Figure 3.5: Balanced V/I converter using a BTL amplifier

circuit are 180° out of phase, thereby doubling the output voltage swing as compared to the single-ended output. The circuit of the balanced V/I converter is shown in Figure 3.5, with the BTL amplifier as OA1, the resistors Ra1, Ra2, Rb1, Rb2, Rc1, Rc2, Rx1, and Rx2, the input voltages v_{i1} and v_{i2} , and the load terminal voltages as v_{L1} and v_{L2}. The amplifier has the differential input terminals v_+ and v_- and the differential output terminals v_{01} and v_{02}. The output voltages are symmetric with respect to a common-mode output v_{oc}, given as

$$v_{01} - v_{oc} = v_{oc} - v_{02} \tag{3.19}$$

By applying KCL at the input terminals of OA1, we get

$$\frac{v_{i1} - v_+}{R_{a1}} + \frac{v_{02} - v_+}{R_{b1}} + \frac{v_{L1} - v_+}{R_{c1}} = 0 \tag{3.20}$$

$$\frac{v_{i2} - v_-}{R_{a2}} + \frac{v_{01} - v_-}{R_{b2}} + \frac{v_{L2} - v_-}{R_{c2}} = 0 \tag{3.21}$$

Let $R_{a1} = R_{a2} = R_a$, $R_{b1} = R_{b2} = R_b$, $R_{c1} = R_{c2} = R_c$, $R_{x1} = R_{x2} = R_x$. With these resistances, the above two equations can be simplified as the following:

$$v_+(1 + \frac{R_a}{R_b} + \frac{R_a}{R_c}) = v_{i1} + v_{02}\frac{R_a}{R_b} + v_{L1}\frac{R_a}{R_c} \tag{3.22}$$

$$v_-(1 + \frac{R_a}{R_b} + \frac{R_a}{R_c}) = v_{i2} + v_{01}\frac{R_a}{R_b} + v_{L2}\frac{R_a}{R_c} \tag{3.23}$$

Applying the virtual short property across the input terminals of the op amp operating in the linear region, we get $v_- = v_+$ .Therefore, (3.22) and (3.23) result in

$$v_{01} - v_{02} = (R_b / R_a)(v_{i1} - v_{i2}) + (R_b / R_c)(v_{L1} - v_{L2}) \tag{3.24}$$

By applying KCL at the load resistance terminal v_{L1}, we get

$$i_L = (v_{01} - v_{L1}) / Rx_2 + (v_+ - v_{L1}) / Rc_1 \tag{3.25}$$

Applying it at the load resistance terminal v_{L2}, we get

$$-i_L = (v_{02} - v_{L2}) / Rx_1 + (v_- - v_{L2}) / Rc_2 \tag{3.26}$$

The above two equations can be written as the following:

$$i_L = (v_{01} - v_{L1}) / R_x + (v_+ - v_{L1}) / R_c \tag{3.27}$$

$$-i_L = (v_{02} - v_{L2}) / R_x + (v_- - v_{L2}) / R_c \tag{3.28}$$

Subtracting (3.28) from (3.27), we get

$$2i_L = (v_{01} - v_{02}) / R_x - (v_{L1} - v_{L2})(1 / R_x + 1 / R_c) \tag{3.29}$$

Substituting the expression for $(v_{01} - v_{02})$ from (3.24) into (3.29), we get

$$2i_L = \left[(R_b / R_c)(v_{L1} - v_{L2}) + (R_b / R_a)(v_{i1} - v_{i2})\right] / R_x - (v_{L1} - v_{L2})(1 / R_x + 1 / R_c)$$

which can be simplified as

$$2i_L = (R_b / R_a)(v_{i1} - v_{i2}) / R_x + (R_b / R_c - 1 - R_x / R_c)(v_{L1} - v_{L2}) / R_x \tag{3.30}$$

The load current as given by (3.30) is independent of the voltages across the load resistance v_{L1} and v_{L2}, if the following condition is satisfied:

$$R_b / R_c - 1 - R_x / R_c = 0 \tag{3.31}$$

This condition can also be expressed as

$$R_x = R_b - R_c \tag{3.32}$$

The load current under this condition is given as

$$i_L = (R_b / R_a)\left(v_{i1} - v_{i2}\right) / (2R_x) \tag{3.33}$$

It may be noted that with $R_x << R_b$, (3.32) leads to $R_b \approx R_c$. Alternatively, unity followers for can be used connecting v_{L1} and v_{L2} to Rc1 and Rc2, respectively, also results in $R_b = R_c$.

The balanced V/I converter circuit of Figure 3.5 is used for providing the current excitation for impedance measurement. The sinusoidal voltage generated by the DAC output of U1 is given as input to the V/I converter and as a baseline correction signal to the baseline correction amplifier as shown in Figure 3.6. The output current is directly proportional to the amplitude of the DAC output voltage. The baseline component in the sensed voltage is proportional to the amplitude of the baseline correction signal. Hence two digital potentiometer ICs AD8400 [37] are used as U2 and U3 for independent control of the amplitude of the excitation current and the baseline correction signal, respectively. The digital potentiometer IC AD8400 operates with a supply voltage of 2.7−5.5 V and has a total resistance of 10 kΩ with 256 steps and a wiper resistance of 50 Ω. The wiper position is controlled through the SPI interface. Both digital potentiometers are interfaced to the second SPI module of the microcontroller. The op amps U5C and U5D are used as buffers with

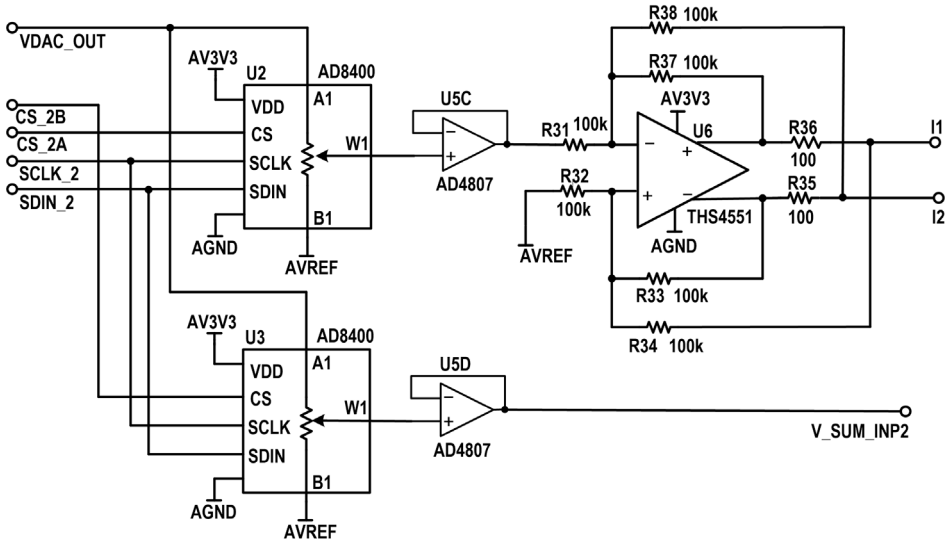


Figure 3.6: Amplitude control using digital potentiometers and op amp based balanced current source.

the outputs of U2 and U3 as their inputs, respectively. The output of the digital potentiometer U2 is connected to one of the inputs of the balanced V/I converter realized using U6, and the other input [36], which is a differential-input differential-output amplifier with the supply of 2.7−5.4 V. In our circuit, all the ICs are powered with 3.3 V. An analog reference AVREF at 1.6 V with respect to AGND is used to bias the signals within the permitted signal swing at the input and output terminals. The resistors R32, R31, R33, R37, R34, R38, R36 and R35 in Figure 3.6 correspond to the resistors Ra1, Ra2, Rb1, Rb2, Rc1, Rc2, Rx1 and Rx2, respectively, in Figure 3.5. Here we select $R_{32} = R_{31} = R_{33} = R_{37} = R_{32} = R_{34} = R_{38} = 100$ kΩ. With $R_{36} = R_{35} = R_x$, the maximum value of R_x is given as

$$|v_{o1} - v_{o2}|_{\max} \geq (2R_x + (R_L)_{\max})\,|i_L|_{\max} \tag{3.34}$$

which can be rewritten as

$$R_x \leq \left[|v_{o1} - v_{o2}|_{\max} / |i_L|_{\max} - (R_L)_{\max}\right] / 2 \tag{3.35}$$

The voltage swing at either output of U6 is 0−3.3 V and therefore $|v_{o1} - v_{o2}|_{\max} = 3.3$ V. With $|i_L|_{\max} = 2.5$ mA and $(R_L)_{\max}$ = 500 Ω, we get $R_x \leq 410\ \Omega$. The resistance value R_x is kept as terminal is connected to the reference voltage. The IC used as the BTL amplifier U6 is THS4551 100 Ω to achieve large output voltage swing across the load resistance R_L. Thus we have $R_a = R_b = R_c$ and $R_x << R_a$. The current i_L, is given as

$$i_L = (v_{i1} - v_{i2}) / (2R_x) \tag{3.36}$$

Thus the excitation current is proportional to $(v_{i1} - v_{i2})$. With R_x=100 Ω, v_{i2} = 1.6 V and $|v_{i1} - v_{i2}|_{\max} < 1.6$ V, we have $|i_L|_{\max} < 9$ mA, which is within the safe limits of current excitation.

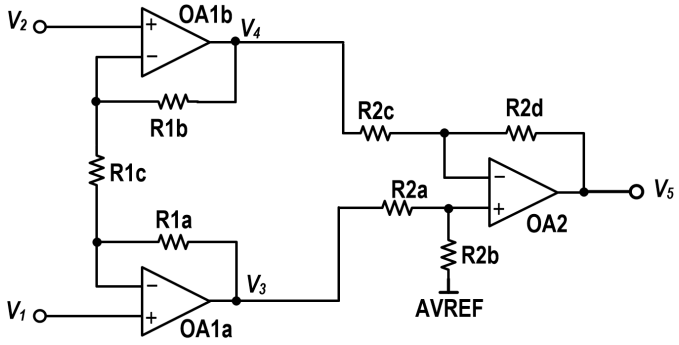


Figure 3.7: Two-stage instrumentation amplifier

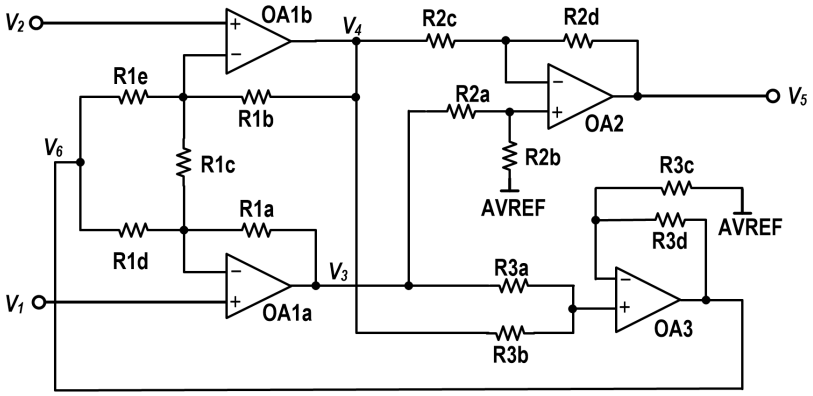


Figure 3.8: Voltage sensing amplifier with common-mode feedback

3.6 Voltage sensing amplifier with improved CMRR

A differential amplifier has finite CMRR due to tolerance of the matched resistances and finite CMRR of the op amp used for realizing the differential amplifier. The CMRR degrades at higher frequencies. For a high CMRR differential amplifier with high input impedance, we generally use the two-stage instrumentation amplifier circuit as shown in Figure 3.7, with the resistances related as $R_{2a} = R_{2c} = R$, $R_{2d} = R_{2b} = \alpha R$, $R_{1a} = R_{1b} = R'$, $R_{1c} = R'/\beta$. The op amps OA1a and OA1b form the first stage, and OA2 forms the second stage. The differential mode and common-mode gain of the first and second stages are given as

$$A_{d1} = (v_3 - v_4)/(v_1 - v_2) = 2\beta + 1 \tag{3.37}$$

$$A_{c1} = ((v_3 + v_4)/2)/((v_1 + v_2)/2) = 1 \tag{3.38}$$

$$A_{d2} = v_5/(v_3 - v_4) = \alpha \tag{3.39}$$

$$A_{c2} = v_5/((v_3 + v_4)/2) \tag{3.40}$$

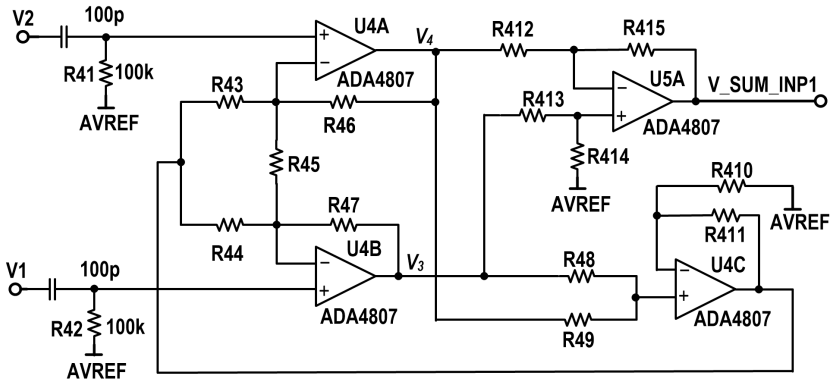


Figure 3.9: Voltage sensing amplifier

With perfectly matched resistances, and infinite CMRR of OA2, the common-mode gain of the second stage is zero. Mismatch of the resistance ratios R_{2d}/R_{2c} and R_{2b}/R_{2a} and also the finite CMRR of OA2 result in a finite value of A_{c2}. As the op amp CMRR decreases with frequency, A_{c2} increases with frequency. The first stage of the circuit provides a differential gain of $2\beta+1$ and common-mode gain of 1 and thus improves the CMRR by a factor of $2\beta+1$. The overall CMRR is given as

$$\text{CMRR} = \frac{A_{d1}A_{d2}}{A_{c1}A_{c2}} = \frac{\alpha}{A_{c2}}(2\beta+1) \tag{3.41}$$

For providing an improved CMRR, we use a circuit with a feedback of the common-mode output to the midpoint of the inputs. The circuit is shown in Figure 3.8. The op amps OA1a and OA1b are used for the first stage of the instrumentation amplifier, and the op amp OA2 is used for the second stage. The op amp OA3 with the output v_6 is used for common-mode feedback. Assuming virtual short across the op amp input terminals of OA1a and OA1b, and applying KCL at the inverting terminals, we get

$$\frac{v_6 - v_1}{R_{1d}} + \frac{v_2 - v_1}{R_{1c}} + \frac{v_3 - v_1}{R_{1a}} = 0 \tag{3.42}$$

$$\frac{v_6 - v_2}{R_{1e}} + \frac{v_1 - v_2}{R_{1c}} + \frac{v_4 - v_2}{R_{1b}} = 0 \tag{3.43}$$

Let us assume $R_{2a} = R_{2c} = R$ and $R_{2d} = R_{2b} = \alpha R$ for the resistors of the second stage, $R_{1a} = R_{1b} = R_{1e} = R_{1d} = R'$ and $R_{1c} = R'/\beta$ for the resistors of the first stage. With these resistances, (3.42) and (3.43) can be written as

$$v_3 = (2+\beta)v_1 - v_6 - \beta v_2 \tag{3.44}$$

$$v_4 = (2+\beta)v_2 - v_6 - \beta v_1 \tag{3.45}$$

From (3.44) and (3.45), we get

$$(v_3 + v_4)/2 = v_1 + v_2 - v_6 \tag{3.46}$$

The common-mode feedback amplifier using OA3 is a non-inverting amplifier. With the output $R_{3a} = R_{3b}$, the output is given as

$$v_6 = (1 + R_{3d}/R_{3c})(v_3 + v_4)/2 \tag{3.47}$$

With $R_{3d} = \gamma R_{3c}$, (3.47) can be written as

$$v_6 = (1 + \gamma)(v_3 + v_4)/2 \tag{3.48}$$

From (3.46) and (3.48), we get

$$\frac{v_3 + v_4}{2} = \frac{v_1 + v_2}{2}\frac{1}{1 + \gamma/2} \tag{3.49}$$

The above equation shows that common mode voltage at the output of the first stage gets attenuated. For maximum attenuation, we can use $\gamma \to \infty$, i.e. $R_{3c} \to 0$ and $R_{3d} \to \infty$. However, we use a finite gain due to stability considerations.

The differential voltage after the first stage is obtained by taking the difference of (3.44) and (3.45) as the following:

$$v_3 - v_4 = 2(\beta + 1)(v_1 - v_2) \tag{3.50}$$

Hence, the differential gain of the amplifier is given as

$$A_d = 2\alpha(\beta + 1) \tag{3.51}$$

where α is the gain of the second stage formed using OA2. The common-mode gain of the amplifier is

$$A_c = A_{c2}/(1 + \gamma/2) \tag{3.52}$$

where A_{c2} is the common-mode gain of the second amplifier. The CMRR of the amplifier is given as

$$\frac{A_d}{A_c} = (\alpha/A_{c2})(2\beta + 2)(1 + \gamma/2) \tag{3.53}$$

It the above, the first term is the CMRR of the second stage, the second term is due to the first stage, and the third term is due to the common-mode feedback. As the common-mode signal at the outputs, v_3 and v_4, is reduced significantly because of the feedback to the input of the first stage, the overall CMRR improves to a large extent.

The voltage across the electrode pair V1-V2 is amplified using the amplifier configuration of Figure 3.8, and the circuit is shown in Figure 3.9. The op amps U4A, U4B, and U5A form the two-stage instrumentation amplifier, and U4C is used for common-mode feedback. The IC used is ADA4807 [39], rail-to-rail input and output quad op amps. The circuit works with a single supply

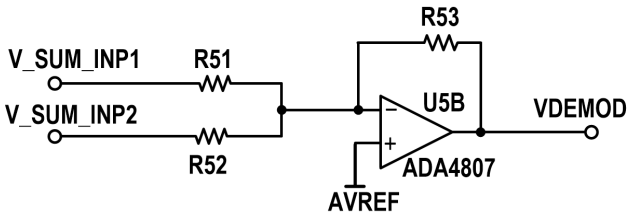


Figure 3.10: Summing amplifier for baseline correction

of 3.3 V and an analog reference of 1.6 V. The resistors R43, R44, R46, R47, R45, R412, R413, R415, R414, R48, R49, R410 and R411 in Figure 3.9 correspond to the resistors R1e , R1d , R1b, R1a, R2c, R2a, R2d, R2b, R3a, R3b, R3c and R3d, respectively in Figure 3.8. The resistance values are selected as $R_{43} = R_{44} = R_{46} = R_{47} = 10$ kΩ, $R_{45} = 3.3$ kΩ, $R_{412} = R_{413} = R_{415} = R_{414} = 10$ kΩ, $R_{48} = R_{49} = 10$ kΩ, $R_{410} = 1$ kΩ, and $R_{411} = 100$ kΩ, resulting in α = 1, β = 3 and γ = 100. It results in the differential gain as A_d = 8 and the CMRR improvement factor, $(2\beta + 2)(1 + (\gamma / 2)$, as 408. The high-pass filters at the front end, formed with R41, R42, C41, and C42 help in rejecting low-frequency noise and other bio-electric signals without affecting the voltage related to the excitation current. The cutoff frequency of the filter is given as

$$f_c = 1/(2\pi RC) \tag{3.54}$$

where $R_{42} = R_{41} = R$, $C_{42} = C_{41} = C$. We use R = 100 kΩ and C = 100 pF, resulting in $f_c \approx 16$ kHz.

The output of the difference amplifier U5A is given as one of the inputs to the baseline correction block. Depending upon the range of the measured impedance, the value of excitation current is adjusted using the digital potentiometer U2 so that the output of differential op amp U5A does not go into saturation.

3.7 Tracking based baseline correction

The baseline of the bio-impedance signals like ICG can have a large drift due to breathing, electrode placement, and offset drift in the analog signal conditioning circuits, body movement, and other motion artifacts. This drift can lead to a reduction in the input dynamic range of the data acquisition circuit. The tracking-based dynamic correction of the baseline wandering method is the effective and fast technique as it ensures that the sensed voltage is within the ADC input range.

Instead of using baseline correction after the demodulation, Mishra [24] proposed a method in which a voltage proportional to the sinusoidal carrier signal is used as a correction signal (V_{bc}) before demodulation. The amplitude of the correction signal can be controlled independently using the digital potentiometer U3. The demodulated output is continuously monitored. If the sensed voltage goes out of the predefined thresholds, the digital potentiometer is modified to bring the

output within the thresholds so that the demodulator does not saturate and the time-varying signal is not too low. We use the same approach in our circuit. An inverting summing amplifier, realized using U5B, is used as a baseline correction amplifier. It adds the output of voltage sensing amplifier U5A and the output of the digital potentiometer U3, as shown in Figure 3.10. The output the summing amplifier is sampled by the ADC of the microcontroller and compared with the upper threshold and lower threshold. If the output of the summing amplifier crosses the upper threshold, the value of the baseline correction signal has to be increased by one step, and if the output goes below the lower threshold, the correction signal amplitude is decreased by one step.

In the circuit of Figure 3.10, let R_{51}= α_1 R_{53} and R_{52}= β_1 R_{53}. The output of the summing amplifier V_{DEMOD}, is given as

$$V_{DEMOD} = -\alpha_1 V_{SUM\_INP1} - \beta_1 V_{SUM\_INP2} \tag{3.55}$$

The output of the voltage sensing amplifier V_{SUM_INP1}, can be expressed as

$$V_{SUM\_INP1} = 2\alpha(\beta+1) i_L Z \tag{3.56}$$

The input to the digital potentiometer U2 and U3 is the sinusoidal carrier output voltage of DAC, V_{DAC_OUT} . Let α_2 be the resistance ratio of the digital potentiometer U2, which is used to vary amplitude of the current excitation. Therefore, the load current i_L in (3.56) is given as

$$i_L = (1/2R_x) V_{DAC\_OUT} \alpha_2 \tag{3.57}$$

The output of U3 forms the correction signal V_{SUM_INP2}, which is given as

$$V_{SUM\_INP2} = V_{DAC\_OUT} \beta_2 \tag{3.58}$$

where β_2 is the resistance ratio of the digital potentiometer U3, which is used to vary the baseline correction signal. Therefore, the output voltage of the summing amplifier (3.55) can be written as

$$V_{DEMOD} = -\alpha_1 2\alpha(\beta+1)(1/2R_x) V_{DAC\_OUT} \alpha_2 Z - \beta_1 V_{DAC\_OUT} \beta_2 \tag{3.59}$$

Let α_1 = β_1 = 1. Replacing the gain of voltage controlled balanced current source and voltage sensing amplifier by constant *K*, (3.59) can be rewritten as

$$V_{DEMOD} = -K V_{DAC\_OUT} Z - V_{DAC\_OUT} \beta_2 \tag{3.60}$$

where $K = 2\alpha(\beta+1)(1/2R_x)\alpha_2$ (3.61)

The thoracic impedance, *Z* can be expressed as the sum of basal component Z_0 and time-varying component $z(t)$ as given below

$$Z = Z_0 + z(t) \tag{3.62}$$

By replacing *Z* by (3.62) in (3.60)

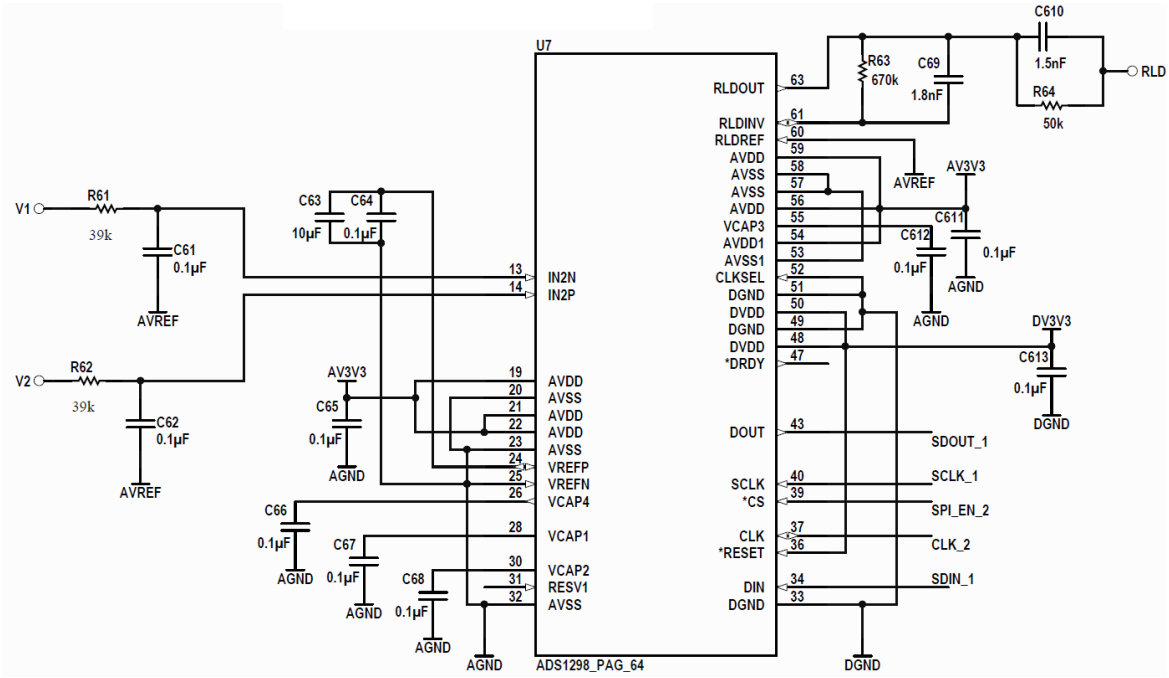


Figure 3.11: ECG extractor using ADS1298 connections

$$V_{DEMOD} = -V_{DAC\_OUT} K(Z_0 + z(t) - \beta_2 / K) \tag{3.63}$$

The resulting output of the summing amplifier, V_{DEMOD} is directly proportional to the difference between thoracic impedance to be measured Z, and the reference impedance β_2 / K. The baseline correction amplifier output is then given as input to the I/Q demodulator of the impedance converter chip TI/AFE4300, to improve the resolution of the impedance measurement.

3.8 ECG extractor using ADS1298

The ECG extractor is used to extract the ECG from the signal sensed by the voltage-sensing electrodes. The R peaks of the ECG waveform are used as a reference in impedance cardiography. The ECG measurement of the system is performed using the IC TI/ADS1298 [35]. It has a set of 8 simultaneous sampling, 24-bit, sigma-delta ADCs with built-in programmable gain amplifiers (PGA), with a programmable sampling frequency of 250 Hz to 32 kHz. The low-pass filter, with a 3-dB cutoff frequency of 40 Hz, at the input of the ECG extractor IC rejects the high-frequency carrier of the impedance measuring circuit. The common mode rejection can be further improved by sensing the input common-mode voltage at the programmable gain amplifier (PGA) outputs and amplifying the difference using the right-leg drive (RLD) amplifier available in the chip and using the output to drive a fifth electrode connected as the right leg electrode. The chip

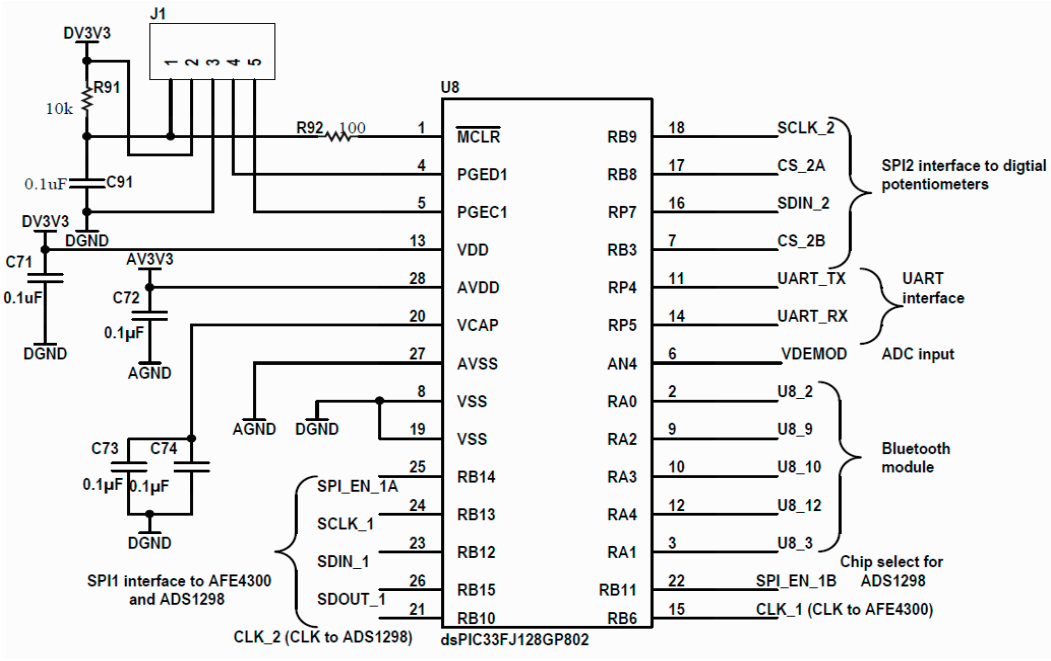


Figure 3.12: Microcontroller circuit

operates with a digital supply of 1.65−3.6 V and a separate analog supply of 2.7−5.25 V. It operates frequency of 2 MHz, which is generated by the microcontroller pin RP10. The SPI-compatible serial interface consists of four signals: CS, SCLK, SDIN, and SDOUT. The SCLK, SDIN, SDOUT, and CS of the ADS1298 are connected to the microcontroller pins RP13, RP12, RP15 and RB11 respectively. The connections for the ECG extractor IC is shown in Figure 3.12.

3.9 Microcontroller

The 16-bit microcontroller Microchip dsPIC33FJ128GP802 [32] is used for generation of the control signals for the impedance converter TI/AFE4300 IC, ECG extractor TI/ADS1298 IC and the digital potentiometers, performing the baseline correction algorithm, reading out the demodulated impedance and ECG via a serial peripheral interface (SPI). It has a supply of 3.0−3.6 V with a maximum current drain of 4 mA, with separate analog and digital supplies. The internal fast RC oscillator with a nominal clock of 7.37 MHz and an internal PLL for scaling the operating frequency to higher values is used to set the device clock frequency FCLK as 80 MHz. The connections are shown in Figure 3.12, with the microcontroller as U8. To stabilize the output voltage of the on-chip voltage regulator capacitors C73 and C74 are connected in parallel at VCAP pin. The $\overline{\text{MCLR}}$ pin of U8 is connected to the pin 1 of the connector J1 for resetting U8 with logic 0, and for programming and debugging using R91 and C91 with logic 1. C91 is discharged using

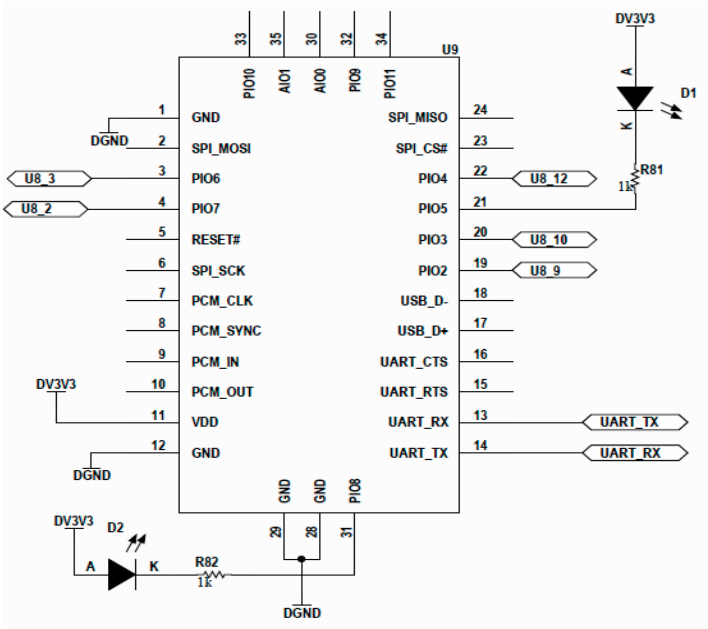


Figure 3.13: Bluetooth module

R92 to limit the current drawn in the event of $\overline{\text{MCLR}}$ breakdown. The programming clock pin PGEC1 and programming data pins PGED1 of U8 are connected to the pin 4 and 5 of J1 respectively for programming and debugging the microcontroller. The controller has two ports, port A (RA0 to RA4) and port B (RB0 – RB15). Each pin of port B can be either used as a general-purpose I/O pin or as a special function can be assigned to it. It has two on-chip SPI modules, which support 8-bit and 16-bit data formats with clock frequency up to 40 MHz. SPI-1 is used to control the impedance converter chip TI/AFE4300 and ECG extractor IC ADS1298, and SPI-2 is used to control the two digital potentiometers. The microcontroller has an on-chip ADC which can support 10-bit conversion up to 1.1 MHz or 12-bit up to 500 kHz sampling. The ADC is used for sampling the output of the summing amplifier with 10-bit resolution, and the pin AN4 is configured as the ADC input pin. The microcontroller has five internal timers (Timer-1−Timer-5). The sampling frequency of the ADC is set by loading appropriate value in the Timer-5 register. The ADC code corresponding to the demodulated impedance is sent after regular intervals of 5 ms. The UART module is used to transmit and receive signals from the Bluetooth module. It is configured with 9600 baud, 8-bits, 1 stop bit, and no parity.

3.10 Bluetooth module

The Bluetooth transceiver module RN42 [40] from Roving Networks with an integrated antenna is used to wirelessly send the acquired time-varying impedance from impedance converter AFE4300 IC and the ECG signal from ADS1298 to GUI software on the PC or a handheld

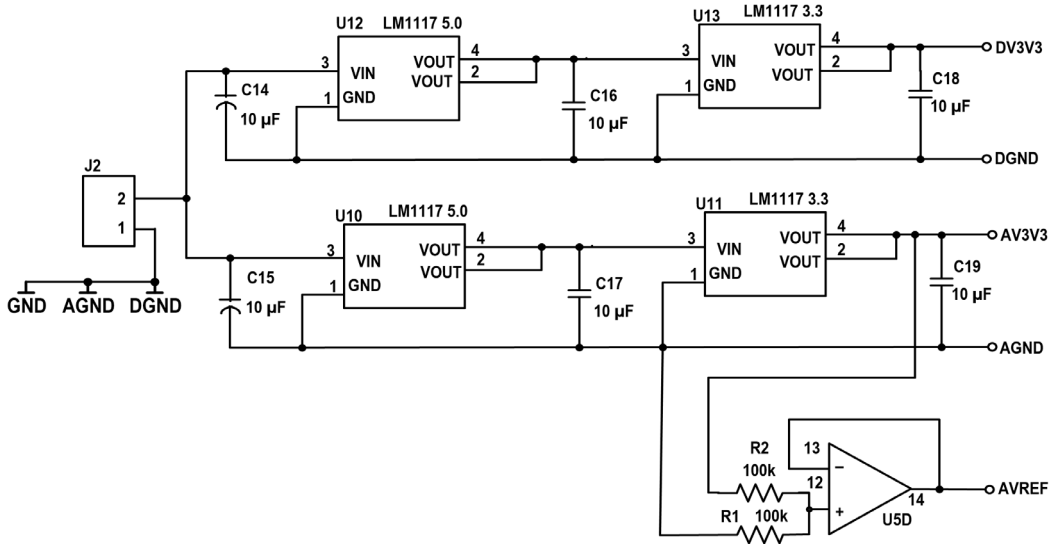


Figure 3.14: Power circuit

Table 3.1. Estimation of current requirements of the various blocks in ICG instrument

Supply voltage	Component	Current Requirement (mA)
AV3V3	U1: AFE4300 U4: ADA4807 U5: ADA4807 U6: THS4551 U7: ADS1298 U8:DSPIC33FJ128GP802 Total	0.970 4.4 4.4 1.40 2.75 9 22.92
DV3V3	U2:AD8400 U3:AD8400 U7: ADS1298 U8:DSPIC33FJ128GP802 U9: RN42 Total	4 4 0.5 40 50 98.5

computing device. It receives the data from the GUI software for setting the parameters of excitation and calibration. The circuit is shown in Figure 3.13, with the Bluetooth module as U9. It is used with 3.3 V digital supply. It has a UART interface with a programmable baud rate up to 115.3 kbps. LED D1 is connected to pin PIO5, with its blink speed indicating connection status as

discoverable mode, command mode, and connected mode. The resistor R81 is connected to limit the current through LED D1. LED D2 is connected to PIO8 to indicate the status of UART transmission and receiving activity. The UART_TX and UART_TX pins of RN42 are connected to the RP5 and RP4 pins of the microcontroller, which are mapped to the UART receive and transmit functions, respectively

3.11 Power Circuit

To reduce the coupling between analog and digital blocks, two separate regulators are used for powering the analog and digital parts of the circuit, as shown in Figure 3.14. The circuit is powered by analog 3.3 V, analog reference 1.65 V, and digital 3.3 V labeled as AV3V3, AVREF, and DV3V3, respectively using two linear regulators ICs U11 and U13. Low dropout linear regulator LM1117 [41] from Texas Instruments, with the input voltage range 4.75−10 V is used for this purpose. The op amp U5D has been used to generate a reference voltage of 1.65 V from the analog 3.3V supply to get the maximum voltage swing on either side of the reference, as the on-chip ADC of the microcontroller operates at 3.3 V. To keep the dissipation in the 3.3 V regulators low, their inputs are obtained from the corresponding 5 V LM117 regulators U12 and U10. Both the 5 V regulators are operated by a single dc input within the voltage range 6.5−12 V.

The analog module of microcontroller U8 and ECG extractor ADS1298 U7are powered by AV3V3 with reference to AGND and their digital module are powered by DV3V3 with reference to DGND. The op amps U5 and U4, THS4551 U6, and impedance converter IC AFE4300 U1 are powered by AV3V3 with respect to AGND and the digital potentiometers U2 and U3, Bluetooth module are powered by DV3V3 with respect to DGND. The total current consumption of the circuit is estimated by considering the current requirements of the individual chips, as shown in Table 3.1. Thus U12 has to supply 99 mA, and U10 has to supply 23 mA.

3.12 PCB design and system assembly

A two-layer PCB has been designed, assembled, and tested for the circuit. The software used for realizing PCB design is Altium Designer. The size of the PCB board is 80 mm x 100 mm. The components used in the PCB are of SMD package and are placed on both the layers to reduce the number of track crossovers and overall board size. The top and bottom side tracks are connected by PTH vias of 0.8mm diameter. The minimum signal track width used is 0.25 mm and the width of the power supply tracks is 1.25 mm. A minimum clearance of 0.33 mm has been used between two signal tracks. A 45^{0} corner style has been used for routing track corners.

Due to the presence of digital and analog blocks in the circuit, separate analog and digital supply and ground planes are designed to avoid the noise. Analog 3.3 V (AV3V3), analog

reference 1.65 V (AVREF), and digital 3.3 V (DV3V3) are provided on the top layer of the PCB. Analog ground (AGND) and digital ground (DGND) planes are provided on the bottom layer. The analog ground and digital ground are routed separately throughout the board and are shorted at the input power supply. Shortest overall connection path has been chosen for pin-to-pin connections. The supply to each IC is provided with 0.1 μF decoupling capacitors to suppress high-frequency noise in power supply signals, which are placed close to the IC. A 5-pin connector has been used for connecting Microchip's PICkit3 debugger for programming and debugging the microcontroller. The different hardware blocks of the device have been separated using jumpers for testing them individually. Each circuit blocks were tested separately to ensure their functionality. The complete schematic of the impedance cardiography hardware is given in Appendix A, and the PCB layout, including the top layer, the bottom layer, and the top overlay, and the top and bottom sides of the assembled PCB are given in Appendix B.

3.13 Microcontroller program

The microcontroller code is written in embedded C using the Microchip MPLAB IDE and loaded into the program memory of the microcontroller through the PICKIT3 programmer/debugger. The main tasks performed by the microcontroller are the following.

1. Setting the impedance converter IC AFE4300 parameters frequency of DDS, ADC data rate, setting the demodulation method, performing the magnitude and phase calibration using reference resistors, and selection of current injecting and voltage sensing terminals, through SPI-1 interface.
2. Continuously monitoring the output of voltage summing amplifier via ADC with a sampling frequency 10 times higher than the carrier signal frequency which is set by loading Timer-5.
3. Controlling the amplitude of the excitation current signal using the digital potentiometer U2 and the baseline correction signal using the digital potentiometer U3, based on the comparison of output of the baseline correction amplifier with predefined thresholds, via SPI-2 interface.
4. Generating the input clock for the impedance converter U1 by Timer-2 and the ECG extractor U7 by Timer-3.
5. Communicating with the PC based GUI for sending the demodulated time varying impedance value at regular intervals, through UART and Bluetooth transceiver module.

The above tasks are carried out through the steps in the main function and using the interrupt

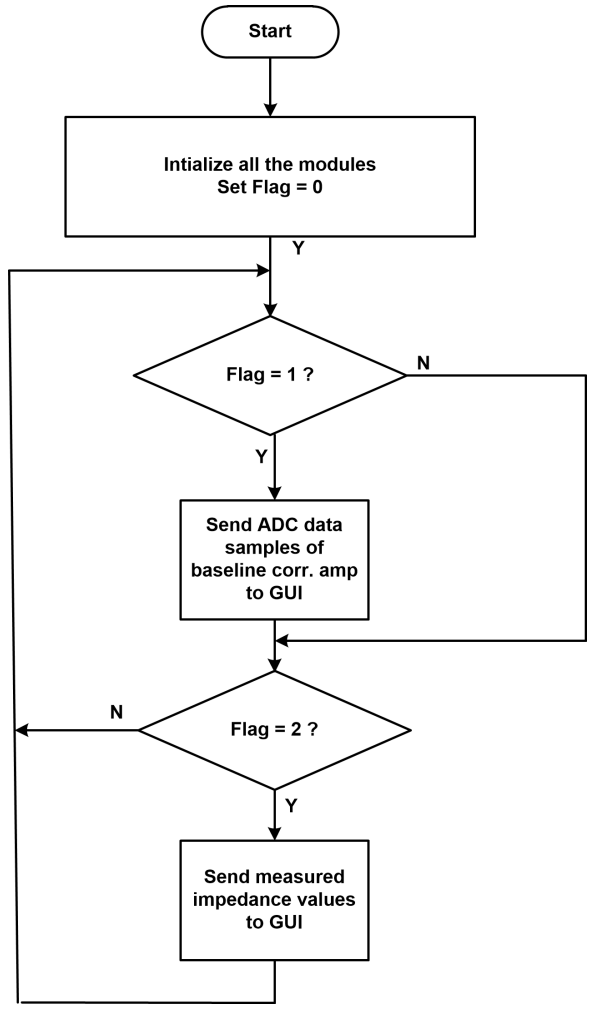


Figure 3.15: Flowchart of main function

service routines (ISR) that can interrupt the main program. Figure 3.15 shows the flowchart of the main function.

The main function comprises following steps.

1. Initialize the system clock, SPI-1, SPI-2, ADC, Timer-2, Timer-3, Timer-5 and UART modules and configure I/O ports.
2. Initialize the impedance converter IC AFE4300 and set the parameters for DDS frequency, ADC data rate, voltage sensing terminals, and the demoulation method through SPI-1 interface.
3. Set the default values of digital potentiometer U2 and U3 through the SPI-2 interface
4. Set an indefinite loop to continuously check the value of the 'Flag', set by the UART interrupt service routine. If the value of 'Flag' is 1, the ADC samples are acquired by calling a function and stored in an array of a size 200. It is then sent to the GUI for plotting via Bluetooth. Similarly, if the value of 'Flag' is 2, the demodulated impedance

samples are acquired and stored in an array of size 200. It is then sent to the PC via Bluetooth for plotting.

The clock configuration bits are used to select the fast FRC oscillator with device clock frequency as 80 MHz. All the I/O ports are configured by programming appropriate TRIS and LAT registers. The SPI-1 module is used to send a data packet of 24 bits to the impedance converter IC, in which first 8 bits represent the address of the register and the remaining bits corresponds to the data to be stored. The SPI-2 module is used to send a data packet of 16 bits to set the value of variable resistance in the digital potentiometer IC AD8400. The 16-bit Timer-5 is used to set the sampling frequency of on-chip ADC for sampling the voltage sensing amplifier output. Depending upon the sampling rate f_s the value N_{timer} is loaded in the Timer-5 register. i.e., $N_{timer} = F_{CY}/f_s$, where F_{CY} is the instruction cycle clock frequency of the microcontroller. The 1 MHz input clock to the impedance converter U1 is generated by the toggling of microcontroller pin RP6 when the Timer-2 value matches the compare register value. Similarly, the 2 MHz input clock to the ECG extractor U7 is generated by microcontroller pin RP10 by loading the 16-bit Timer-3. The demodulated impedance samples are sent to GUI via UART at regular intervals of e5 ms.

Depending upon the range of load impedance to be measured, the value of excitation current is adjusted using the digital potentiometer U2 so that the output of the baseline correction amplifier does not go into saturation. The baseline correction can be either done by comparing the maximum and minimum of a fixed number of ADC samples in an array, with the upper threshold level and lower threshold level, respectively, or by monitoring the output of baseline correction amplifier on the GUI. Here, the second method is used. If the peak to peak value exceeds the limits and the digital potentiometer U3 is adjusted to remove the baseline drift from the sensed signal and bring it back to threshold limits. The adjustment of U2 and U3 is done by sending appropriate ASCII character from the GUI.

UART interrupt service routine (UIRX Interrupt).

The UART module invokes the 'U1RX Interrup*t*' whenever it receives an ASCII character from GUI via Bluetooth and stores the character in the UART receive register. The ISR 'U1RX Interrupt' is written to perform calibration, setting the amplitude of current excitation and the baseline correction signal, monitoring the output of baseline correction amplifier and reading the time-varying demodulated output from the impedance converter chip, based on the ASCII command received. Figure 3.16 shows the flowchart of 'UIRX Interrupt' ISR. The steps involved in UART ISR are given below.

1. Store the received ASCII character in a variable and check it for selecting the operations to be performed.

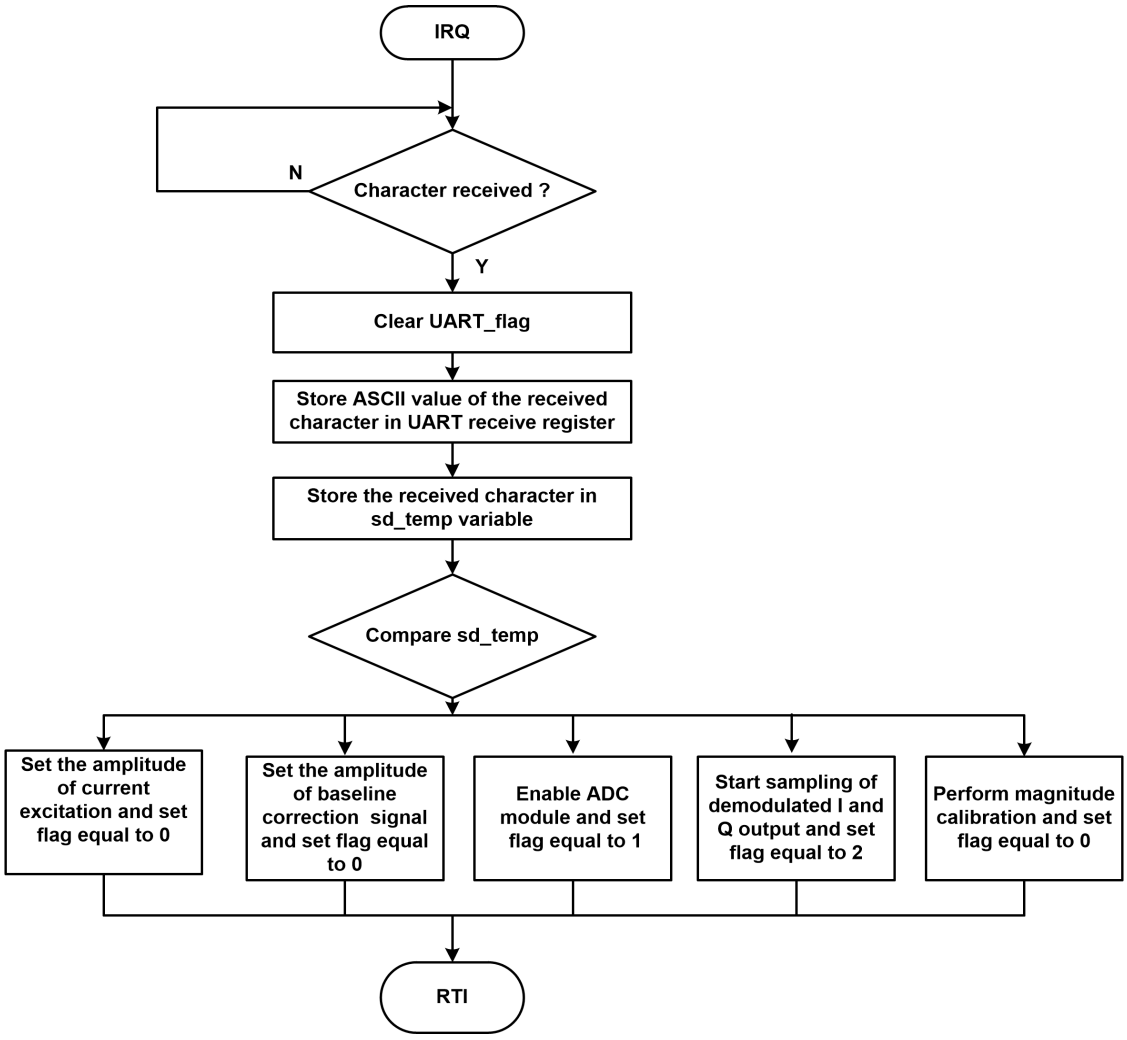


Figure 3.16: Flowchart of UIRX interrupt ISR

2. If the received character corresponds to calibration is received, then the magnitude calibration is performed using two reference resistors Rx and Ry by reading out 30 samples of each demodulated output. The average of 30 samples is used to calculate the slope m' and the offset o by two-point calibration method. Send the slope m', and offset o via Bluetooth to the GUI. Also, set 'Flag' as '0'.
3. If the received character corresponds to setting the amplitude of current excitation, then the digital potentiometer U2 value is adjusted accordingly via SPI-2. Also, set 'Flag' as '0'.
4. If the received character corresponds to setting the amplitude of baseline correction signal, then the digital potentiometer U3 value is adjusted accordingly via SPI-2. Also, set 'Flag' as '0'.
5. If the received character corresponds to ADC output, then the following steps are executed.
    a) Enable Timer-5 and ADC module and set Flag as '1'.

b) Load Timer-5 with the value corresponding to the sampling rate.
c) Send the command to start ADC sampling of the output of the baseline correction amplifier.

6. If the received character corresponds to Z output, then the following steps are executed.
   a) Disable Timer-5 and ADC module and set Flag as '2'
   b) Set the ADC conversion mode as 'Continuous conversion mode' and send the command to start sampling of demodulated I and Q output.
7 Return to the main program.

3.14 PC-based GUI for impedance data acquisition

A PC based graphical user interface is developed using 'Qt' framework for acquiring the impedance data acquisition and plotting the time varying impedance. It can be invoked by clicking on the 'icg_demodulator.exe' file installed on the PC. The GUI program communicates with the RN42 Bluetooth module interfaced with microcontroller in the demodulator circuit over a serial COM port of the PC. The Bluetooth module of the demodulator needs to be paired with Bluetooth of PC for data transfer. A plot area is located in the centre on which the impedance waveform can be plotted using the 'Qcustomplot' class in 'Qt' which gives the facility to interpolate between two adjacent ADC samples, x-axis and y-axis scaling etc. Figure 3.17 shows the screenshot of the GUI developed in which the time varying impedance measured using impedance converter IC TI/AFE4300 in the FWR mode is plotted. The frequency of excitation current was set as 20 kHz and a time-varying impedance is generated using a digital potentiometer in the form of a step variation from 90 Ω to 100 Ω.

The GUI has nine buttons such as 'Connect', 'Disconnect', 'Clear_adc', 'Clear_Z', 'start_Z' 'Plot Z', 'start_ADC', 'ADC_out', and 'Quit' and two labels such as 'Status' and 'I/Q magnitude'. The COM port selection is done by a drop-down list. The GUI includes features for controlling the amplitude of current excitation and the baseline correction signal. It has two vertical sliders 'Amp' and 'Base Corr'. The 'Amp' slider is used for setting amplitude of the current excitation by controlling the digital potentiometer U2. The 'Base Corr' slider is used for setting amplitude of the baseline correction signal by adjusting the digital potentiometer U3. Each time a value is changed in the slider controls, an ASCII character is sent from PC over the Bluetooth to the ICG instrument. The microcontroller receives the character from the Bluetooth device through its UART module, which invokes an interrupt. The microcontroller program identifies the ASCII character and performs the corresponding operation.

A COM port of PC is provided to the paired Bluetooth USB adapter module which can be identified by the Bluetooth device setting option. From the drop-down list of available COM ports given in GUI, select the assigned one. In the GUI code the baud rate, number of data bits, stop bit,

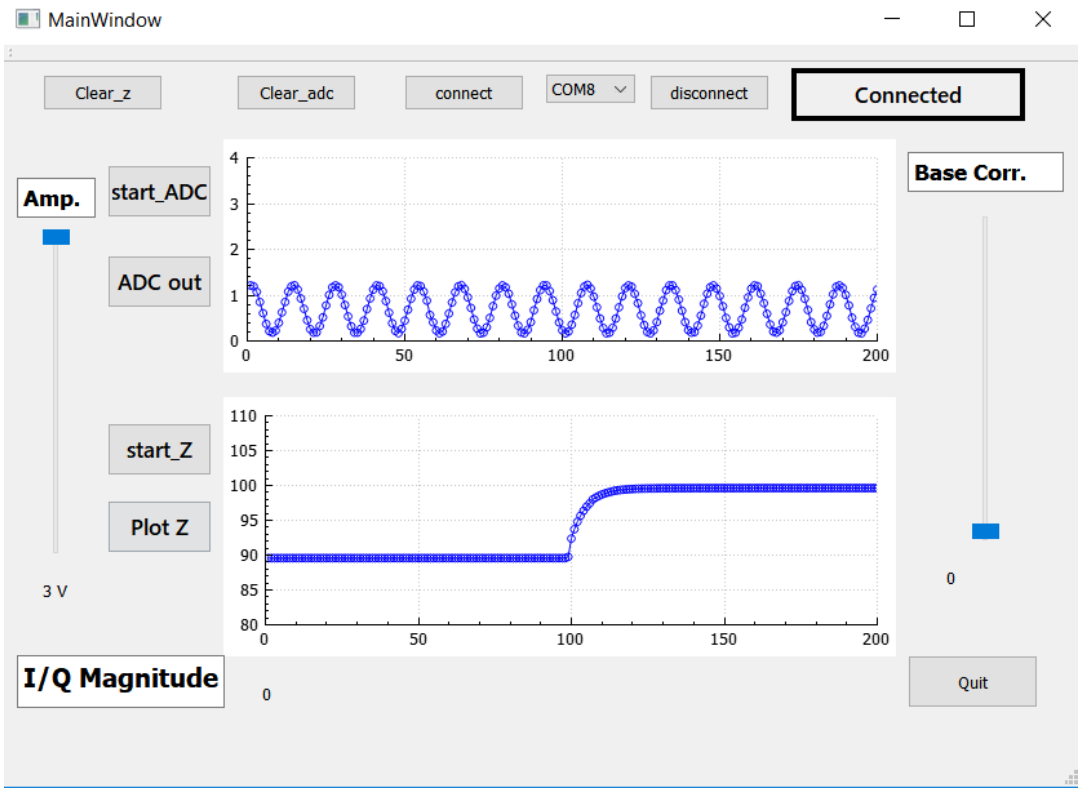


Figure 3.17: Screenshot of the GUI for impedance cardiograph

and parity are initialized as 115200 bps, 8, 1 and 0 respectively. After choosing the appropriate COM port click on the 'Connect' button. If the serial connection is established between the demodulator and PC, the label 'Status' will show as connected else shows 'Not connected'. The 'Disconnect' button is used to disconnect the connection.

A plot area is provided to monitor the output of the baseline correction amplifier to ensure that the peak-to-peak value of the sensed signal is not exceeding the ADC input range. The button 'start_ADC' is used for enabling ADC sampling of baseline correction amplifier output and the button 'ADC_out' is used for plotting the received data samples. Similarly, the button 'start_Z' is used for enabling ADC sampling of demodulated I and Q output and the button 'Plot_Z' will initiate the reading of data received at the serial port. After receiving 4 bytes of data which corresponds to the magnitude of unknown impedance, the received value is calibrated using the slope *m*' and offset *o* values and then plotted on the graph. Also, the calibrated value is displayed under 'I/Q magnitude' label. The time-varying impedance waveform is displayed by plotting 200 such samples. Using 'Clear' button, the graph can be cleared and can start plotting again. The 'Quit' button is for closing the GUI.

Chapter 4

TEST RESULTS

4.1 Introduction

After assembling the impedance cardiograph circuit on a two-layer PCB, the different hardware blocks and associated software were tested separately. The ICG instrument was tested for its (i) linearity during measurement of static resistances, (ii) effect of carrier frequency on measurement of static impedances, (iii) noise rejection, and (iv) dynamic response for measurement of pulsatile change in resistance. Before performing the measurements, two-point magnitude and phase calibration was carried out using two reference resistors, with values measured using a multimeter as R_x = 572 Ω and R_y = 100 Ω.

For testing the linearity during measurement of static impedances, the static resistance across the current injecting terminals was varied and the corresponding demodulated output was recorded, keeping the frequency and amplitude of the excitation constant.

The second test was carried out by varying the excitation frequency, with constant amplitude of the current excitation and constant load resistance for examining the effect of excitation frequency in both the demodulation modes of AFE4300. The relative error in the magnitude and phase measurement was calculated by comparing it with those values measured using a multimeter.

The noise rejection of the instrument was tested by injecting an interfacing current at different frequencies for a fixed load resistance. In this test, the amplitude and frequency of the current excitation was kept constant. The relative magnitude error for synchronous I/Q modulation was calculated from the recorded values.

For finding the dynamic response of the instrument for measurement of pulsatile change in the resistance, a time-varying load resistance was connected across the current terminals. The time-varying resistance was in the form of periodic pulsatile changes in the resistance, of 0.1−10% of the base resistance. It was generated using a microcontroller and a digital potentiometer. The amplitude and frequency of the current excitation were kept constant during the test. The time-varying measured resistance values were recorded using GUI.

The methods of the above tests and the results obtained are presented in the following sections.

4.2 Linearity during measurement of static resistances

The testing was carried out in two stages. The first stage of testing was for the impedance converter chip using its internal current source and the voltage amplifier. The second stage of

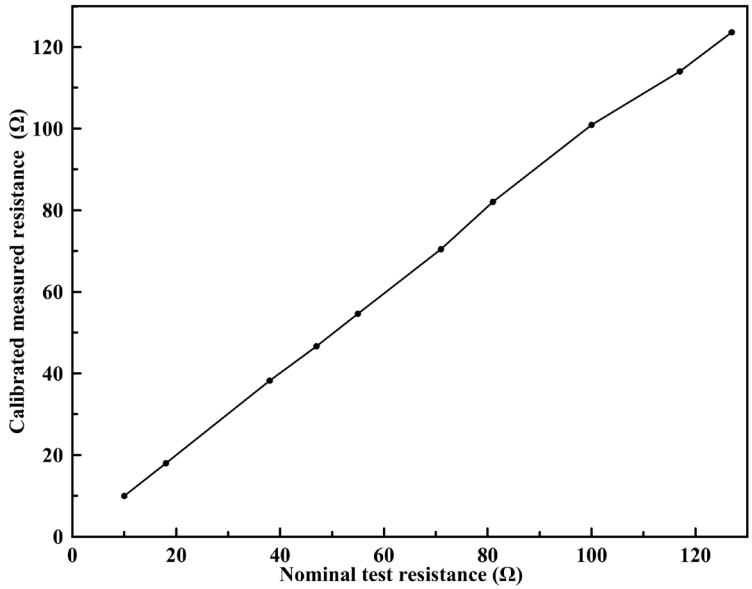


Figure 4.1: Plot of the measured value using the chip vs the resistance value measured using a multimeter.

Table 4.1. Error in measurement of resistance for various test resistances

Test resistance value measured by multimeter (Ω)	Value measured using the chip in synchronous mode (Ω)	Error (%)
10	9.9	0.1019
18	17.9	0.10
38	38.2	0.60
47	46.6	0.77
55	54.6	0.67
71	70.4	0.75
81	82.04	1.29
100	100.9	-0.91
117	114.01	2.55
127	123.60	2.67

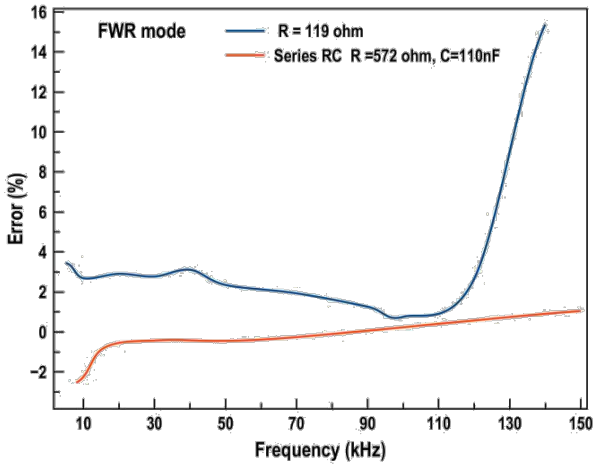


Figure 4.2: Relative error obtained for FWR mode

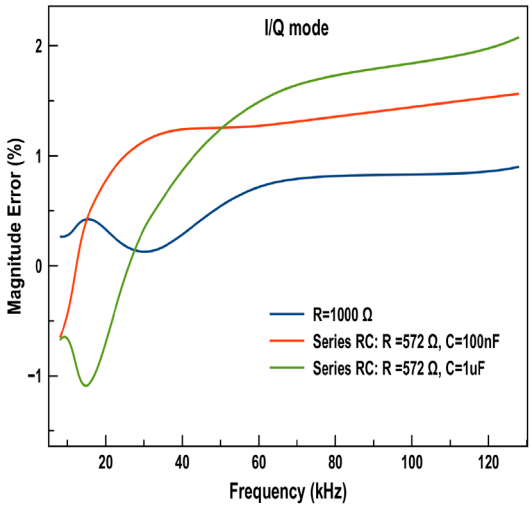


Figure 4.3: Relative error in magnitude for I/Q mode

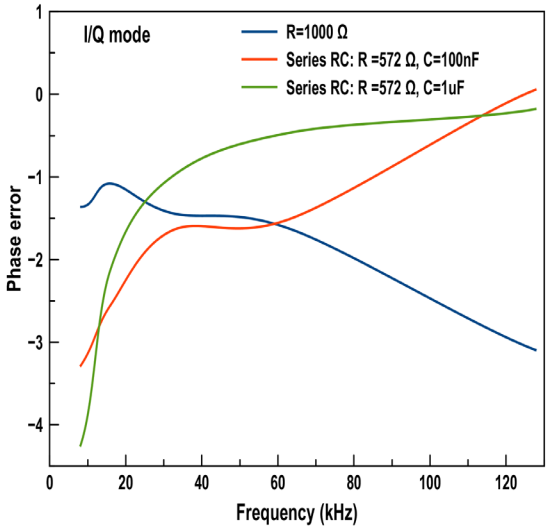


Figure 4.4: Relative error in phase for I/Q

testing was for the assembled instrument, with the external balanced current source and the external voltage sensing amplifier with common mode feedback. In the first stage, testing was carried out for both modes of demodulation. In the second stage, only synchronous demodulation was used.

For testing the linearity of the impedance converter T1/AFE4300, different test resistors with nominal values from 100 Ω to 1200 Ω were connected across the current injecting terminals IOUTP1 and IOUTN0. These terminals were connected to the voltage sensing terminals VSENSEP1 an VSENSEN0. The magnitude of the injected current was 247.5 µArms and the frequency of measurement was 64 kHz. The impedance measurements were made in both FWR and IQ mode. The values of the resistors were also measured using a multimeter. It was found that

the graph between nominal and measured resistance values is almost linear. The linearity was valid for resistance up to 1200 Ω .

The linearity of the ICG instrument developed was tested by reading the demodulated samples from TI/AFE4300 for different values of resistances as load impedance. The excitation amplitude and frequency of excitation were set as 2.5 mA peak to peak and 20 kHz, respectively. Analog reference AVREF was given as the baseline correction signal obtained by keeping the digital potentiometer U3 wiper at its minimum position. The resistances were varied from 10 Ω to 130 Ω after the magnitude calibration using reference resistors. The test resistance values measured using a multimeter and the corresponding values measured using the instrument are given in Table 4.1. The errors for measurement of the impedances are found to be below 3%. Figure 4.1 shows the graph between test resistance and the calibrated measured resistance.

4.3 Effect of carrier frequency on measurement of static impedances

The impedance converter chip TI/AFE4300 was tested both in FWR and I/Q mode by injecting current at different frequencies for fixed test impedance. The frequency was varied from 5 kHz to 150 kHz. The measurements were made by averaging 32 samples. The relative error was calculated with reference to the values using an impedance analyzer. Figure 4.2 shows the relative error obtained for FWR mode for (i) the impedance consisting of R =119 Ω and (ii) the impedance consisting of series RC network with R= 572 Ω and C =110 nF. It was found that the relative error of magnitude measurement in FWR mode was less than 5% for frequency up to 110 kHz and increased for higher frequencies, with an error of about 15% at 130 kHz. Figure 4.3 and Figure 4.4 show the relative error in magnitude and phase measurement of I/Q mode for three test impedances: (i) R =1000 Ω, (ii) series RC network with R = 572 Ω and C = 100 nF, and (iii) series RC network with R = 572 Ω and C = 1 uF. In the I/Q mode, the magnitude error was found to be less than 2% and the phase error less than 4% for all the test frequencies, showing that the synchronous demodulation scheme gives better noise performance. The measurements for the assembled instrument need to be carried out.

4.4 Noise rejection

The noise rejection of the hardware was tested by injecting an interfacing current at different frequencies for fixed resistance R =119 Ω as shown in Figure 4.5. The op amp U14 corresponds to the single-ended V/I converter inside the impedance converter chip TI/AFE4300. The excitation current amplitude and frequency was 247.5 μArms and 32 kHz respectively. The interference voltage was kept 500 mVpp and its frequency was varied from 5 kHz to 1000 kHz. The relative magnitude error for synchronous I/Q modulation is shown in the Figure 4.6 as the frequency is varied from 5 kHz to 1000 kHz. It was found that the relative error is maximum when

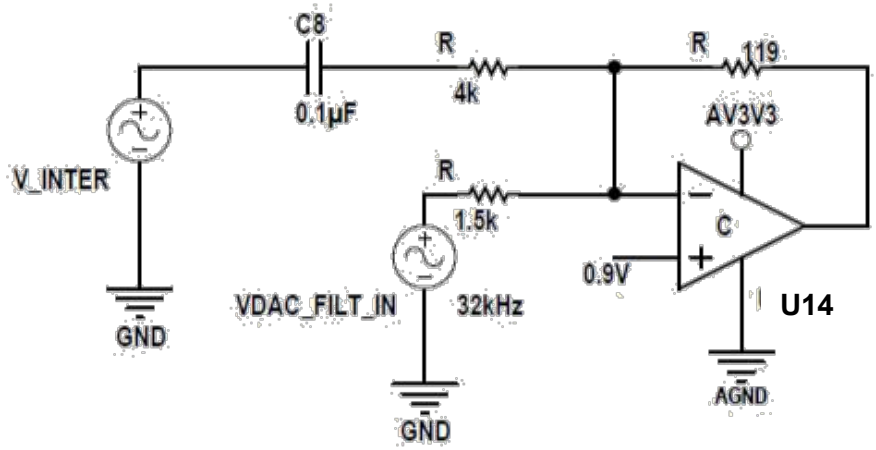


Figure 4.5: Noise rejection testing circuit

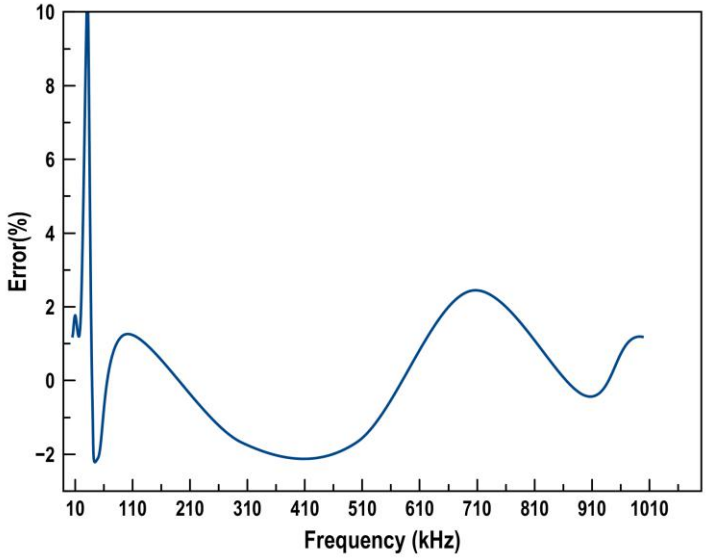


Figure 4.6: Relative error in magnitude for I/Q mode at different interfering frequencies

the interfering frequency is near the excitation frequency 30 kHz to 33 kHz, else the interference effect is less than 2%. The measurements for the assembled instrument need to be carried out.

4.5 Dynamic response for measurement of pulsatile change in resistance

The ICG instrument was tested for various impedance variations of 0.1−10% over a base resistance. The excitation amplitude and frequency of excitation were set as 2.5 mA peak to peak and 20 kHz, respectively. The test setup for generating the impedance simulations is shown in the Figure 4.7. The resistor R91 represents the basal component and the digital potentiometer IC AD8400, labelled as U15, generates the time-varying component. E1 and E2 represents the electrode contact points. The total resistance across the electrode pair will be parallel

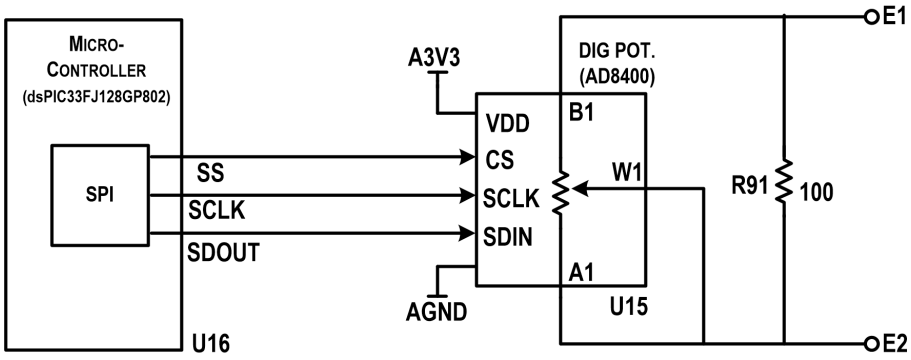
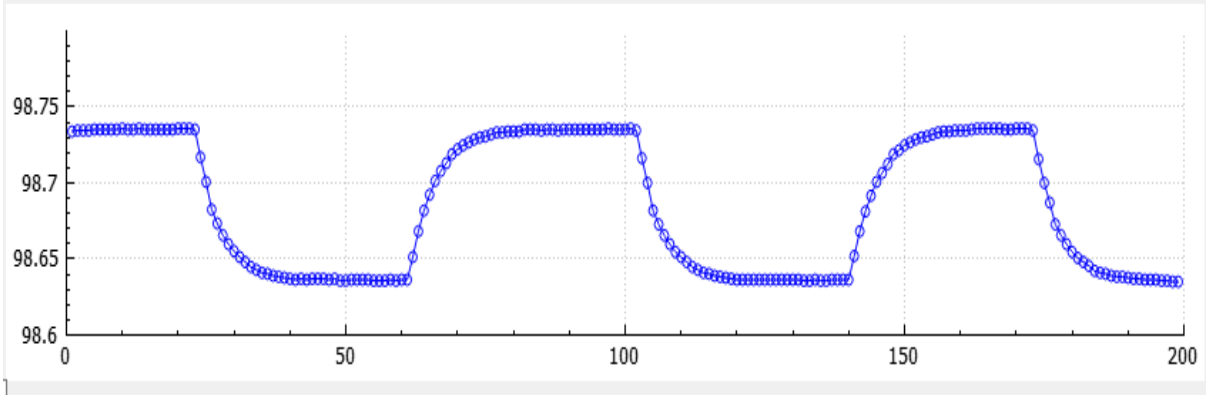


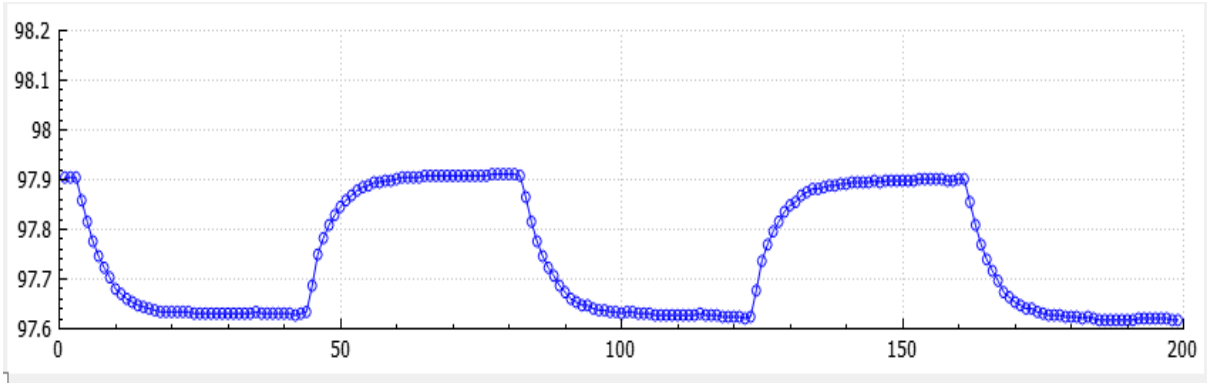
Figure 4.7: Test setup for generating impedance variations.

combination of 100 Ω and the resistance across digital potentiometer R_{WB}. U15 operates with a supply voltage of 2.7−5.5 V and has a total resistance of 10 kΩ with 256 steps and a wiper resistance of 50 Ω. The wiper position is controlled by the microcontroller through the SPI interface. The impedance simulator generates time-varying resistance in the form of square wave variation over a base resistance by changing the digital potentiometer U15 ratio at a frequency of 16 Hz. The on chip timer of microcontroller is used to set the frequency of variation. The microcontroller "Microchip dsPIC33FJ128GP802" is used for controlling the periodic change in the basal resistance via SPI module.

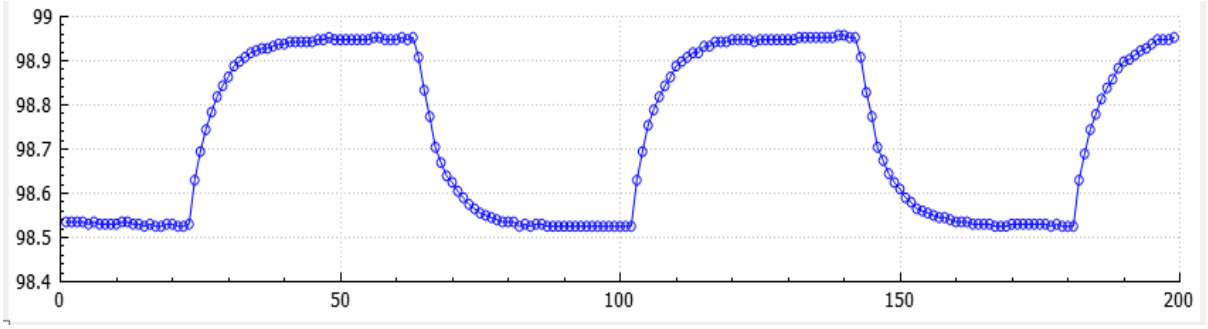
Let ΔR be the change in base resistance when the digital potentiometer is switched between two different values. The first value corresponds to 10 kΩ and the second value is chosen depending upon the desired ΔR. Thus, the variation of resistance can be obtained over 99 Ω (99-ΔR). Figure 4.8 shows the plots of time-varying measured resistance values ranging from 0.1−10% observed in the GUI. From the plots, it is found that the step changes introduced by the impedance simulator are correctly reflected in the measured values and shows a good match with the nominal values. Also, the peak ripples in the demodulated output are found to be less.



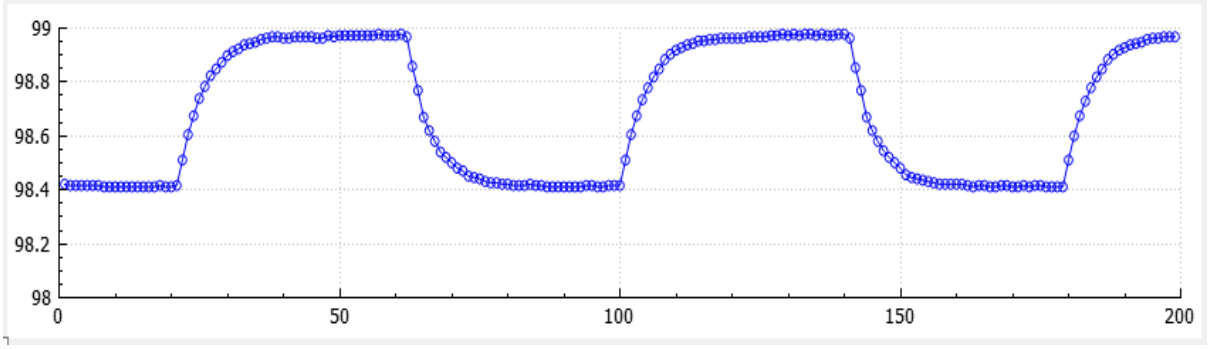
(a): ΔR = 0.1 Ω



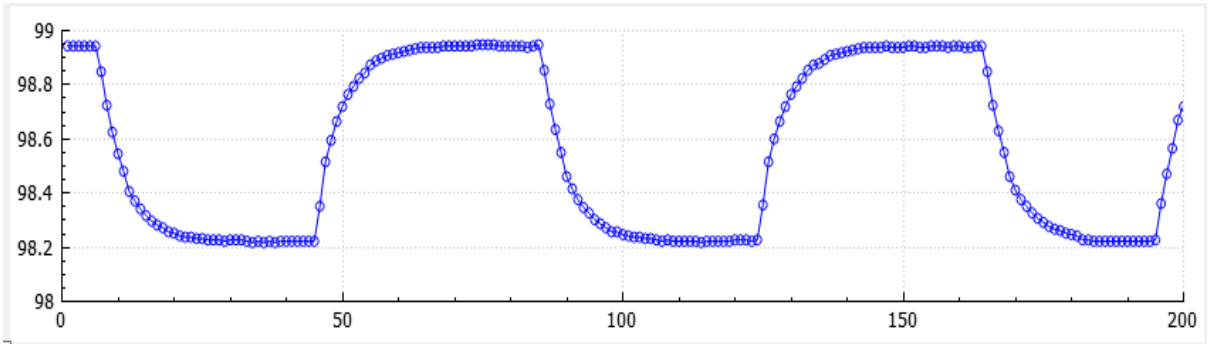
(b): ΔR = 0.3 Ω



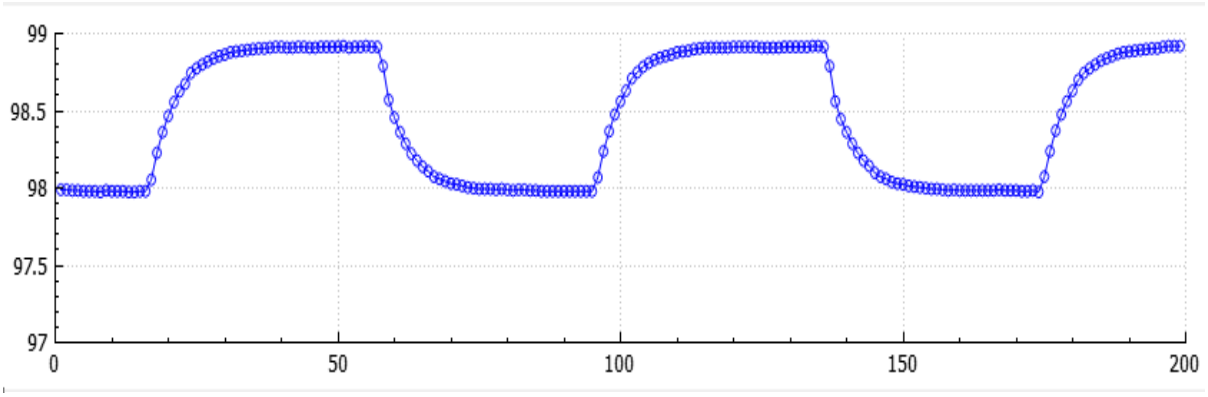
(c): ΔR = 0.5 Ω



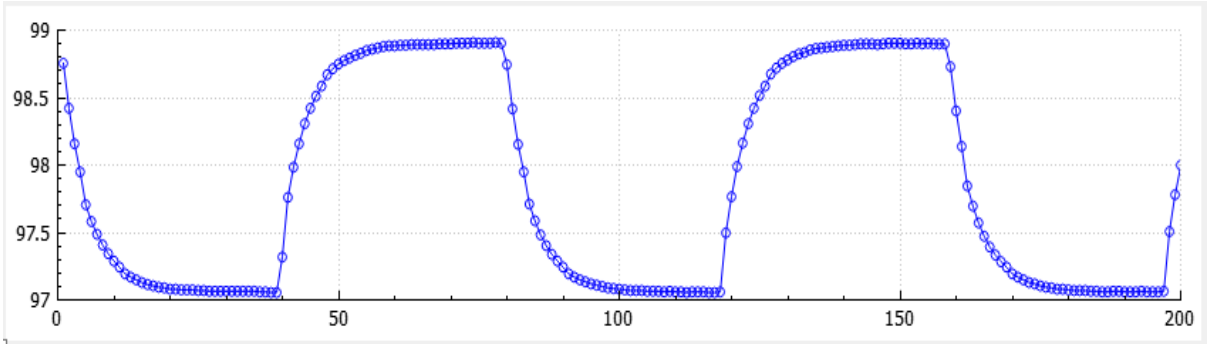
(d): ΔR = 0.6 Ω



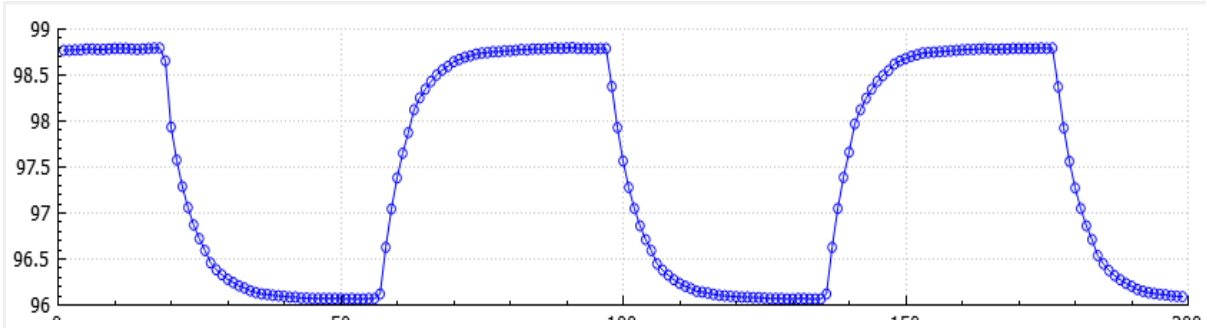
(e): ΔR = 0.7 Ω



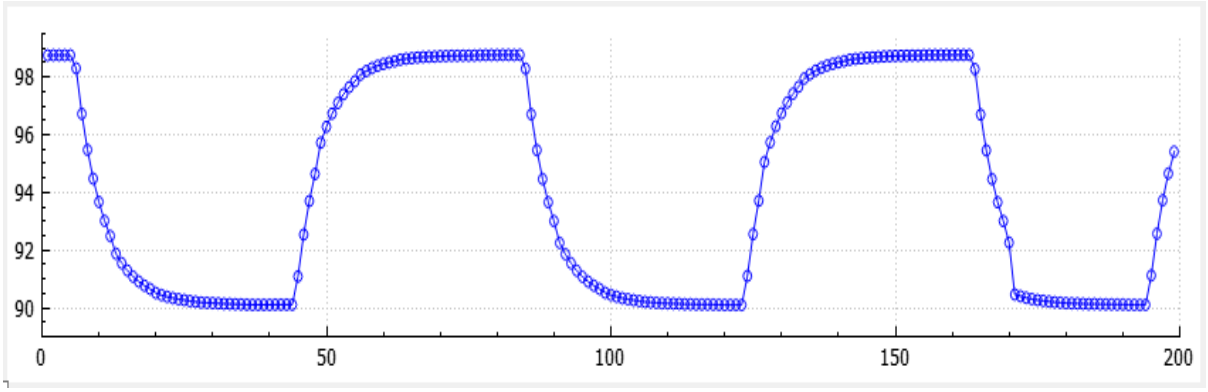
(f): ΔR = 1 Ω



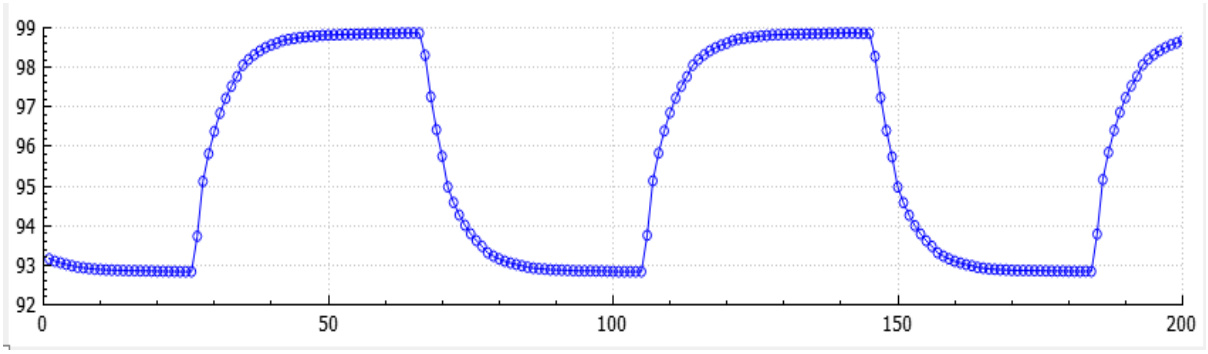
(g): ΔR = 2 Ω



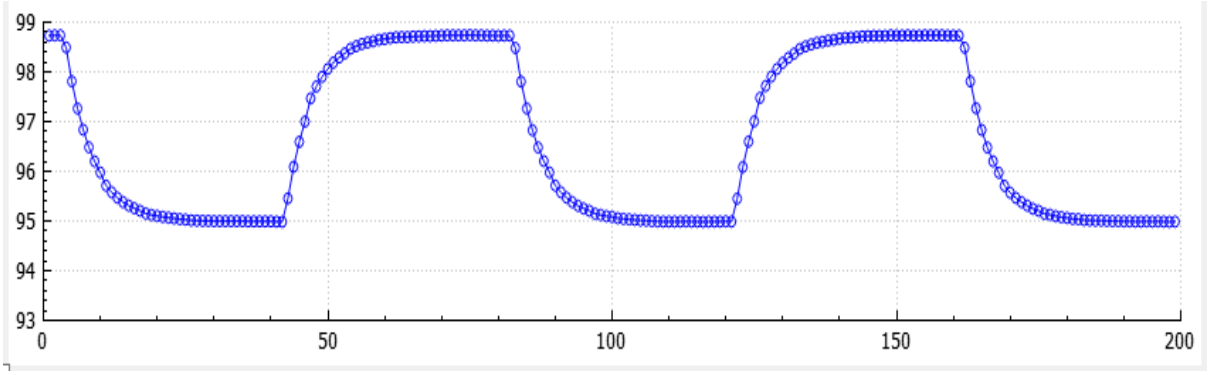
(h): ΔR = 3 Ω



(i): ΔR = 5 Ω



(j): ΔR = 7 Ω



(k): ΔR = 10 Ω

Figure 4.8: Plots of time-varying measured resistance values for different ΔR ranging from 0.1−10 Ω observed in the GUI .

Chapter 5

SUMMARY AND CONCLUSION

The project objective was to develop an impedance cardiograph for body wearable application, with emphasis on improving sensitivity, noise rejection, and ripple rejection and on reducing the circuit complexity. The developed instrument uses impedance monitoring by current excitation and amplitude demodulation of the sensed voltage using synchronous demodulation with integrated baseline correction. For reducing the chip count, we have used the impedance converter IC TI/AFE4300 for its on-chip DDS, synchronous demodulator, and sigma-delta ADC. For ECG extraction TI/ADS1298 has been used. The design uses a microcontroller and Bluetooth module for controlling all the measurement parameters. As the impedance converter chip does not have provision for separating the basal and time-varying components of the impedance signal, a baseline correction amplifier is used for integrating the baseline correction with the synchronous demodulation. For additional performance improvement, a transformer-less balanced current source and voltage sensing amplifier with enhanced CMRR have been devised and used in the design. To allow independent control of the amplitude of the current excitation and the baseline correction signal, two digital potentiometer ICs are used. A PC-based user interface was designed to acquire ICG data samples via Bluetooth interface. The circuit is powered by analog and digital 3.3 V supply.

The entire hardware has been assembled on a two-layer PCB. The different hardware blocks have been tested separately. The errors for measurement of static resistances are found to be below 3%. Also, the ICG instrument was tested for various impedance variations of 0.1−10% over a base resistance.

The output voltage swing of the excitation circuit is limited because of a mismatch in the voltage references of the voltage amplifier and the DDS. The circuit and the PCB design to be revised for removing this shortcoming. Subsequently, the following tests need to be carried out:

(i) CMRR of the voltage sensing amplifier as a function of excitation frequency.

(ii) Output impedance of the current source.

(iii) Noise rejection by the demodulator.

(iv) Carrier ripple suppression for different measurement rates.

(v) Dynamic response for pulsatile impedance changes as a function of excitation frequency.

(vi) Testing of the instrument using a thoracic impedance simulator providing time-varying impedance.

After completion of the tests and carrying out the required revisions, test for the safety considerations need to be carried out. Subsequently, the instrument should be packaged and used for recordings from subjects. After validation of the results, it can be used in clinical applications.

APPENDIX A

SCHEMATIC OF IMPEDANCE CARDIOGRAPHY HARDWARE

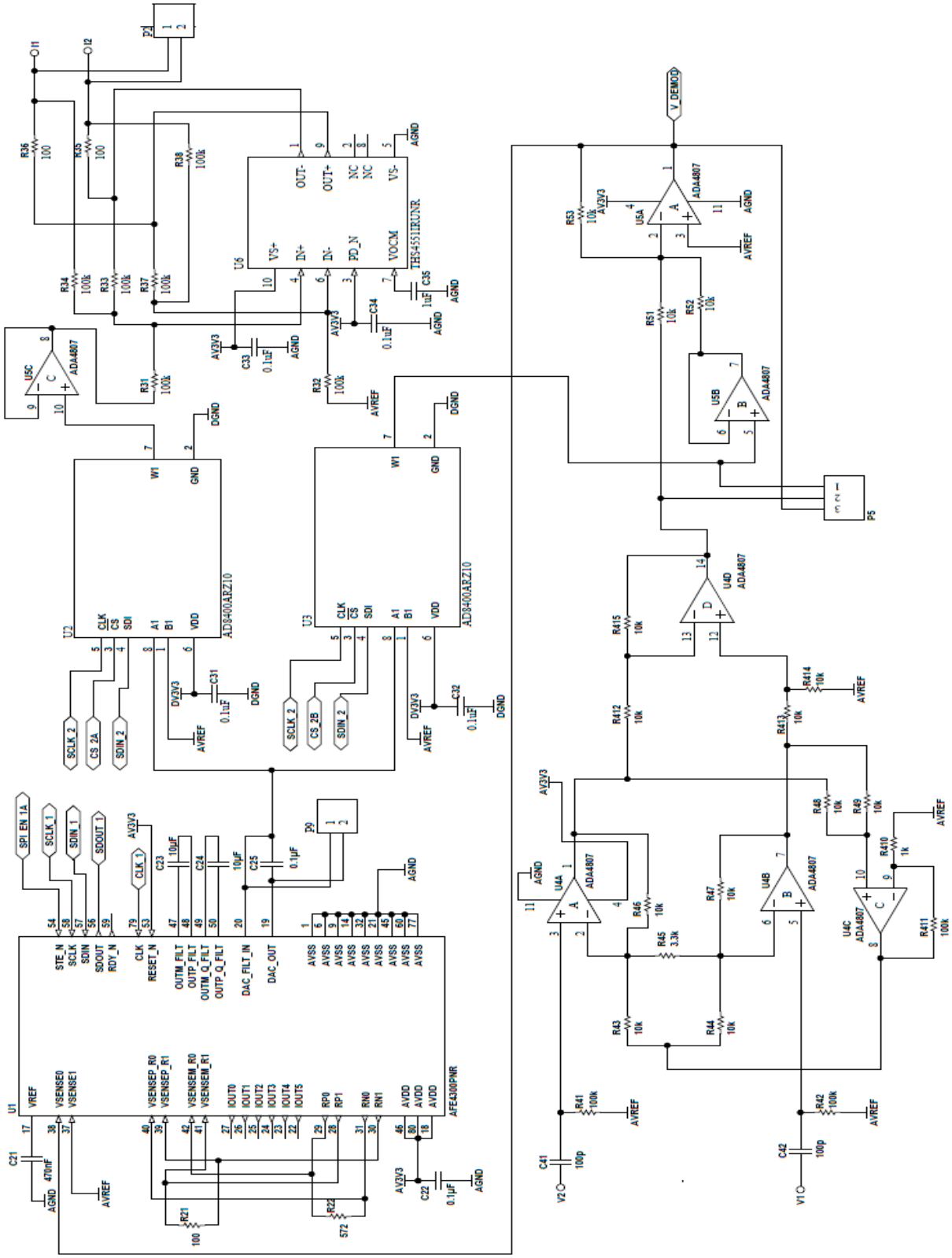


Fig. A.1: ICG schematic sheet 1: Impedance converter, V-I converter, voltage sensing amplifier, summing amplifier and digital potentiometers.

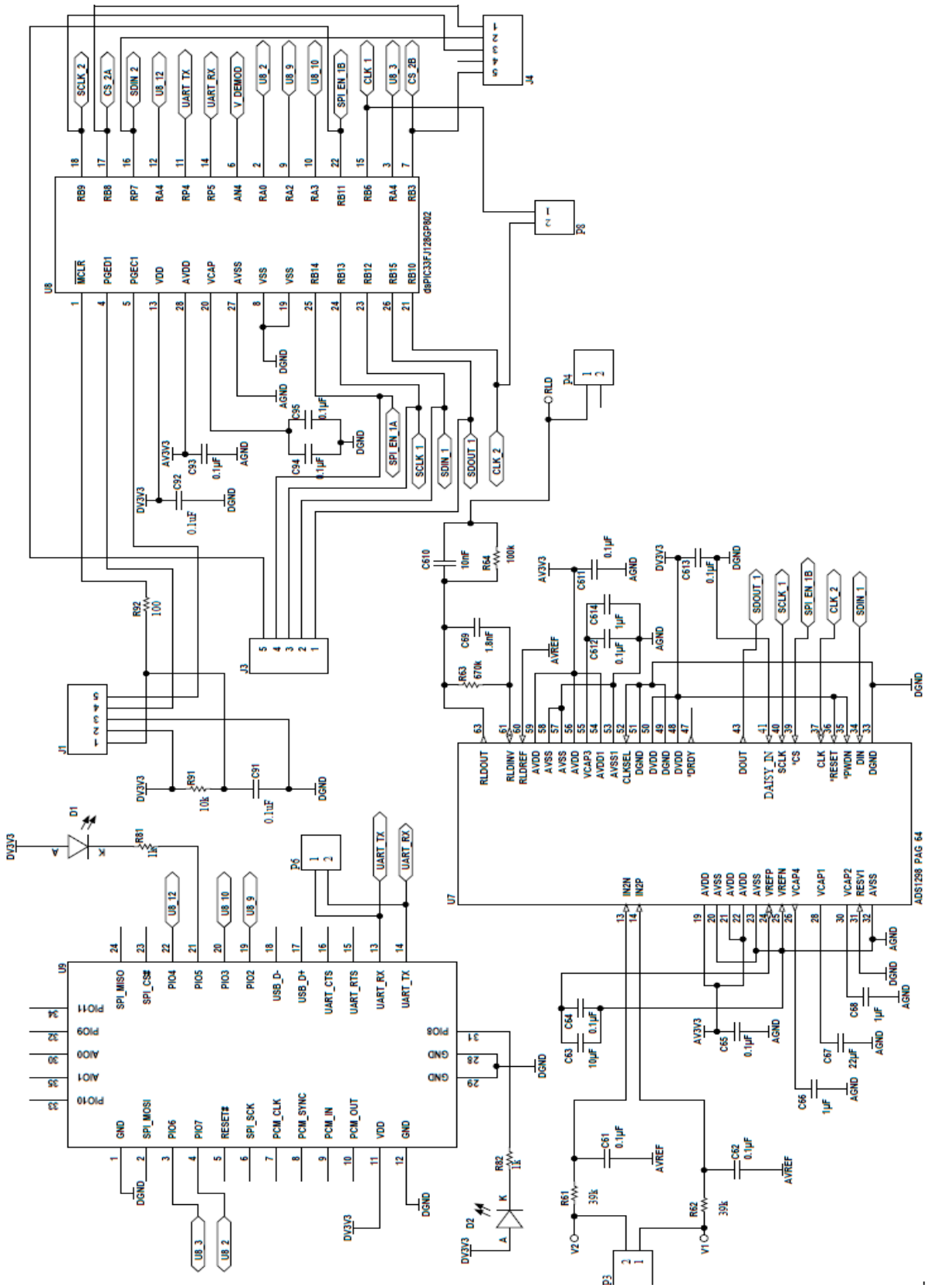


Fig. A.2: ICG schematic sheet 2: ECG extractor, microcontroller and Bluetooth module.

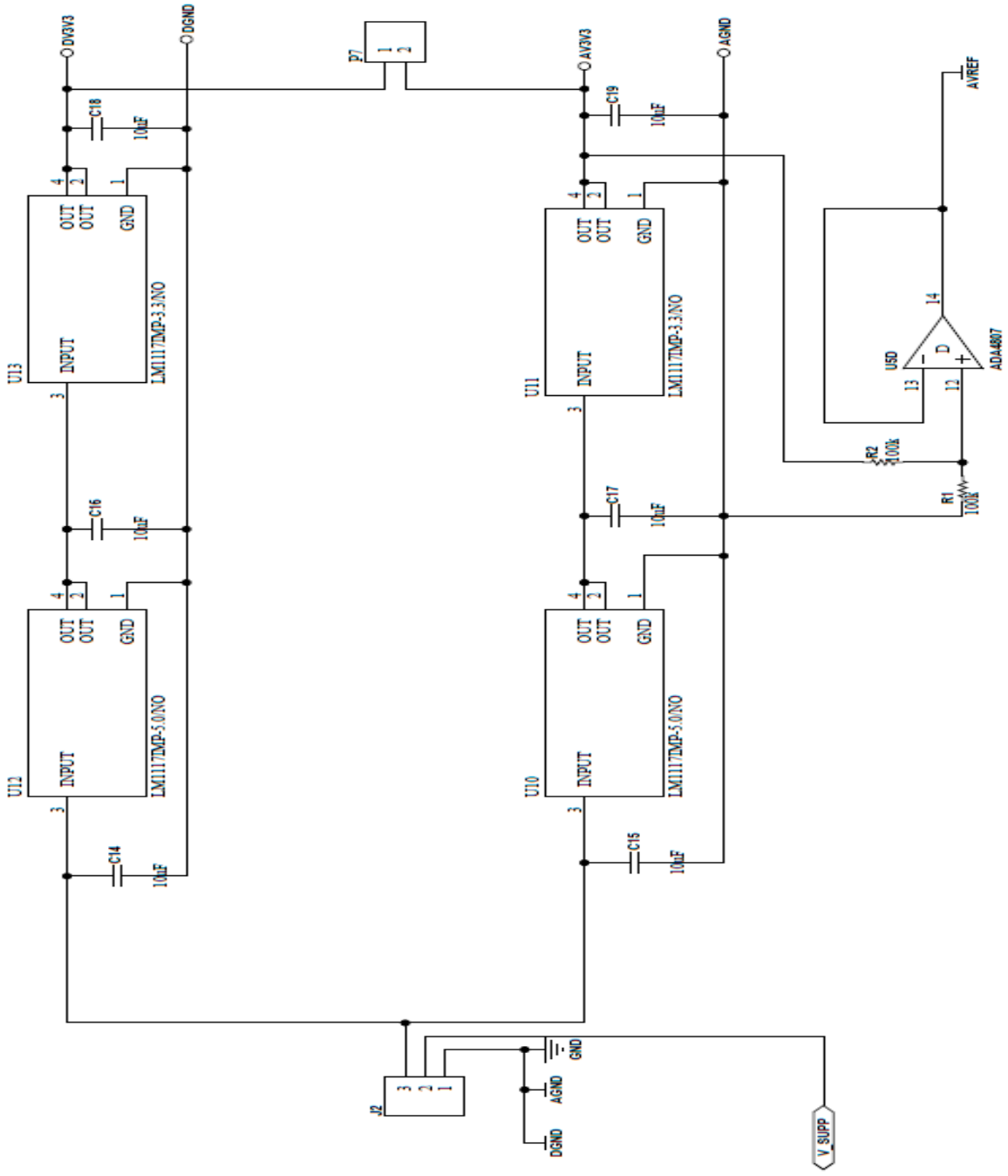


Fig. A.3: ICG schematic sheet 3: Power supply unit

APPENDIX B
PCB LAYOUT

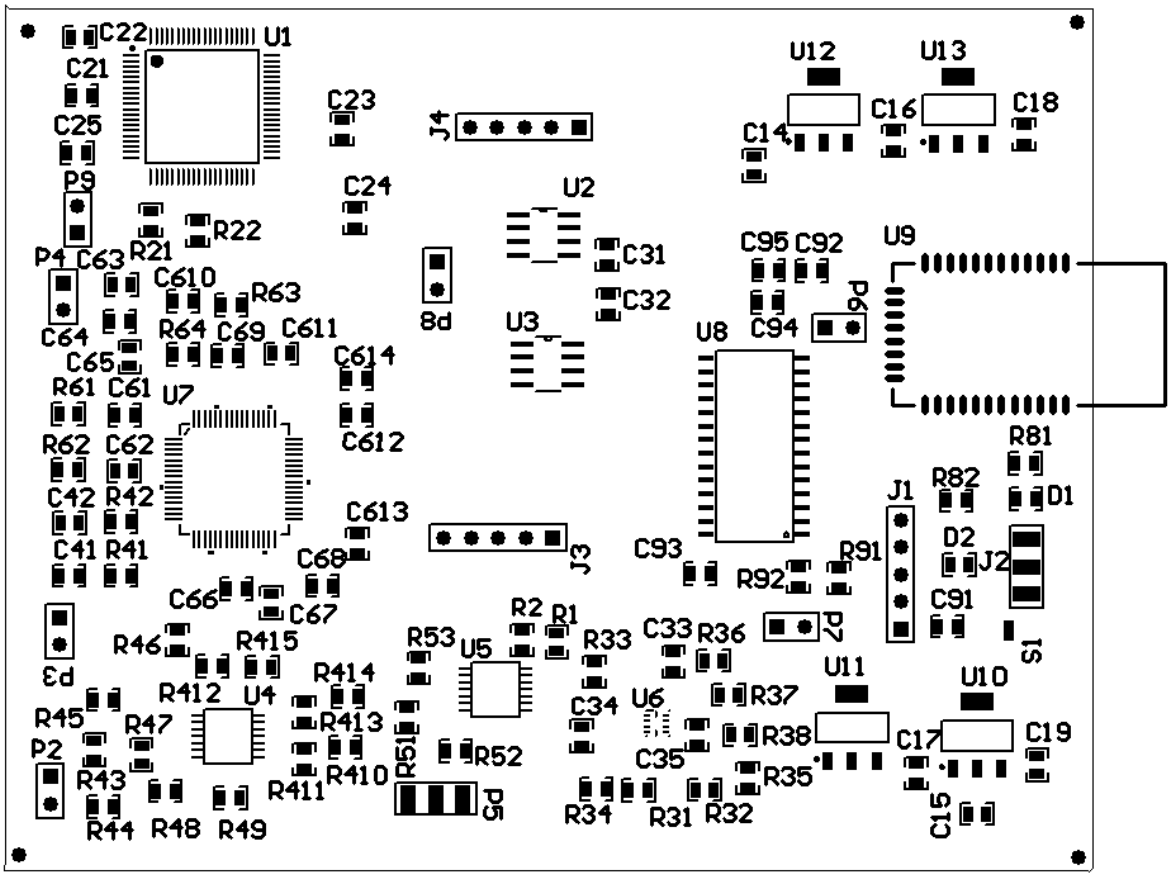


Figure. B.1: Top overlay of the assembled PCB.

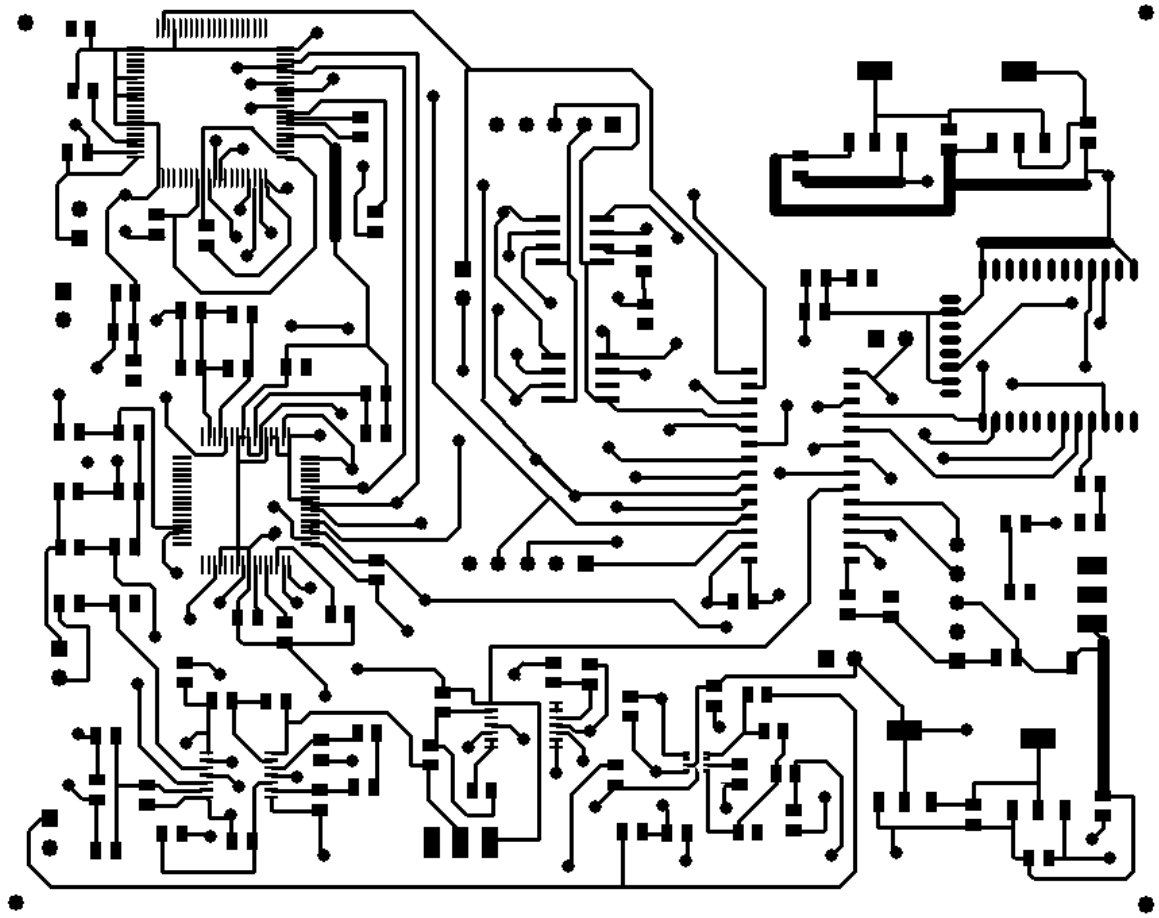


Figure. B.2: Top layer of the assembled PCB.

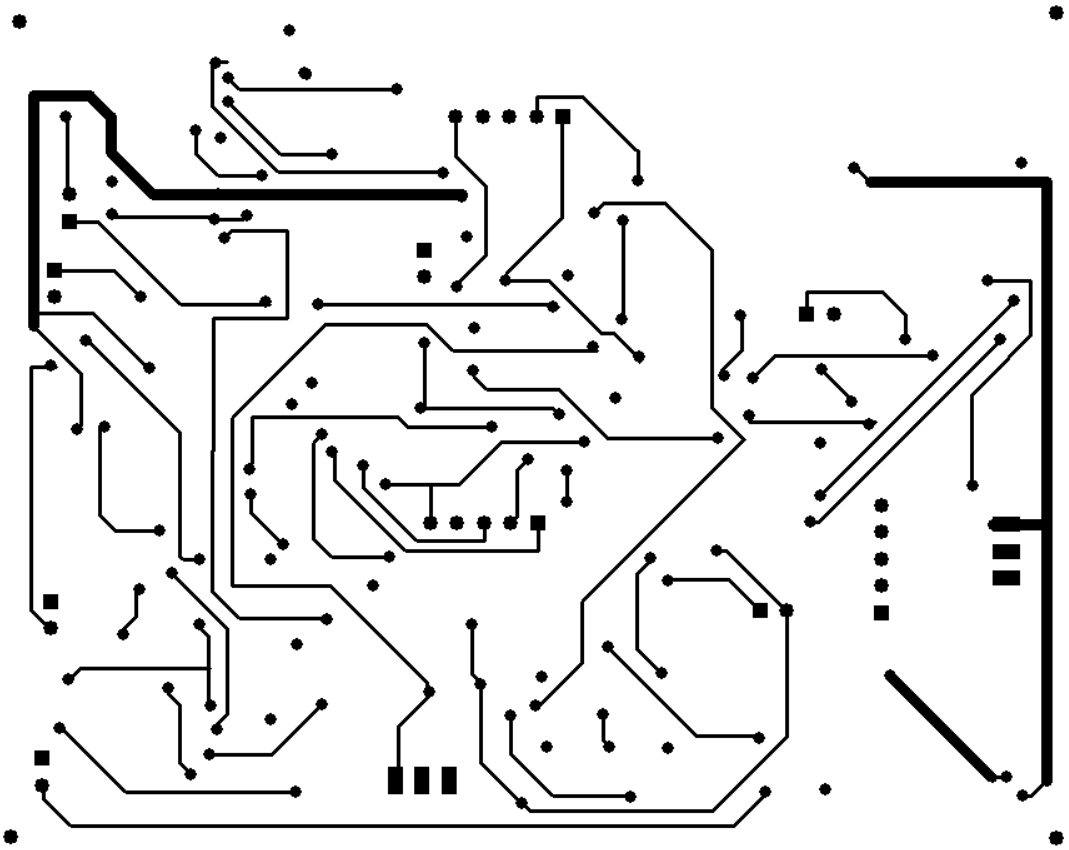


Figure. B.3: Bottom layer of the assembled PCB.

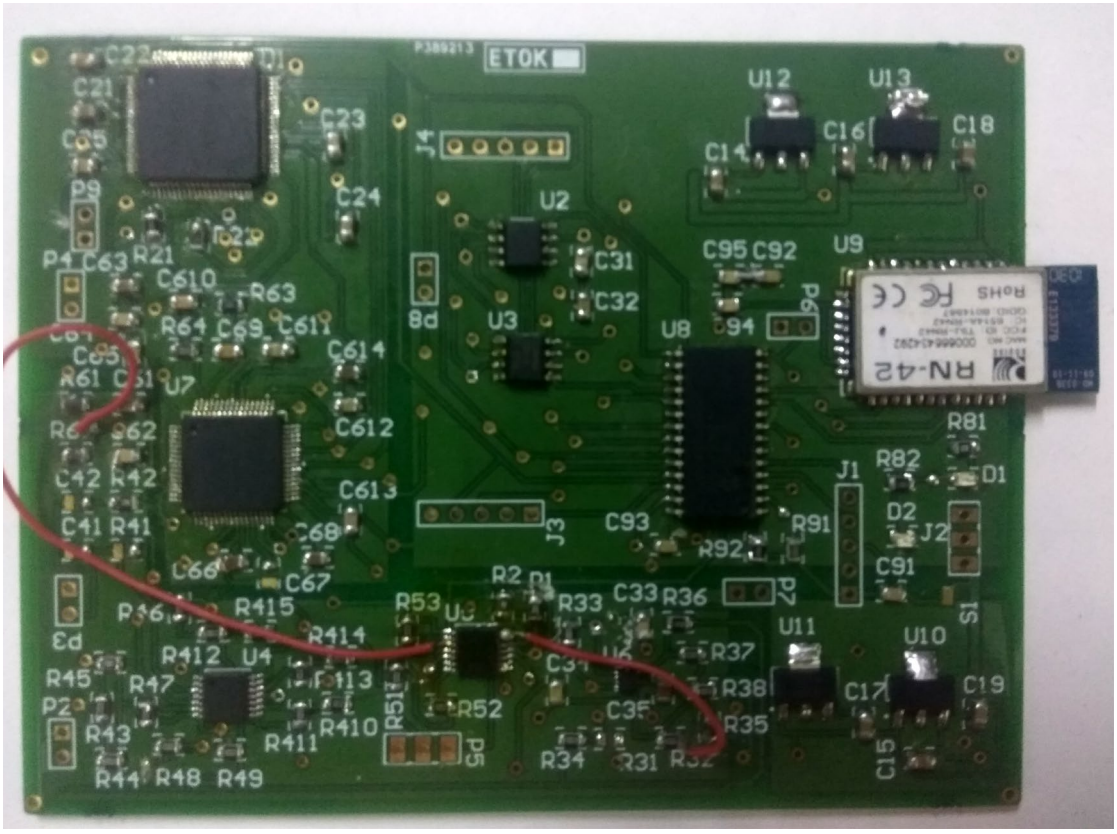


Figure. B.4: Top view of the assembled PCB.

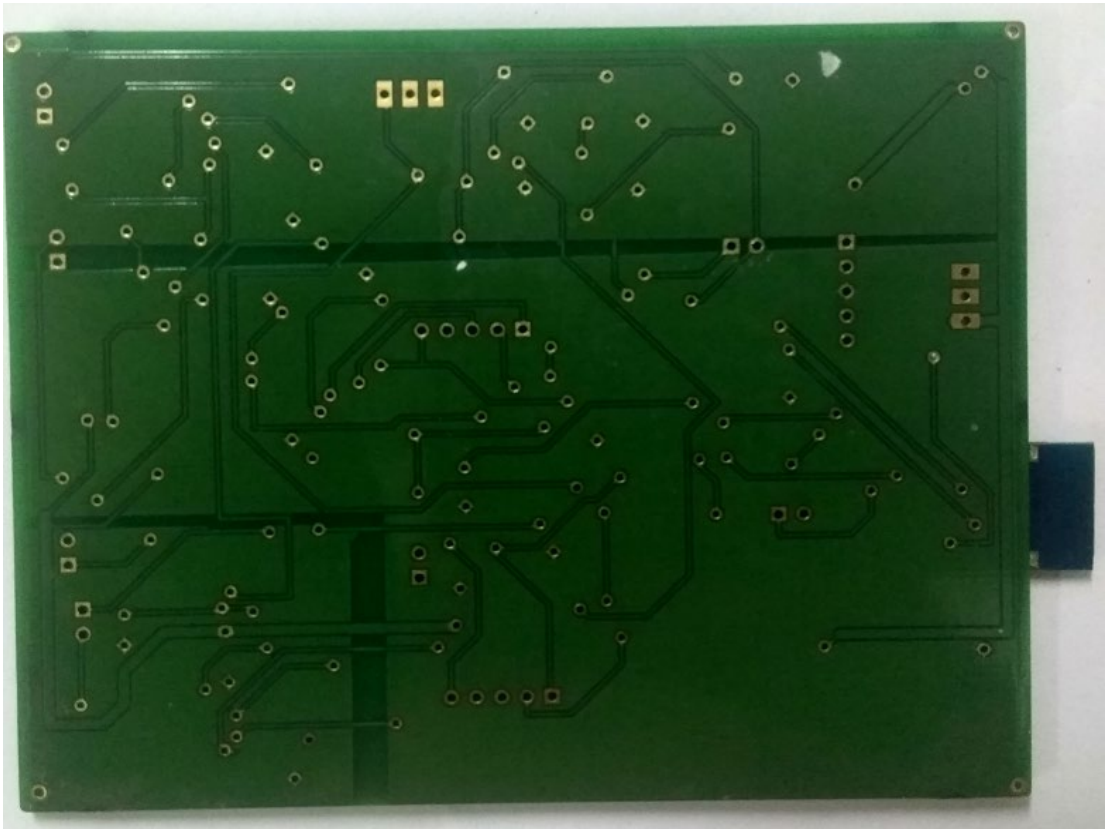


Figure. B.5: Bottom view of the assembled PCB.

APPENDIX C

COMPONENT LIST FOR IMPEDACNE CARDIOGRAPHY HARDWARE

Table C.1. Component list for the impedance cardiography hardware

Component designator	Component description	Part Number / Value	Quantity
R21, R35, R36,R92	0805 resistor	100	4
C21, C22, C25, C31, C32, C33, C34, C35, C61, C62, C64, C65, C69, C91, C92, C93, C94, C95, C611, C612, C613	0805 capacitor	0.1uF	20
C41, C42	0805 capacitor	100pF	2
C69	0805 capacitor	1.8nF	1
C610	0805 capacitor	10nF	1
C67	0805 capacitor	22uF	1
C66, C68, C614	0805 capacitor	1uF	3
C23, C24, C63	0805 capacitor	10uF	3
R31, R32, R34, R33, R37, R38	0805 resistor	100k	6
C610	0805 capacitor	1.5nF	1
R1,R2, R41, R42, R411	0805 resistor	100k	5
R43, R44, R46, R47, R48, R49, R412, R413, R414, R415,R51, R52, R53,R91	0805 resistor	10k	14
R81,R82 R410	0805 resistor	1k	2
R45	0805 resistor	3.3k	1
R61, R62	0805 resistor	39k	2
R64	0805 resistor	100k	1
R22	0805 resistor	572	1
R63	0805 resistor	670k	1
U2, U3	Digital potentiometer	AD8400ARZ10	2
U4, U5	Quad op amp	ADA4807	2
U7	ECG extractor chip	ADS1298PAG64	1
U1	Impedance converter chip	AFE4300PNR	1
C14, C15, C16, C17, C18, C19	0805 capacitor	10 uF	6

J1, J3, J4	Connector 5-pin	DEBUG, SPI-1, SPI-2	3
D1, D2	LED	LED	2
U8	Micro controller	dsPIC33FJ128GP802	1
P2, P3, P4, P6, P7, P8, P9	Connector 2-pin	header_2 pin	7
J2, P5	Connector 3-pin	header_3 pin	2
U11, U13	3.3 V voltage regulator	LM1117IMP-3.3/NO	2
U10, U12	5.0 V voltage regulator	LM1117IMP-5.0/NO	2
U9	Bluetooth module	RN42	1
S1	short_gnd	short_gnd	1
U6	Fully differential op amp	THS4551IRUNR	1

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