A JFET-based Circuit for Realizing a Precision and Linear Floating Voltage-controlled Resistance

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***Abstract*—A JFET-based circuit for realizing a precision and linear floating voltage-controlled resistance (VCR) is presented for use in analog multipliers and programmable analog circuits and as a resistance mirror. It uses a matched JFET pair along with an op amp based negative feedback for realizing a precision resistance and a feedback of the source and drain voltages to the gate for realizing a linear floating resistance. The circuit operation is validated through circuit simulation and practical testing.**

***Keywords*—JFET; programmable analog circuits; self-tracking circuit; voltage-controlled resistance**

I. INTRODUCTION

In many applications such as analog multipliers, modulators, demodulators, volume controllers, and programmable analog circuits, there is need for a voltage-controlled-resistance (VCR). This is often realized using a JFET or a MOSFET with the drain-source resistance controlled by the gate-source voltage [1], [2]. However, it realizes a grounded VCR which acts as a linear resistor for small values of drain-source voltage, typically up to tens of mV. The relationship between the gate-source voltage and the drain-source resistance is dependent on device parameters which may vary with temperature and also may have a significant piece-to-piece variation. For many applications, the resistance of the VCR circuit should remain linear for a terminal voltage much larger than 100 mV. In many programmable analog circuits, it is desirable that neither terminal of the VCR is grounded, i.e. it should act as a floating resistance. For a precision resistance, the effect of temperature-dependent and piece-to-piece variations in the device parameters should be reduced. Several circuits [3] − [12] have been reported which satisfy one or more of the above mentioned requirements but not all.

A JFET-based circuit is presented to realize a precision and linear floating voltage-controlled resistance. The proposed circuit can also be used in applications requiring a resistance mirror, i.e., a resistance whose value is proportional to a variable resistance. It uses a matched JFET pair with an op amp based negative feedback loop for reducing the effect of variations in device parameters in order to realize a precision resistance and a feedback of the source and drain voltages to the gate to realize a floating resistance with extended range of linearity. The circuit operation is validated through circuit simulation and practical testing.

II. CIRCUIT DESCRIPTION

Fig. 1 shows an n-channel JFET used as a grounded VCR with its drain-source resistance controlled by the gate-source voltage. The drain current i_D with the device operating in the triode region can be approximated as the following quadratic function of its gate-source voltage v_{GS} and drain-source voltage v_{DS}:

$$i_D = (2I_{DSS}/V_p^2)((v_{GS} - V_p)v_{DS} - v_{DS}^2/2), \quad V_P \le v_{GS} < 0 \quad \text{and} \quad 0 < v_{DS} < v_{GS} - V_P \tag{1}$$

where V_P is the pinch-off voltage and I_{DSS} is the maximum saturation current [1]. With $k = 2I_{DSS}/V_P^2$, the above equation can be written as

$$i_D = k((v_{GS} - V_p)v_{DS} - v_{DS}^2/2), \quad V_P \le v_{GS} < 0 \quad \text{and} \quad 0 < v_{DS} < v_{GS} - V_P \tag{2}$$

The channel resistance $R_{DS} = v_{DS}/i_D$ is given as

$$R_{DS} = 1/[k(v_{GS} - V_P - v_{DS}/2)] \tag{3}$$

The resistance R_{DS} is linear for $v_{DS} << v_{GS} - V_P$. As the device parameters V_P and I_{DSS} have significant temperature dependence and a large piece-to-piece variation, R_{DS} can have a large variability.

Several VCR circuits [3] – [5] using a combination of transistors operating in the triode and saturation regions have been proposed for eliminating the nonlinearity due to the quadratic term in the expression for the drain current and thereby extending the range of linearity of the resistance. These circuits do not realize a floating resistance and do not provide a precision resistance as they do not eliminate the dependence of the resistance on the device parameters. Another way to cancel the nonlinearity in a grounded VCR is to provide a feedback from drain to gate in which half of the drain voltage is added to the control voltage [6] – [8]. A method for implementing floating voltage-controlled resistors in CMOS technology was proposed in [9] using matched

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transistors for cancellation of the first-order nonlinearities. Extending these approaches, Senani [10] realized a JFET-based floating VCR circuit in which an op amp and five resistors are used to superimpose the mean value of the drain and source voltages on the control voltage to obtain the gate voltage, as shown in Fig. 2. The circuit may be considered to be having "source-drain bootstrapped" gate. Although the circuit realizes a floating VCR with an extended range of linearity, the resistance value is dependent on device parameters and hence the circuit cannot be used in applications requiring a precision VCR.

Fort [11] reported a MOSFET-based VCR circuit with compensation to reduce the variations occurring due to temperature. The circuit does not provide a floating VCR and does not compensate for variation in the resistance values due to change in the terminal voltages. Clarke [12] proposed a set of four VCR circuits using a matched JFET pair and an op amp to realize a grounded resistor whose resistance value is compensated against variations in device parameters using negative feedback. One of the circuits is shown in Fig. 3. It consists of an op amp A1 and two matched n-channel JFETs M1 and M2. Assuming the transistors to be in the triode region, the drain-source resistance of M2 is given as $R_X = (v_{REF}/(-v_C))R_1$. The circuit can be considered as "self-tracking" as it compensates for piece-to-piece and temperature-dependent variations in the device parameters. The circuit can be used as a precision grounded VCR for small terminal voltages.

We combine the approaches of the self-tracking circuit of Clarke [12] and the source-drain-bootstrapped gate circuit of Senani [10] to realize a precision and linear floating VCR, as shown in Fig. 4. The n-channel JFETs Q1 and Q2 are matched transistors, operating in the triode region. Q2 serves as a floating resistor with terminals X and Y. The negative feedback using op amp A1 stabilizes the channel resistance of Q1 against variations in the device parameters. Both transistor gates are controlled by the voltage v_C with feedback of the mean of the respective source and drain voltages: using R_2 and R_3 for Q1 and using A2, R_4, R_5, R_6, R_7, and R_8 for Q2. The feedback of source and drain voltages extends the range of linear behavior.

In the circuit of Fig. 4, the control voltage v_C for the devices Q1 and Q2 is generated through the negative feedback loop consisting of A1 and Q1, keeping the inverting input terminal of A1 at ground. For loop feedback to be negative, the drain and source terminals of Q1 must be as shown in the figure, and therefore $v_2 > 0$ and $v_1 < 0$. The current i_1 through Q1 is given as

$$i_1 = -v_1 / R_1 \tag{4}$$

The gate voltages v_{G1} and v_{G2} are obtained by adding together half of the respective drain and source voltages and v_C, and are given as

$$v_{G1} = (v_C + v_2)/2 \tag{5}$$

$$v_{G2} = (v_C + v_X + v_Y)/2 \tag{6}$$

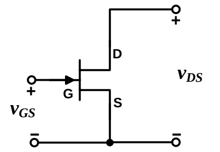

Fig. 1. Grounded VCR using n-channel JFET.

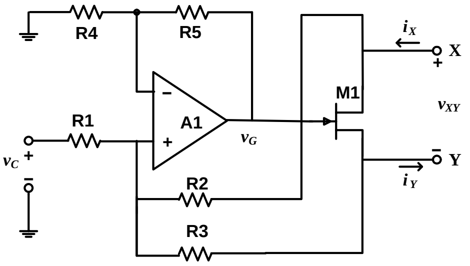

Fig. 2. Floating linear VCR circuit with source-drain bootstrapped gate as proposed by Senani [10]. $R_1 = R_2 = R_3$, $R_4 = 2R_5$.

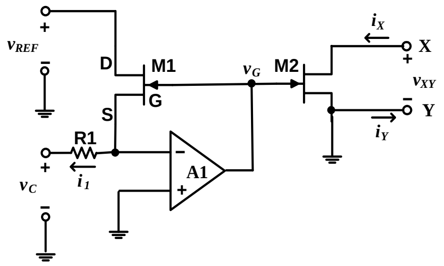

Fig. 3. Self-tracking VCR circuit as proposed by Clarke [12].

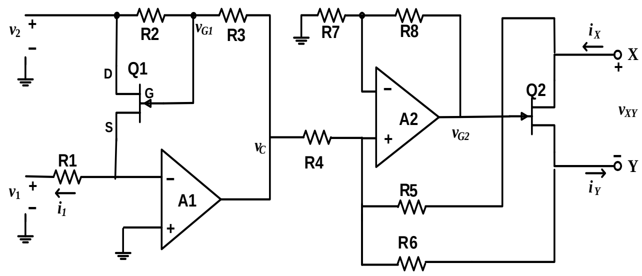

Fig. 4. JFET-based precision and linear floating VCR circuit with source-drain bootstrapped gate and self-tracking. $R_2 = R_3$, $R_4 = R_5 = R_6$, $R_7 = 2R_8$.

The resistances R_5 and R_6 are selected to be large enough to not cause any loading on the terminals X and Y.

Assuming that the voltage v_2 is such that Q1 operates in the triode region, the current i_1, in accordance with (2) is given as

$$i_1 = k_1[(v_{G1} - V_{P1})v_2 - v_2^2/2], \quad 0 \geq v_{G1} \geq V_{P1} \text{ and } v_{G1} - v_2 \geq V_{P1} \tag{7}$$

Using (4), (5), and (7), the control voltage v_C can be written as

$$v_C = 2\left[-v_1/(k_1 R_1 v_2) + V_{P1}\right] \tag{8}$$

For the transistor Q2, the drain current $i_D = i_X = i_Y$ and the drain source voltage $v_{DS} = v_X - v_Y$. Assuming v_X and v_Y to be such that Q2 is in the triode region, the drain current in accordance with (2) is given as

$$i_X = k_2[(v_{G2} - v_Y - V_{P2})(v_X - v_Y) - (v_X - v_Y)^2/2], \quad 0 \ge v_{G2} - v_Y \ge V_{P2} \text{ and } 0 \ge v_{G2} - v_X \ge V_{P2} \tag{9}$$

Using v_{G2} as given in (6), the current i_X can be rewritten as

$$i_X = k_2[(v_C/2 - V_{P2})(v_X - v_Y)], \quad 0 \ge v_C > 2V_{P2} \text{ and } |v_X - v_Y| \le \min(-v_C, v_C - 2V_{P2}) \tag{10}$$

Using the control voltage v_C as given in (8), we can write

$$i_X = k_2\left[\frac{-v_1}{R_1 k_1 v_2} + V_{P1} - V_{P2}\right](v_X - v_Y) \tag{11}$$

For the matched pair of transistors Q1 and Q2, $k_1 = k_2 = k$ and $V_{P1} = V_{P2} = V_P$, and (11) can be rewritten as

$$i_X = (-v_1/v_2)R_1(v_X - v_Y), \quad 0 \ge v_C > 2V_P \text{ and } |v_X - v_Y| \le \min(-v_C, v_C - 2V_P) \tag{12}$$

Therefore the circuit serves as a floating linear VCR, and its value $R_{XY} = (v_X - v_Y)/i_X$ is given as the following:

$$R_{XY} = (v_2/(-v_1))R_1 \tag{13}$$

The control can be exercised by a combination of v_1, v_2, and R_1, with the constraints on their values such that $v_C = 2\left[V_P - v_1/(kR_1 v_2)\right]$ satisfies the condition $0 \ge v_C > 2V_P$ over the range of values of the device parameters V_P and *k*.

The control of the resistance can also be exercised by using a current source as i_1 in place of v_1 and R_1 and thus the circuit can be used to realize a current-controlled resistance. Neither of the terminals X and Y needs to be grounded and therefore the circuit can be used in applications requiring a floating VCR. Another feature of the circuit is that it can be used as a resistance mirror, for controlling resistances across a set of multiple ports using a common control. Such a circuit for providing controlled resistances across two ports is shown in Fig. 5. The proposed circuit can also be realized using a matched MOSFET pair with independent substrates [13].

The proposed circuit has been implemented using U441 (Vishay Siliconix) [14] as the matched pair of n-channel JFETs and LT 1366 (Linear Technology) [15] as the op amps, and its operation has been verified by circuit simulation and practical testing.

III. Simulation Results

A simulation of the proposed circuit using LTspice IV has been carried out for its extensive testing, particularly for examining the effect of variation in device parameters on the value of the controlled resistance. The simulation was carried out using the models of U441 [14] and LT 1366 [15] as matched pair of JFETs and op amps, respectively, and ±15 V supply. The circuit was tested with v_Y kept at zero and varying v_X.

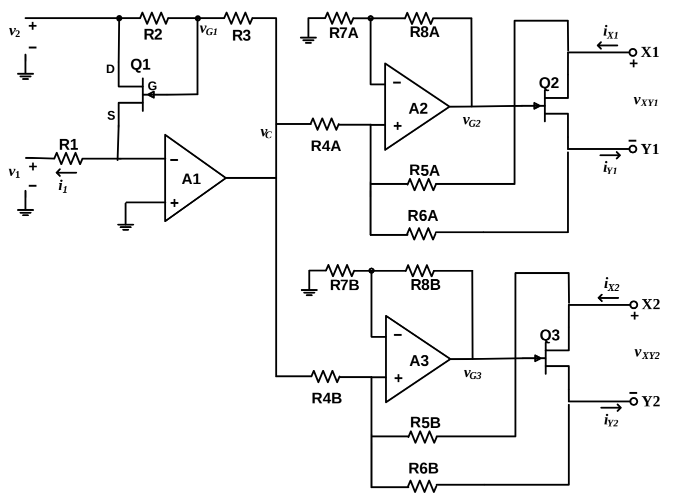

Fig. 5. Resistance mirror circuit for controlling resistances across two ports (X1-Y1, X2-Y2) using a common control. $R_2 = R_3$, $R_{4A} = R_{5A} = R_{6A}$, $R_{7A} = 2R_{8A}$, $R_{4B} = R_{5B} = R_{6B}$, $R_{7B} = 2R_{8B}$. $R_{X1Y1} = R_{X2Y2} = (v_2/(-v_1))\, R_1$.

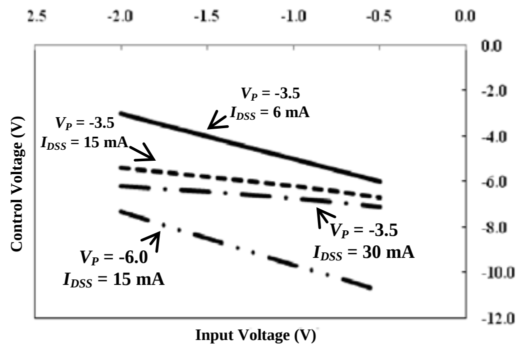

Fig. 6. Control voltage v_C (op amp A1 output) versus input voltage v_1 for different combinations of device parameters V_P and I_{DSS}.

Fig. 6 shows the effect of device parameters V_P and I_{DSS} on the op amp A1 output v_C which serves as the control voltage for both transistors. For a given value of v_1, the negative feedback loop formed by A1 and Q1 adjusts v_C to keep the channel resistance of Q1 constant against the variations in the device parameters.

The device parameters were selected to represent the range of values as given in the datasheet of U441 [14]. Table I shows the effect of variation in device parameters V_P and I_{DSS} and the voltage across the resistance. The values of v_1, R_1, and v_2, were selected as −1.0 V, 1.0 kΩ, and 1.0 V, respectively, resulting in i_1 = 1.0 mA and the set value of R_{XY} as 1.0 kΩ. The voltage v_{XY} was varied from −1 to 1 V. It is seen that as V_P and I_{DSS} are changed, corresponding

Table I. Simulation results for observing the effects of voltage v_{XY} and the device parameters V_P and I_{DSS} on R_{XY}. Circuit parameters: $v_1 = -1$ V, $v_2 = 1.0$ V, and $R_1 = 1.0$ kΩ (i.e. $i_1 = 1.0$ mA and $R_{XY,SET} = 1.0$ kΩ).

v_{XY} (V)	$V_P = -3.5$ V, $I_{DSS} = 15$ mA (Observed: $v_C = -6.21$ V, $v_{G1} = -2.61$ V)		$V_P = -6.0$ V, $I_{DSS} = 15$ mA (Observed: $v_C = -9.67$ V, $v_{G1} = -4.33$ V)		$V_P = -3.5$ V, $I_{DSS} = 6$ mA (Observed: $v_C = -5.01$ V, $v_{G1} = -2.00$ V)	
	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)	v_{G2} (V)	R_{XY} (Ω)
−1.0	−3.61	1000.0	−5.33	1000.0	−3.00	1000.0
−0.8	−3.51	1020.1	−5.23	1020.1	−2.90	1020.1
−0.6	−3.41	1026.2	−5.13	1026.2	−2.80	1026.2
−0.4	−3.31	1032.2	−5.03	1032.2	−2.70	1032.2
−0.2	−3.21	1038.4	−4.93	1038.4	−2.60	1038.4
0.0	−3.11	1044.1	−4.83	1044.1	−2.50	1044.1
0.2	−3.01	1038.4	−4.73	1038.4	−2.40	1038.4
0.4	−2.91	1032.2	−4.63	1032.2	−2.30	1032.2
0.6	−2.81	1026.2	−4.53	1026.2	−2.20	1026.2
0.8	−2.71	1020.1	−4.43	1020.1	−2.10	1020.1
1.0	−2.61	1000.0	−4.33	1000.0	−2.00	1000.0

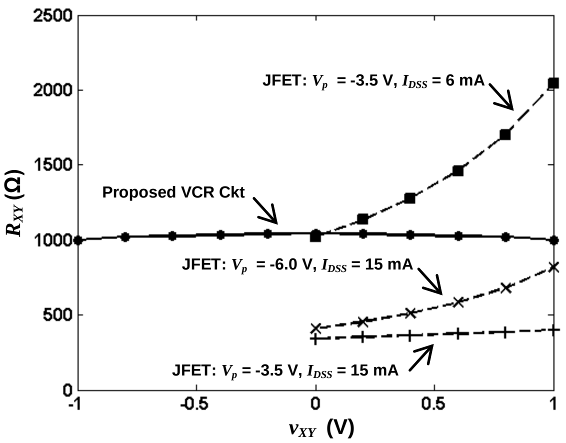

Fig. 7. R_{XY} versus V_{XY} for the proposed VCR circuit ($v_1 = -1$ V, $v_2 =$ 1.0 V, and $R_1 = 1000$ Ω, U441 as the matched JFET pair) and a single JFET ($v_{GS} = -2.5$ V, one JFET from U441).

changes occur in v_C, v_{G1}, and v_{G2}, and R_{XY} remains constant for a given v_X. Thus the simulation results show that the self-tracking feature of the circuit stabilizes R_{XY} against variations in the device parameters. Variation in v_X over $\pm$1 V results in a change in R_{XY} of less than 5%.

Plots of R_{XY} versus v_{XY} for the proposed VCR circuit (Fig. 4) are shown in Fig. 7. The figure also shows the plots for a JFET used as a grounded VCR (Fig. 1). Both sets of plots are for three sets of device parameters as in Table 1. It is seen that R_{XY} of a single device shows a very large variation with v_{XY} while the proposed circuit shows a change of less than 5%. Further R_{XY} for a single device shows a very large variation with changes in device parameters while R_{XY} for the proposed circuit shows no variation, i.e. no dependence on the device parameters.

IV. Experimental Results

For experimental validation, the circuit of Fig. 4 was assembled using n-channel matched JFET pair from U441. The drain characteristics of the JFET were plotted for calculating the device parameters V_P and I_{DSS} and the values for the two devices came out to be $V_{P1} = -2.35$ V, $I_{DSS1} = 4.16$ mA, $V_{P2} = -2.35$ V, $I_{DSS2} = 4.18$ mA. The resistors with following values were used: $R_1 = 1$ kΩ, $R_2 = R_3 = 1$ MΩ, $R_4 = R_5 = R_6 = R_7 = 12$ kΩ, $R_8 = 6$ kΩ (two 12 kΩ in parallel). The resistors used had 5% tolerance. The 12 kΩ resistors had a close match, with measured values of 11.98 − 11.99 kΩ and R_1 had measured value of 998 Ω.

The circuit operation was found to be satisfactory for a wide range of values of input voltages v_1 and v_2 and the terminal voltage v_{XY}. For $v_2 = 1$ V, the values of v_C corresponding to v_1 of −1 V and −0.5 V were −3.68 and −4.85 V, respectively. For $v_1 = -1$ V, R_{XY} had a mean value of 1033 Ω and varied from −2.7% to 2.0%, for variation of v_{XY} over ± 1 V. For $v_1 = -0.5$ V, the corresponding mean value was 2039 Ω and the variation was from −4.2% to 2.2%. Thus the experimental results show satisfactory operation of the circuit for terminal voltage of up to ±1 V, with the variation in the resistance with v_{XY} being within 5% as shown by the simulation results.

V. Conclusion

A circuit using matched JFET pair has been presented for realizing a precision and linear floating voltage-controlled resistance. It combines the approaches of a self-tracking circuit to compensate for variations in the device parameters and source-drain bootstrapped gate for extending the range of linearity and realizing a floating resistance. The operation of the circuit as a floating linear VCR has been validated using simulation and practical testing. The resistance value is proportional to the product of a physical resistance and a voltage ratio. Therefore it can be used to realize a time-varying resistance with a very flexible set of controls. It can also be used as a current-controlled resistance or as a resistance mirror for controlling resistances across a set of multiple ports using a common control. The voltage range of operation of the JFET-based circuit is limited because of the requirement of the gate-channel junction remaining reverse biased. This can be relaxed by realizing the circuit using a matched MOSFET pair, with the two devices in the pair having independent substrates and additional circuit used for keeping the source-substrate voltages as zero. An IC version of the circuit using a small number of devices for realizing the two op amps and on-chip resistances needs to be designed and tested.

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