SYNTHESIS OF ANALOG CIRCUITS EMPLOYING CURRENT-MODE BUILDING BLOCKS

Thesis

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by

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Abstract

The circuits using current-mode building blocks have received considerable attention in many filtering and signal processing applications. Compared to their voltage-mode counterparts, the current-mode building blocks are attractive because of their wider bandwidth, higher slew rate, and lower power consumption. As a large number of op-amp based circuits with elegant realization procedures are already available, it is worthwhile to convert them into the circuits based on current-mode building blocks. The initial contribution of the thesis deals with the transformation technique for converting a class of voltage-mode analog circuits into the current-mode analog circuits without requiring any additional circuit elements and change in the circuit topology. For fabrication as integrated circuits, it is desirable to have circuit topologies with equal-valued grounded capacitors. The major contribution of the thesis is, therefore, focused towards the development of synthesis procedures for realizing analog circuits like filters, equalizers, oscillators using current-mode building blocks such as current conveyor, current feedback amplifier, four terminal floating nullor, current differencing buffered amplifier, operational transresistance amplifier, using (i) equal-valued grounded capacitors and (ii) minimal number of active and passive elements.

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List of Symbols

$A(f)$	differential gain of the op-amp
$A_v(f)$	voltage gain of the circuit
A_0	DC gain of the op-amp
$D(\omega)$	group delay
f	frequency, in Hz
f_0	3-dB cutoff frequency
G	(i) circuit gain, (ii) conductance
$H(s)$	transfer function
K	gain constant
Q	Quality factor
R_m	transresistance
R_0	reference resistance
$T(s)$	system transfer function
Y	admittance
Z	(i) impedance, (ii) transfer impedance
Z_{in}	input impedance
Z_0	transfer impedance at zero frequency
ϵ	dielectric constant
$\theta(\omega)$	phase angle
ω	angular frequency, in rad/sec
ω_n	normalized frequency
ω_0	pole frequency, in rad/sec

List of Abbreviations

AE	Amplitude equalizer
BLO	Bridged-ladder oscillator
BPF	Band-pass filter
BW	Bandwidth
CC	Current conveyor
CDBA	Current differencing buffered amplifier
CFA	Current feedback amplifier
CFOA	Current feedback operational amplifier
CM	Current-mode
DPA	Driving point admittance
EVGC	Equal-valued grounded-capacitor
FTFN	Four terminal floating nullor
GIC	Generalized impedance converter
HPF	High-pass filter
IC	Integrated circuit
LPF	Low-pass filter
NIC	Negative impedance converter
OA	Operational amplifier
OTA	Operational transconductance amplifier
OTRA	Operational transresistance amplifier
TTO	Twin-T oscillator
VM	Voltage-mode

Chapter 1

INTRODUCTION

A large number of analog circuits using voltage-mode (VM) building blocks such as operational amplifiers (op-amps, or OAs) have already been developed with elegant realization procedures [1]-[3]. As compared to VM building blocks, the current-mode (CM) building blocks can generally operate with low voltages and have higher bandwidth and slew rate [4], [5]. In CM building blocks, the output is controlled by the input current. The analog circuits using such CM building blocks have simple topologies and are suitable for integrated circuit (IC) technology. Due to the availability of the CM building blocks, the synthesis of analog circuits using these building blocks have received renewed attention [6]-[8]. The above limitations of VM analog circuits can be overcome by using the following techniques.

(i) *Current mode operation*: In the circuits operating in voltage mode, the floating voltages can be summed simply by connecting them in series. However, summing voltage signals having a common terminal requires additional circuitry. In the circuits operating in current mode, summing of current signals requires only a node. The current signals can be easily replicated and scaled using current mirrors. This reduces the complexity of the circuit operating in current mode as compared to that operating in voltage mode.

(ii) *CM building blocks*: The CM building blocks have higher bandwidth and slew rate as compared to VM building blocks. They can operate with low voltages and hence the circuits employing CM building blocks are suitable for IC technology.

(iii) *Grounded capacitor realization*: Grounded-capacitors allow easy compensa-

tion for the parasitic capacitors, latter being in parallel with the grounded capacitors [9]. For thin film fabrication, the use of grounded capacitors eliminates the etching process and reduces the number of gold contacts, thereby leading to a greater circuit reliability [10].

(iv) *Equal-valued capacitor realization*: Equal-valued grounded capacitors help saving silicon area and easy processing in IC technology [6], [11], [12] (pp. 10-12), [13]-[15]. For low frequency applications, equal-valued grounded-capacitor (EVGC) realization would facilitate time-multiplexing of the capacitors and thereby reducing the area on the silicon wafer [16]. If all the driving point impedances in EVGC realization of ladder networks are realized in *RC* Foster II form, then these impedances will have minimum total capacitance [17].

The major thrust undertaken in this direction is, therefore, focused towards the development of synthesis techniques for realizing analog circuits using CM building blocks, and using equal-valued grounded capacitors and minimum number of active and passive elements.

The various CM building blocks are described in the next section. As a large number of OA based VM circuits have already been developed, and because of the advantages of CM operation, it is worthwhile to convert the VM circuits into CM circuits. Section 1.2 discusses the various available VM-to-CM transformation techniques. In IC technology, it is desirable to operate circuits at low voltages which can be achieved by using CM building blocks. Section 1.3 describes the synthesis of some of the analog circuits employing CM building blocks. Finally, the chapter outlines the research objectives and the work presented in the subsequent chapters of the thesis.

1.1 CM building blocks

Some of the CM building blocks are current conveyor (CC), current feedback amplifier (CFA), four terminal floating nullor (FTFN), current differencing buffered amplifier (CDBA), and operational transresistance amplifier (OTRA). These are briefly described here.

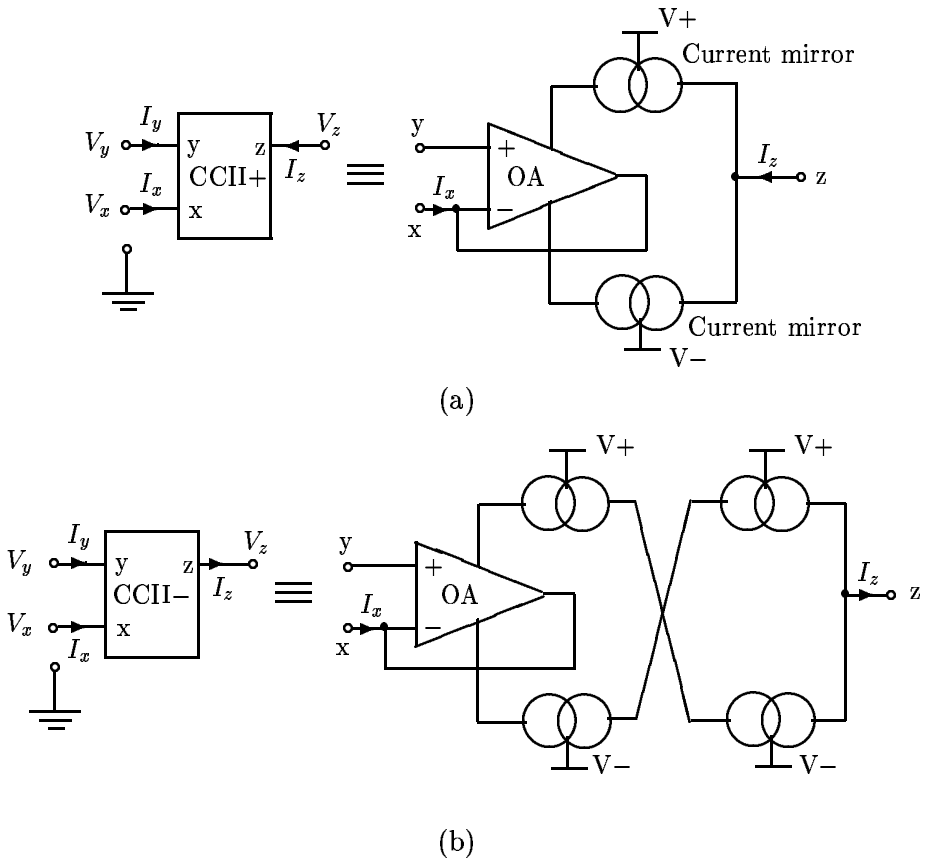


Fig. 1.1. Block representation and model of (a) CCII+ and (b) CCII−.

1.1.1 Current conveyor

The CM building block known as the first generation of current conveyor (CCI), introduced by Smith and Sedra [18], has the following terminal characteristics:

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix}. \tag{1.1}$$

The second generation of current conveyor (CCII) [19], introduced by the same authors, has the following terminal characteristics:

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix}. \tag{1.2}$$

Fig. 1.1 shows the block representation and a model of CCII [20], [21]. The output current $I_z = \pm I_x$. If the sign is '+' ('−'), the conveyor is termed as CCII+ (CCII−).

By convention, the '+' sign is taken to mean I_x and I_z both flowing simultaneously into or out of the conveyor. The current I_z either may be the same as I_x or it may be produced by the copy of the input voltage V_y, from terminal y, acting across the impedance connected at x input. CCII− can be realized from CCII+ by using a pair of current mirrors, crosscoupled to produce a phase inversion [21].

1.1.2 Current feedback amplifier

The terminal characteristics of the current feedback amplifier (CFA) also known as current feedback operational amplifier (CFOA) are

$$\begin{bmatrix} V_x \\ I_y \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ I_w \end{bmatrix}. \tag{1.3}$$

The block representation of CFA, a model of CFA, and a model of practical CFA are shown in Fig. 1.2. There is a buffer between the noninverting input terminal y and the inverting input terminal x as shown in Fig. 1.2(b). In the model of practical CFA as can be seen from Fig. 1.2(c), there is a nonzero input resistance R_x at the input terminal x and on the output side, there is a current-controlled voltage source of the strength ZI_x where Z is the forward dynamic transfer impedance, or transfer impedance, of the device (modeled as the parallel combination of R_T and C_T) and I_x is the current flowing out of the inverting input terminal. Thus, for an ideal CFA, $R_x = 0$ and $Z = \infty$. The CFA was introduced by Analog Devices as early as in 1984. Due to its internal architecture being a cascade of a CCII+ followed by a buffer, it could be used to realise not only CCII+ and CCII− [22], [23] but also as versatile 4-terminal device in its own right.

The CFA is available in commercial form as IC AD844. The different gain-bandwidth characteristic of an OA and CFA based circuits can be appreciated by analyzing the non-inverting amplifier [24], realized using an OA in Fig. 1.3(a) and using a CFA in Fig. 1.3(b).

The gain of the OA based circuit shown in Fig. 1.3(a) is given by

$$A_v(f) = \frac{V_o}{V_i} = \frac{G}{1 + G/A(f)} \tag{1.4}$$

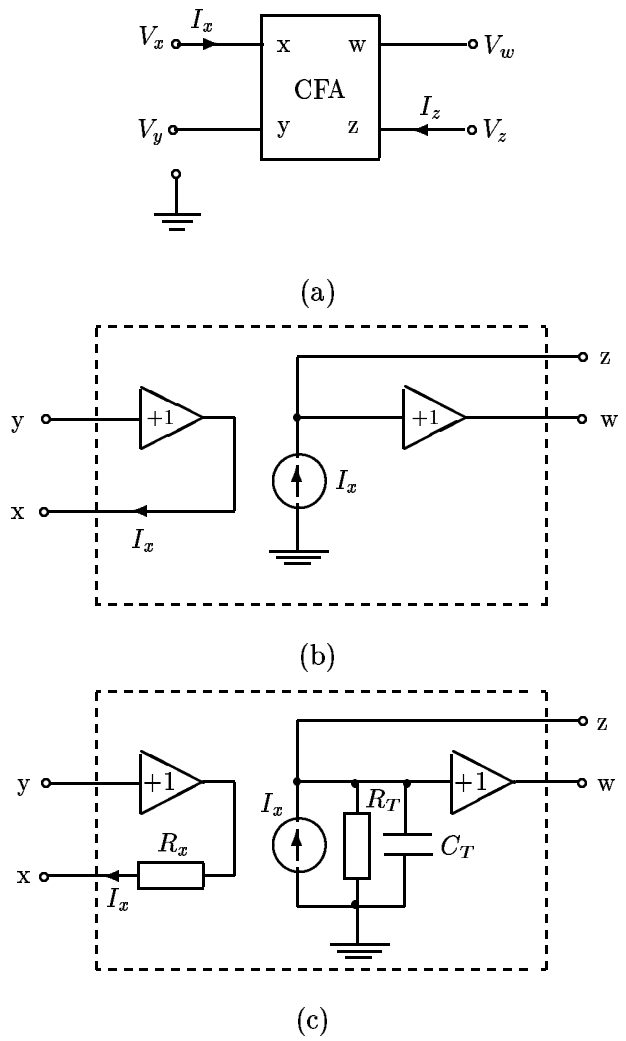


Fig. 1.2. (a) Block representation of CFA, (b) model of CFA, and (c) model of practical CFA.

where $G = 1 + R_f/R_g$ and $A(f)$ is the differential gain of OA. Let us take the single-pole model of the gain $A(f)$ as

$$A(f) = \frac{V_o}{V_e} = \frac{A_0}{1 + jf/f_0} \tag{1.5}$$

where V_e is the potential difference between the two input terminals of the OA, A_0 is the DC gain, and f_0 is the 3-dB cutoff frequency. The voltage gain of the circuit is given as

$$A_v(f) = \frac{G}{1 + (G/A_0) + jf/(A_0 f_0/G)}. \tag{1.6}$$

For $A_0 >> G$, the voltage gain is given as

$$A_v(f) \approx \frac{G}{1 + jf/(A_0 f_0/G)}. \tag{1.7}$$

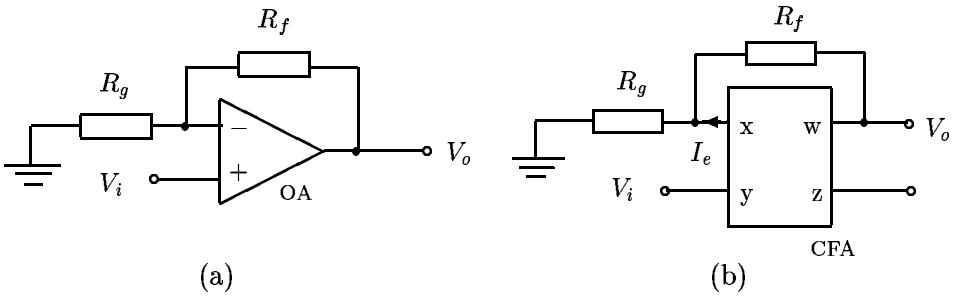


Fig. 1.3. Realization of non-inverting amplifier using (a) OA and (b) CFA.

Thus $A_v(0) \approx G$ and the bandwidth (BW) is given by

$$\text{BW} = A_0 f_0 / G. \tag{1.8}$$

We see that, BW and A_v both depend on G and hence cannot be controlled independently.

The gain of the CFA based circuit shown in Fig. 1.3(b) is given by

$$A_v(f) = \frac{V_o}{V_i} = \frac{G}{1 + (R_f + GR_x)/Z(f)}. \tag{1.9}$$

where $G = 1 + R_f/R_g$ and $Z(f)$ is the transfer impedance of the CFA. Let us take the first order model of $Z(f)$ as

$$Z(f) = \frac{V_o}{I_e} = \frac{Z_0}{1 + jf/f_0} \tag{1.10}$$

where I_e = the error current coming out of the inverting input, $Z_0 \approx R_T$ is the transfer resistance, and $f_0 = 1/2\pi R_T C_T$. The voltage gain can be written as

$$A_v(f) = \frac{G}{1 + [(R_f + GR_x)/R_T](1 + jf/f_0)}. \tag{1.11}$$

For $R_T >> R_f + GR_x$, the voltage gain can be written as

$$A_v(f) \approx \frac{G}{1 + jf/[R_T f_0/(R_f + GR_x)]}. \tag{1.12}$$

Thus, $A_v(0) \approx G$ and the BW is given by

$$\text{BW} = \frac{R_T f_0}{R_f + GR_x}. \tag{1.13}$$

If $R_x << (R_f/G)$, the BW becomes

$$\text{BW} \approx R_T f_0 / R_f. \tag{1.14}$$

As BW is independent of R_g, and if G is controlled by R_g rather than R_f, large G and BW can simultaneously be achieved [5], [24], [25].

More differences between OA and CFA will be apparent after going through their internal structures as shown in Fig. 1.4. The input stage of the OA as can be seen from Fig. 1.4(a) is a difference amplifier. Because of the symmetry in the input stage and as the transistors Q1 and Q2 are matched, the input offset voltage will be minimum. In case of CFA structure shown in Fig. 1.4(b), transistors Q1 and Q3 need to be matched with transistors Q4 and Q2, respectively, for having minimum input offset voltage. Here, since two pairs of transistors need to be matched, the input offset voltage may not be as minimum as that of OA based one. In CFA structure, the slew rate is determined by the rate at which the set of transistors Q3 and Q4 can charge the compensation capacitors C_c. The current that can be sourced is dynamic and is not limited to any fixed value as is often the case in OA structure. The CFA structure with the dynamic current leads to a high slew rate. Thus, a CFA can be used in applications that require bandwidth independent of gain and high slew rate.

1.1.3 Four terminal floating nullor

The port relations of the four terminal floating nullor (FTFN) are characterized by

$$\begin{bmatrix} V_x \\ I_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 \end{bmatrix} \begin{bmatrix} V_y \\ V_z \\ V_w \\ I_w \end{bmatrix}. \tag{1.15}$$

The '+' and '−' signs of the I_z denote plus- and minus-type FTFNs. The 'floating' is used here to define that no current is internally flowing from the port and the current and voltage of the port are not internally dependent on the common mode voltage of the port [26]. Fig. 1.5 shows a possible implementation of an FTFN using OA and CFA [27]-[29].

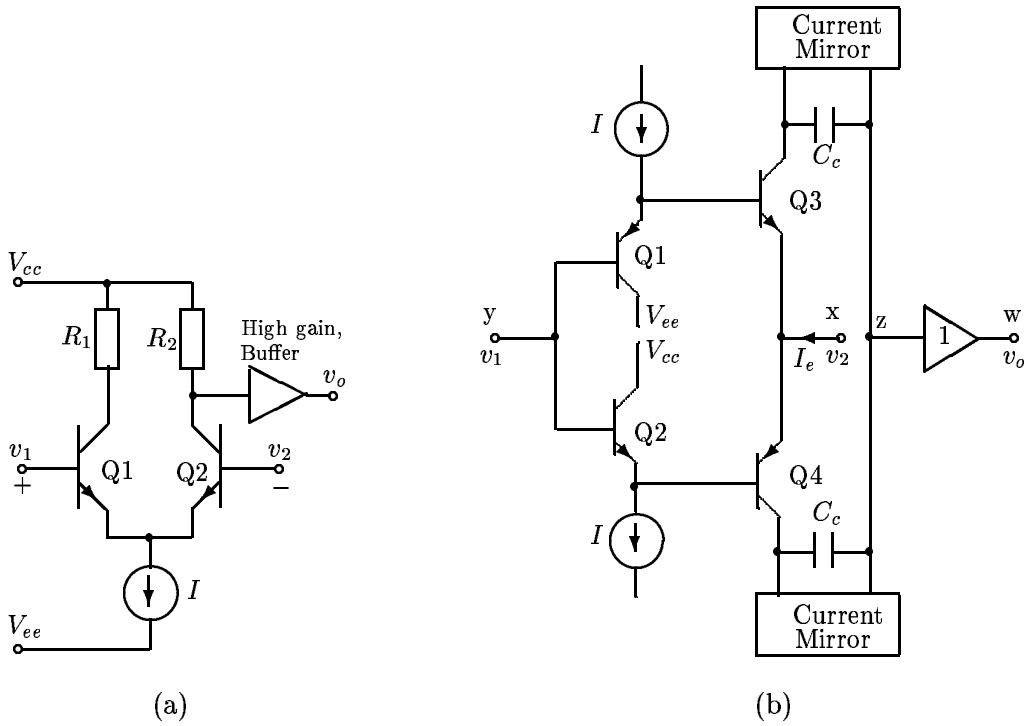


Fig. 1.4. Basic structure of (a) OA and (b) CFA [5].

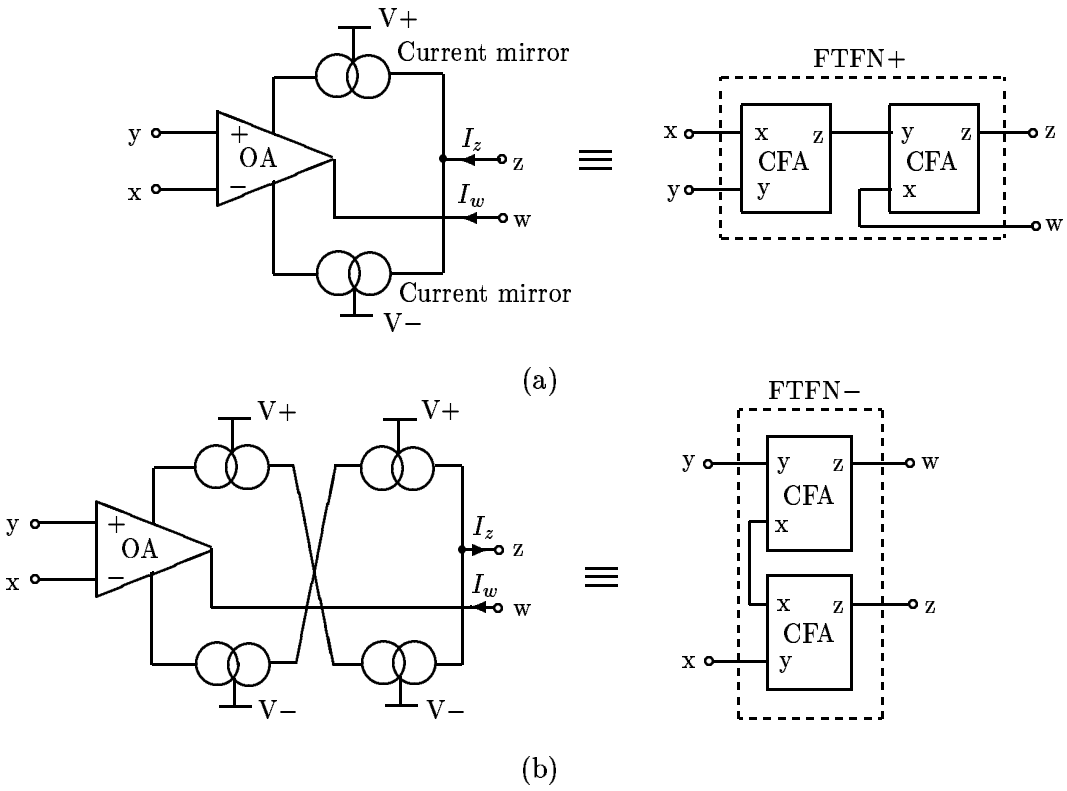


Fig. 1.5. OA and CFA based implimentation of (a) FTFN+ [29] and (b) FTFN− [27], [28].

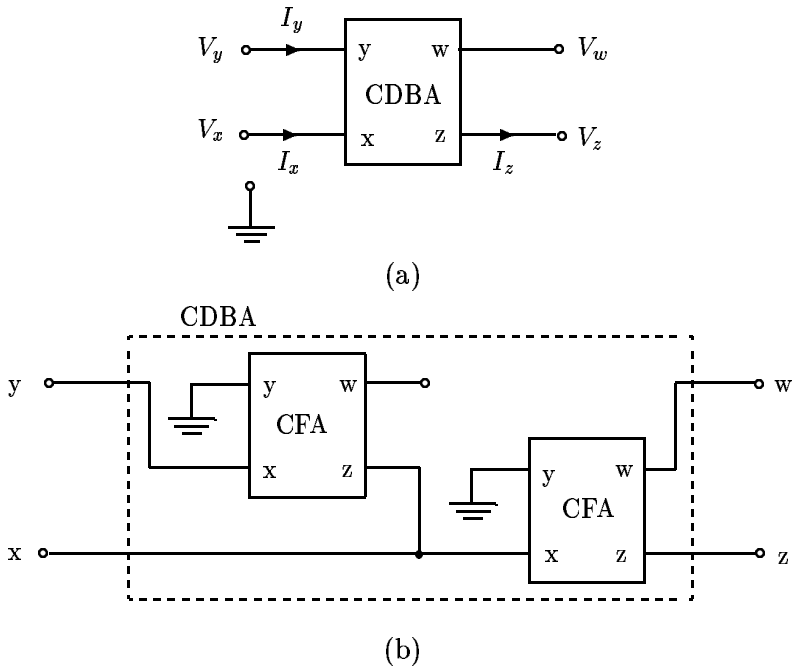


Fig. 1.6. (a) Block representation of CDBA and (b) implimentation of CDBA using CFA.

1.1.4 Current differencing buffered amplifier

The terminal characteristics of the current differencing buffered amplifier (CDBA) are [30]

$$\begin{bmatrix} V_x \\ V_y \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ I_y \\ V_z \\ I_w \end{bmatrix}. \tag{1.16}$$

The block representation of CDBA and its implimentation using CFA are shown in Fig. 1.6. As the input terminals are internally grounded, the circuits using CDBA becomes insensitive to the stray capacitances [30].

1.1.5 Operational transresistance amplifier

Operational transresistance amplifier (OTRA) is a high gain current-input, voltage-output device. The operation of the OTRA is characterized by

$$\begin{bmatrix} V_x \\ V_y \\ V_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ -R_m & R_m & 0 \end{bmatrix} \begin{bmatrix} I_x \\ I_y \\ I_z \end{bmatrix} \tag{1.17}$$

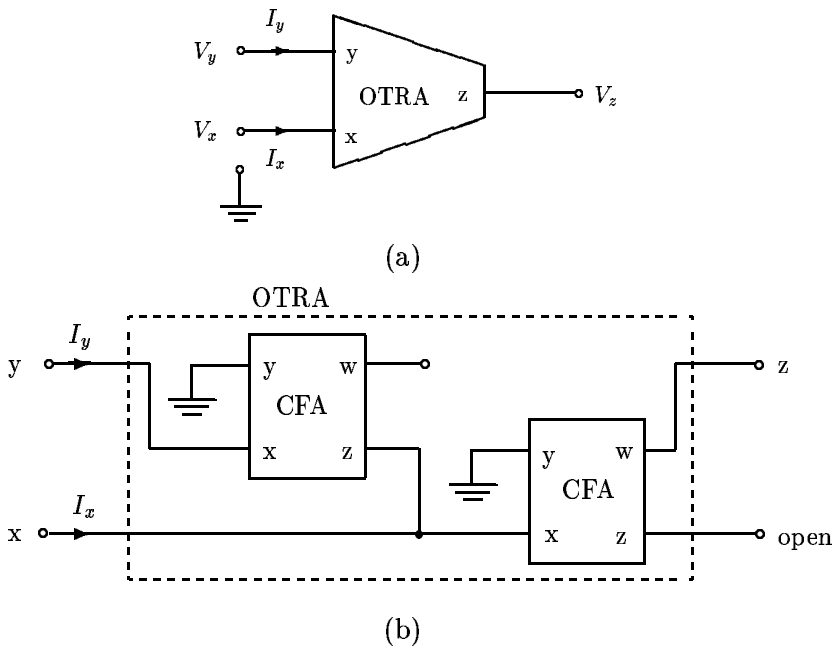


Fig. 1.7. (a) Block representation of an OTRA and (b) implimentation of an OTRA using CFA.

where R_m is the transresistance of OTRA. Fig. 1.7 shows the block representation of OTRA and its implimentation using CFA [30], [31]. For ideal operation, the R_m approaches infinity forcing the input currents to be equal. There are certain disadvantages in using commercially available devices under the name of Norton amplifier as they do not provide internal ground at the input port and have unilateral current flow. The former disadvantage limits the functionality of the OTRA whereas the latter forces the use of external DC bias current leading to a complex design [32], [33]. The CMOS realization of OTRA [31] is obtained from that of a CDBA [34] by open circuiting its z terminal and taking its w terminal as the output z terminal. Both input and output terminals of CMOS OTRA are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The input terminals are internally grounded leading to circuits which are insensitive to the stray capacitances [35].

1.2 VM-to-CM transformation techniques

In a VM network, a voltage is applied as the input and the output is the open circuit voltage. In case of CM networks, a current is applied as the input and the output is

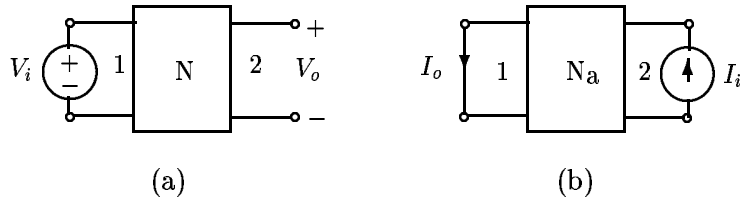


Fig. 1.8. Network N and N_a are inter-reciprocal when $\frac{V_o}{V_i} = \frac{I_o}{I_i}$.

the short circuit current. The process by which the voltage transfer function of a VM network can be made same as the current transfer function of a CM network is known as VM-to-CM transformation. Due to the advantages of CM building blocks, it is worthwhile to convert the already available large number of OA based VM circuits into CM circuits. The various VM-to-CM transformation techniques already available are discussed here.

Robert and Sedra [36] proposed the VM-to-CM transformation using 'adjoint network' concept. A network is considered reciprocal when the same input-output transfer function results as the excitation and the response are interchanged. Although not all the networks possess this reciprocal behaviour, given a network N, a corresponding network N_a, referred to as the adjoint network, can be created such that when the excitation and response of network N are interchanged and network N is replaced by network N_a as shown in Fig. 1.8, the input-output transfer function remains the same. The two networks N and N_a are said to be inter-reciprocal to one another [37]. Reciprocal networks are, by definition, inter-reciprocal with themselves [36]-[40]. Robert and Sedra have presented a set of inter-reciprocal pairs of some basic active building blocks as shown in Fig. 1.9 [36], [39], [41].

The following are the steps involved in transformation of a VM circuit to a corresponding CM circuit as shown in Fig. 1.8 using adjoint blocks.

1. Replace each block of the VM circuit by its corresponding adjoint block.
2. Input voltage source at port 1 is replaced by a short circuit, and the current through this short circuit is the output current of the CM circuit.
3. A current source is connected to port 2 to act as an input for the CM circuit.

Hereafter, steps 2 and 3 together will be referred, for convenience, as "input-output source replacement". Following the above steps, the Lovering circuit [42] shown in

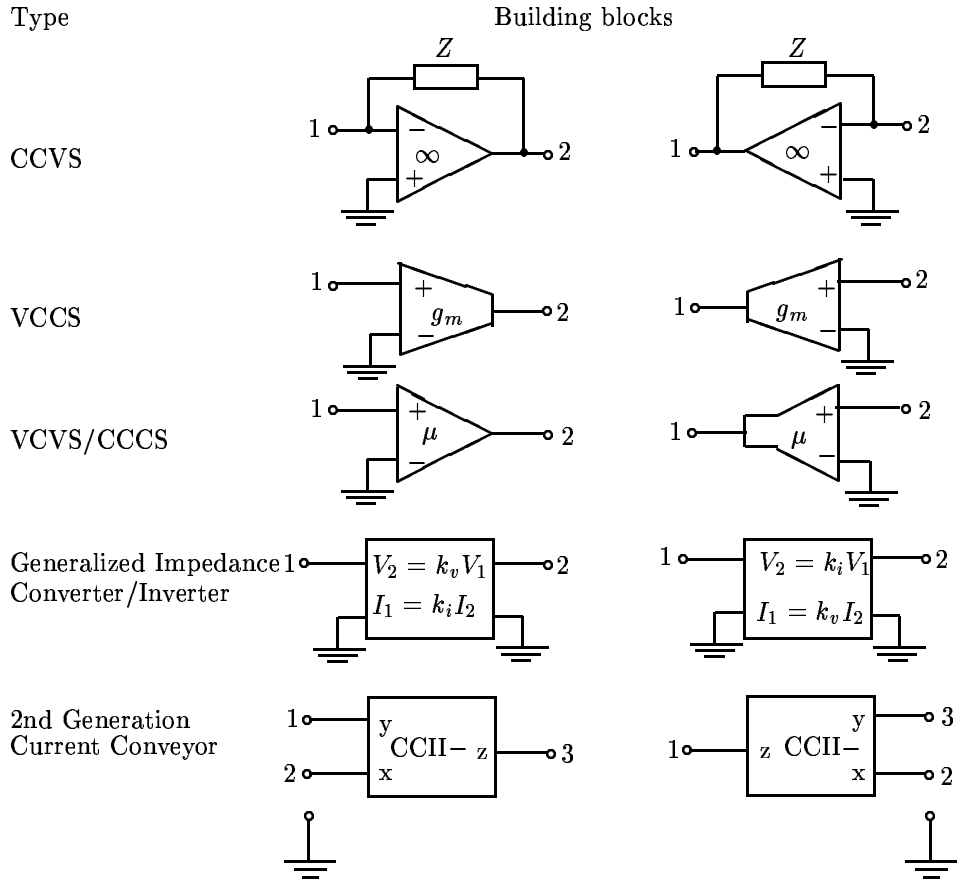


Fig. 1.9. Inter-reciprocal active circuit building blocks.

Fig. 1.10(a) is transformed into the CM circuit as shown in Fig. 1.10(b). Here, the adjoint of a given network is obtained using identical circuit components. The voltage and the current transfer function of the circuits shown in Fig. 1.10 are identical and are given by

$$T(s) = \frac{V_o}{V_i} = \frac{I_o}{I_i} = \frac{Y_a Y_c - Y_b Y_e}{Y_b Y_d - Y_c Y_f}. \tag{1.18}$$

Carlosena and Moschytz [43] proposed the VM-to-CM transformation using nullators and norators. The steps involved are as the following:

1. Replace each controlled source by its nullator-norator equivalent.
2. Interchange nullator and norator of each controlled source.
3. Perform the input-output source replacement.
4. Finally, replace each nullator-norator pair by a corresponding OA.

The short circuit current transfer function of the resulting circuit is then exactly the same as the open circuit voltage transfer function of the original circuit. Let us

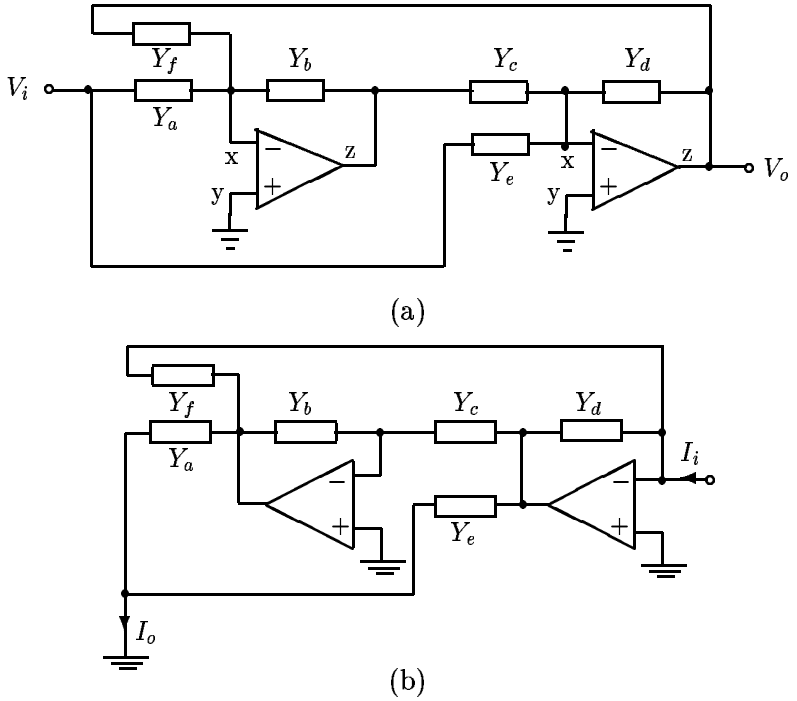


Fig. 1.10. (a) Lovering circuit in VM and (b) transformed Lovering circuit in CM.

consider the Lovering circuit shown in Fig. 1.10(a). Following the above steps, the CM circuit obtained using nullator-norator is shown in Fig. 1.11. Finally, replacing each nullator-norator pair by a corresponding OA, the CM circuit can be obtained which will be same as that of Fig. 1.10(b).

Aronhime and Lata [44] proposed another method of OA based VM-to-CM transformation, with the following steps:

1. Remove the input admittances (set to infinity).
2. The cascadable CM circuits are obtained by adding admittances from the output of each OA to the virtual ground input of the next circuit.

Although the authors have used the virtual ground terminal to achieve cascadable CM circuits, these admittances can be connected directly to ground in case of CM circuits. Thus, the Lovering circuit in VM shown in Fig. 1.10(a) can be converted into its CM counterpart as shown in Fig. 1.12. The virtual ground input of the next circuit is represented by a dashed line in Fig. 1.12. The current transfer function of the circuit shown in Fig. 1.12 is

$$T(s) = \frac{I_o}{I_i} = \frac{Y_c Y_h - Y_d Y_g}{Y_b Y_d - Y_c Y_f}. \tag{1.19}$$

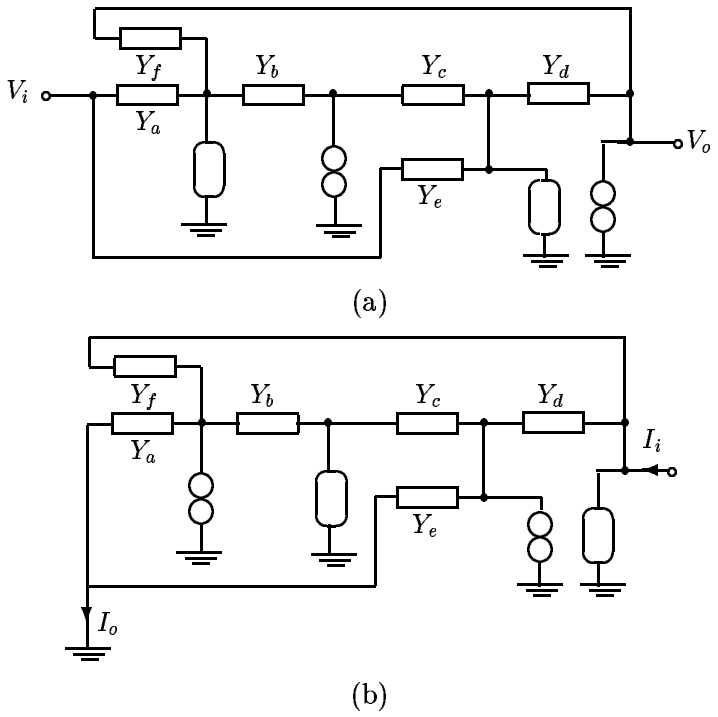


Fig. 1.11. Carlosena-Moschytz transformation of the Lovering circuit of Fig. 1.10(a): (a) step 1- nullator-norator equivalent of controlled sources and (b) step 2- nullator-norator interchange.

Here, the current transfer function obtained is not the same as the voltage transfer function given by (1.18). One possibility that the two become equal is when $Y_h = Y_a$ and $Y_g = \frac{Y_b Y_e}{Y_d}$ provided Y_g is realizable as a driving point admittance. It is possible that Y_g may not be realizable at all, or not realizable by the similar elements alone. As an example, let us consider the realization of all-pass transfer function $T(s) = \frac{V_o}{V_i} = \frac{s^2 - s + 1}{s^2 + s + 1}$, using Lovering's configuration [1] (p. 478) with $Y_a = \frac{3s}{s+1}$, $Y_e = Y_f = s + 1$, $Y_d = \frac{s}{s+1}$, and $Y_b = Y_c = 1$, all of which can be realized by *RC* elements alone. Applying Aronhime-Lata method, the CM circuit will have $Y_h = Y_a = \frac{3s}{s+1}$ and $Y_g = \frac{s^2 + 2s + 1}{s}$. Thus, the topology of the CM circuit obtained by this transformation method is not the same as that of the VM one, and it may require different passive elements.

Uzunhisarcikli and Alci [45] used a nullor (nullator-norator) model for each active element to transform OA based VM circuits into CC and FTFN based CM circuits. Following are the steps involved in transforming the former category.

1. Replace the OA with feedback element by the CC equivalent circuit.
2. Replace each CC by its nullor equivalent.

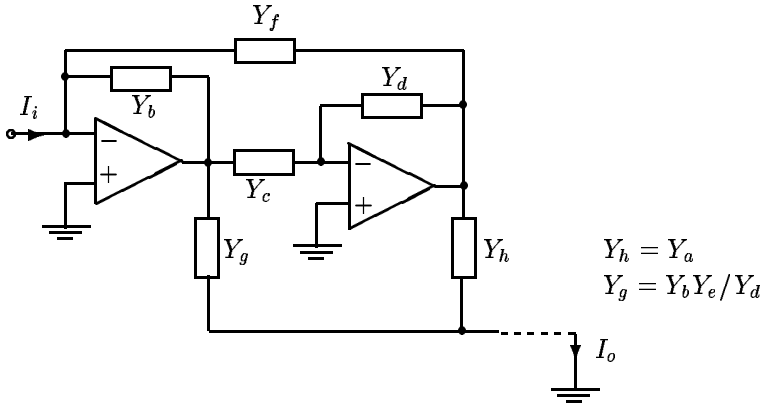


Fig. 1.12. CM transformation, using Aronhime-Lata method [44], of the circuit shown in Fig. 1.10(a).

3. Interchange the nullators and norators of each CC.
4. Perform the input-output source replacement.
5. Replace nullators and norators back to CCs to get the CM circuit.

Following the above steps, the VM Lovering circuit shown in Fig. 1.10(a) is converted into a corresponding CM circuit as shown in Fig. 1.13. Each OA with feedback element has been replaced by its CC equivalent [46], [47], [48] followed by a buffer. Comparison of Figs. 1.13(a) and (d) shows that the transformation can simply be obtained by interchanging CCII+ and CCII− and terminals y-z. However, the transformation method requires CCs double the number of OAs in the original circuit.

Following are the steps involved in transformation of OA based VM circuits into FTFN based CM circuits using Uzunhisarcikli-Alci method [45].

1. Replace each of the OAs in the VM circuit by nullor equivalents.
2. Interchange the nullators and norators of each OA.
3. Perform the input-output source replacement.
4. Replace nullators and norators by their FTFN structure to get the CM circuit.

The CM Lovering circuit obtained, after applying the above steps to the VM Lovering circuit of Fig. 1.10(a), is shown in Fig. 1.14. Here, the steps involving the transformation of OA based circuit into nullor equivalent circuits are not shown as they are similar to that of shown in Fig. 1.11. The transformation method is similar to that given by Carlosena and Moschytz [43] except that the OA has been replaced by FTFN.

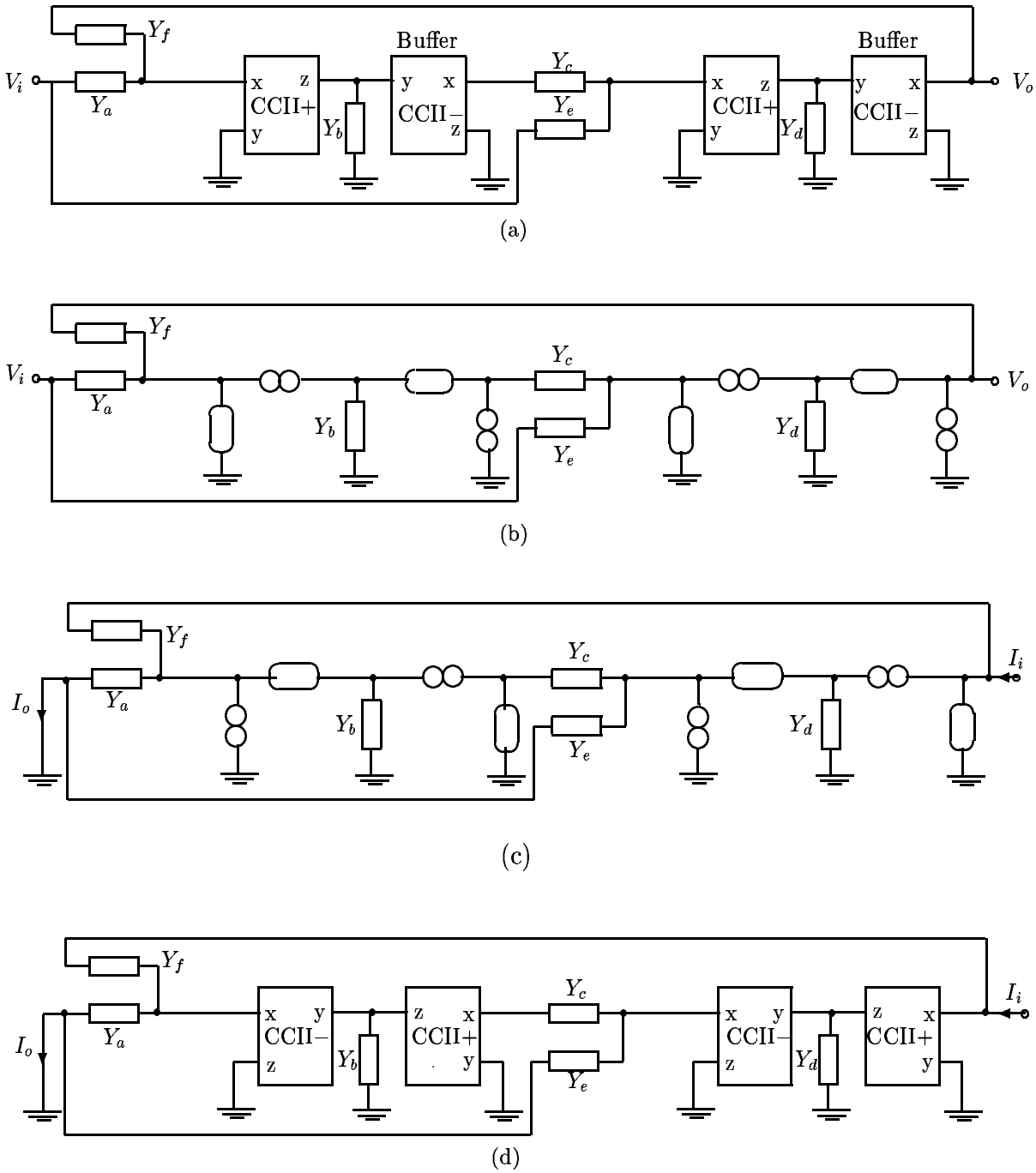


Fig. 1.13. The circuit transformation using Uzunhisarcikli-Alci method [45].

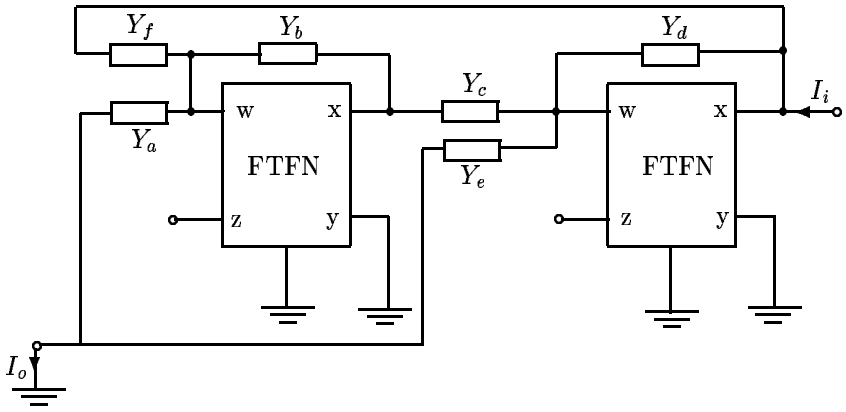


Fig. 1.14. FTFN based CM Lovering circuit obtained using Uzunhisarcikli-Alci method [45].

The above VM-to-CM transformations require the replacement of OAs by either OAs without change in passive elements through their adjoints [37] or nullor models [43] or by CCs and FTFNs [45]. The Aronhime-Lata method [44] requires additional elements. A systematic VM-to-CM transformation method without requiring any additional elements has been proposed in Chapter 2.

1.3 Analog circuits employing CM building blocks

The analog circuits based on CM building blocks have wider bandwidth, higher slew rate, and lower power consumption compared to their VM counterparts [21]. FTFN [27], [28], [49]-[53], CC [23], [54]-[56], and CFA [57]-[64] based CM circuits have received considerable attention in many filtering and signal processing applications. The CFA based circuits offer the special advantage of high slew rate and bandwidth independent of closed loop gain [5], [24], [25]. The various difficulties and limitations associated with the synthesis of analog circuits such as filters, equalizers, and oscillators are discussed here.

1.3.1 Filters

Since inductors are not preferred in IC technology, several methods have been proposed to realize the inductorless filters [1], [3]. *RC* symmetrical lattice realization [65], [66] requires a large number of elements. Unsymmetrical *RC* lattice realization

[67] yields minimum number of capacitors and all grounded capacitors. However, 3-terminal (of which one terminal is grounded) realizations are preferred in practice. Such realizations of transfer functions with positive real zeros are not possible with RC elements alone, whereas functions with complex zeros in the right half plane require increasingly large number of elements with decreasing imaginary part of these zeros because of the polynomial augmentation [68]-[71]. Therefore an extensive research has been carried out in the area of active RC realizations. For several decades, the OA realizations dominated over those employing negative resistance, finite gain amplifiers, gyrator, and negative impedance converters, due to their excellent performance and low sensitivity [1]. However, they are unsuitable for high frequency applications due to the restriction of constant gain bandwidth product and slew rate limitation [21]. Many new acitve devices have been proposed to extend the frequency range of operation. The OTRA has attracted considerable attention due to the developments in the CM analog circuits [27], [49]-[51]. There are certain disadvantages in using the commercially available OTRAs as they do not provide internal ground at the input port and have a unilateral current flow. However, several high performance CMOS OTRAs have been developed which overcome these disadvantages. Acar and Ozoguz's procedure [30], based on signal flow graph, realizes any nth order transfer function, but it requires $(n+1)$ active elements. Salama and Soliman's procedure [32] requires two active elements to realize second order universal filters. The method by Chen *et al.* [72] requires three and four active elements to realize second and third order universal filters, respectively. Thus, circuit realization of the transfer function using these procedures require a large number of active devices.

RLC ladder filters have been used as prototypes to derive OA based RC active filters [3], [73], OTA (operational transconductance amplifier) based continuous-time filters [4], [11], [74], and switched-capacitor filters [75], [76]. Doubly-terminated RLC filters share all the low sensitivity characteristics and low component spread of the RLC prototype. They are also reported to be suitable for monolithic integrated filters [77]. The CM circuits offer potential advantages for applications in both the continuous-time and sampled-data signal processings [6], [78]-[84]. CM filters have received a wide attention due to their wide bandwidth, low voltage operation, and simple implementation of signal operations such as addition and subtraction [4], [6].

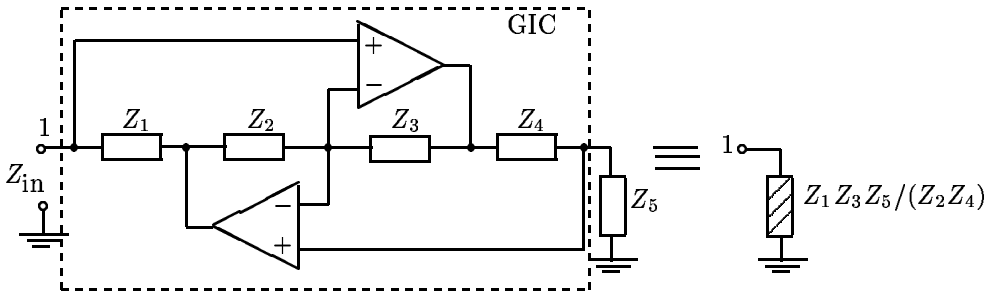


Fig. 1.15. Active circuit equivalent to grounded inductor.

Usually two approaches are in vogue for a ladder simulation: element simulation and functional relation simulation. In the former approach [3], each inductor is replaced by its active simulation using active devices such as generalized impedance converter (GIC). A grounded inductor can be replaced by the circuit as shown in Fig. 1.15 [3], [85]. The analysis of the circuit leads to

$$Z_{in} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}. \tag{1.20}$$

By choosing $Z_x = R_x$ ($x = 1, 2, 3, 5$) and $Z_4 = 1/sC_4$, (1.20) becomes

$$Z_{in}(s) = s\left(C_4 \frac{R_1 R_3}{R_2}\right) R_5 \equiv sL. \tag{1.21}$$

Alternatively, by choosing $Z_x = R_x$ ($x = 1, 3, 4, 5$) and $Z_2 = 1/sC_2$, (1.20) becomes

$$Z_{in}(s) = s\left(C_2 \frac{R_1 R_3}{R_4}\right) R_5 \equiv sL. \tag{1.22}$$

Two GICs can be connected back to back with an impedance in the center as shown in Fig. 1.16 to realize the floating impedance [3], [85]. From Figs. 1.15 and 1.16, we see that a large number of active devices are required for simulating grounded and floating inductors using element simulation approach.

Most of the synthesis methods using OTAs for simulating high-order LC ladder filters involve either a complicated design procedure or a large number of OTAs [77]. In such OTA based ladder filter simulations [4], [77], it is possible to have all the capacitors of equal value and grounded, but they impose a practical difficulty in tuning the transductance of each OTA. A single FTFN circuit [86] can yield all capacitors grounded, but the capacitors may not necessarily be of equal value. Further, it is restricted to the transfer functions with negative real poles. The signal flow graph

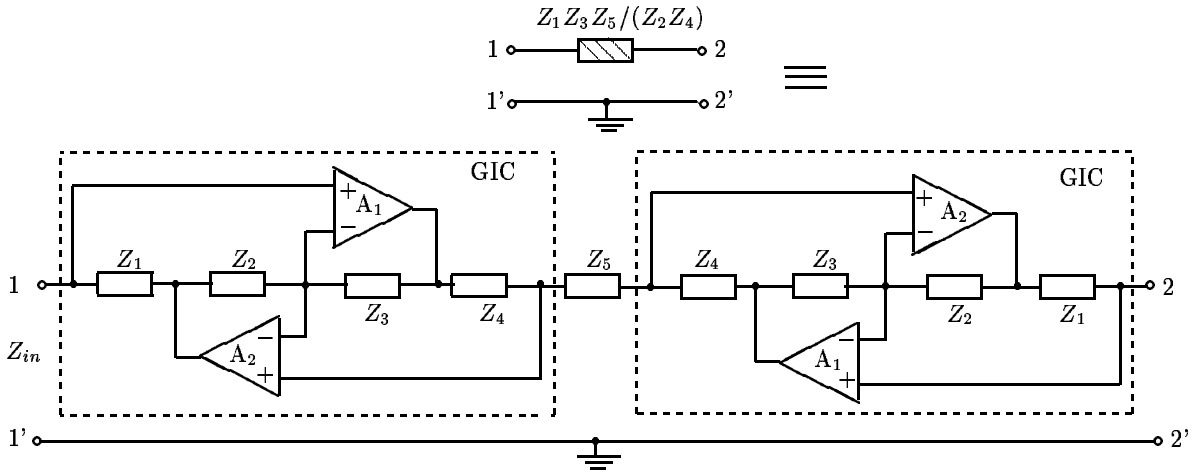


Fig. 1.16. Active circuit equivalent to floating inductor.

technique of Biolek and Biolkova [87] for ladder filter simulation using CDBA does not lead to a simulation with all capacitors grounded. The current mirror array based technique [88] for LC prototype filter simulation can yield all capacitors grounded, but they may not be of equal value. The method of Tangsrirat *et al.* [89] is restricted to certain types of series and shunt branches. Thus, the topologies developed for the ladder filter realization are either restricted to certain types of series and shunt branches and/or they are not suitable for IC technology.

1.3.2 Amplitude equalizers

The amplitude equalizers are used in many systems to compensate for the deviations produced in the loss-gain response. Bode [90] introduced the amplitude equalizers using only passive elements and having the transfer function of the form

$$T(s) = \frac{1 + xH(s)}{x + H(s)} \tag{1.23}$$

where x is a function of variable resistor R_v and has no dimension. The R_v is the only variable resistor. From (1.23), the following properties are noted here.

(i) As x varies from 0 to ∞, $T(s)$ varies from $\frac{1}{H(s)}$ to $H(s)$. The "whole range" is defined as a difference in the values of the variable resistance R_v when $T(s) = H(s)$ and $T(s) = \frac{1}{H(s)}$. Thus, the whole range is [0, ∞].

(ii) When x is replaced by $\frac{1}{x}$, $T(s)$ becomes $\frac{1}{T(s)}$. Hence, one has to consider the realization of $T(s)$ or $\frac{1}{T(s)}$.

(iii) When $H(s)$ is replaced by $\frac{1}{H(s)}$, $T(s)$ becomes $\frac{1}{T(s)}$.

(iv) The x and $H(s)$ are interchangeable.

(v) A flat response, $T(s) = 1$, is obtained when $x = 1$.

The amplitude equalizer by Saraga and Zyoute [91] requires 2 OA, one for negative impedance converter (NIC) and one for buffer to avoid loading. It has whole range of $[0, \infty]$ and $H(s) = \frac{Z}{Z + R_0}$, where R_0 is a reference resistance. Brglez [92] developed another NIC based amplitude equalizer that requires 2 OAs and $H(s) = \frac{R_0}{Z + R_0}$ with whole range of $[0, 2R_0]$. Later, Brglez [93] has replaced the NIC by a switch. In this amplitude equalizer, the toggling of the switch is required to provide positive and negative range of R_v. Zyoute [94] proposed a single OA amplitude equalizer with zero output impedance, $H(s) = \frac{Z}{Z + 2R_0}$, and whole range of $[0, \infty]$. A practical resistor cannot have such a wide range. Talkhan *et al.* [95] modified the component values in Zyoute's amplitude equalizer to bring down the whole range to $[0, R_0]$. The resulting circuit has $H(s) = \frac{Z}{Z + R_0}$. All these amplitude equalizers do not accomodate the desired $H(s)$. Nowrouzian and Fuller [96] proposed an amplitude equalizer which can realize any specified RC realizable $H(s)$ such as $\frac{R_0 + Z}{R_0 - Z}$ at the cost of an increase in the number of circuit components (5 OAs, 14 resistors). The whole range is $[0, \infty]$. Later, Nowrouzian *et al.* [97] proposed an amplitude equalizer with a smaller number of OAs and resistors (3 OAs, 11 resistors). The amplitude equalizer has $H(s) = \frac{2Z}{2Z + R_0}$ and whole range of [0, ∞]. None of these circuits can realize specified values for both the whole range and the value of variable resistor at which the flat response is required.

1.3.3 Oscillators

A large number of oscillator circuits have been reported in the past and some of them can be used for sensor applications [98], [99]. Circuits using CM building blocks can be devised to have independent control for condition of oscillation and frequency of oscillation and also for extending the frequency range of operation.

1.4 Research objectives

This research is aimed at *developing novel synthesis techniques for realizing analog circuits such as filters, equalizers, and oscillators employing CM building blocks and the circuit topologies suitable for IC technology.* The various CM building blocks that have been used are CC, CFA, FTFN, CDBA, and OTRA. In most of the work, there is an emphasis on realizing the circuits with a small number of active and passive elements and equal-valued grounded capacitors, which are important from suitability for integration point of view [6], [11]-[15], [100], [101].

First the various difficulties associated with OA based VM circuits in achieving better frequency response and the circuit topologies suitable for IC technology are studied. Subsequently the synthesis techniques using CM building blocks have been developed for realizing the analog circuits with a small number of active and passive elements and grounded equal-valued capacitors.

The simple design procedures for realizing amplitude equalizers and oscillator based sensor circuits employing CM building blocks are developed. The design procedure of realizing amplitude equalizers helps accommodating both the specified whole range and value of variable resistor at which the flat response is required. The design procedure of realizing oscillator based sensor circuits helps in easier controls such as frequency tuning.

1.5 Thesis organization

Chapter 2 deals with a systematic procedure for transforming VM circuits based on OA, CC, FTFN, and CFA with virtual ground into CM circuits with no additional circuit elements [102]. Later, transformation from OA based VM/CM circuit to the circuit employing CM building blocks and vice versa is proposed. The transformation is verified on filter and oscillator circuits.

Chapter 3 proposes new synthesis procedures for realizing various transfer functions and for enhancing the performance of active filters using only one active device [86], [103]. Among high Q, low-pass filters reported, those with equal-valued grounded capacitor are suitable for IC technology. However, they do not possess simple arrang-

ments for the gain adjustment and/or for accommodating the source conductance. Because of the OA, they do not operate satisfactorily at frequencies above about 50 kHz. CFA has a high slew rate and the circuits with bandwidth independent of the gain can be realized [5], [24], [25]. Therefore, in the later part of Chapter 3, single CFA based VM and CM EVGC low-pass filters with extremely low sensitivities are introduced [104].

In Chapter 4, EVGC realization of ladder networks [105] is presented. It is applicable when both the series and shunt branch admittances can be expressed as $Y + \frac{1}{Z}$ where $Y(Z)$ can be expressed as sum of RL and RC admittances (impedances).

All the amplitude equalizers discussed in Subsection 1.3.2 have been derived systematically and logically in Chapter 5. We also propose some new amplitude equalizers with additional features. A new design for realizing the Zyoute's amplitude equalizer [106] so as to have the variation within a specified whole range of the variable resistor and to have a flat response at a specified value of the same resistor is given in Chapter 5. The amplitude equalizers using CM building blocks are also derived which can operate satisfactorily at much higher frequencies compared to the OA based ones.

A novel oscillator [107], employing CM building block, with its utility in sensor circuits suitable for measurement of very small displacements, is presented in Chapter 6. In Chapter 7, a summary of the work is presented and some suggestions for further work are put forward.

Chapter 2

VOLTAGE MODE-TO-CURRENT MODE TRANSFORMATION

2.1 Introduction

Some of the VM-to-CM transformations proposed by various researchers have been reviewed in the last chapter. A new transformation for converting a class of VM circuits having active devices with virtual ground into corresponding CM circuits without any additional circuit elements is proposed here. Subsequently, it is shown that a VM/CM circuit using OAs can be converted into either a VM or a CM circuit using CM building blocks and vice versa. The validity of the transformation has been checked through simulation software PSPICE as well as on assembled circuits.

2.2 Proposed VM-to-CM transformation method

Let us examine the two circuits shown in Fig. 2.1 where N_a is the active network. Simpler circuits have been taken for the sake of convenience of analysis and more general circuits will be taken up in the next section.

Analysis of the circuits shown in Fig. 2.1(a) and (b) (derivations given in Appendix), respectively, lead to the following relations.

$$\frac{V_o}{V_i} = -\frac{Y_1}{Y_2} + \frac{V_x}{V_i}\left(1 + \frac{Y_1}{Y_2}\right) + \frac{I_x}{V_i Y_2} \tag{2.1}$$

$$\frac{I_o}{I_i} = -\frac{Y_1}{Y_2} + \frac{\overline{V}_x Y_1}{I_i} + \frac{\overline{I}_x Y_1}{I_i Y_2} \tag{2.2}$$

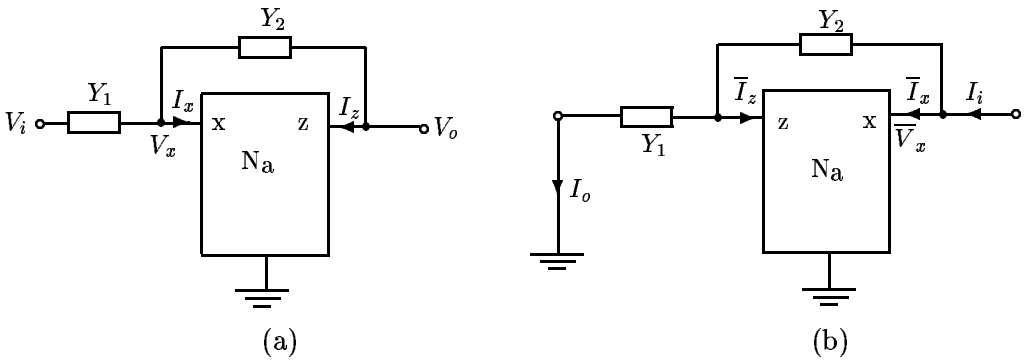


Fig. 2.1. (a) VM circuit and (b) CM circuit.

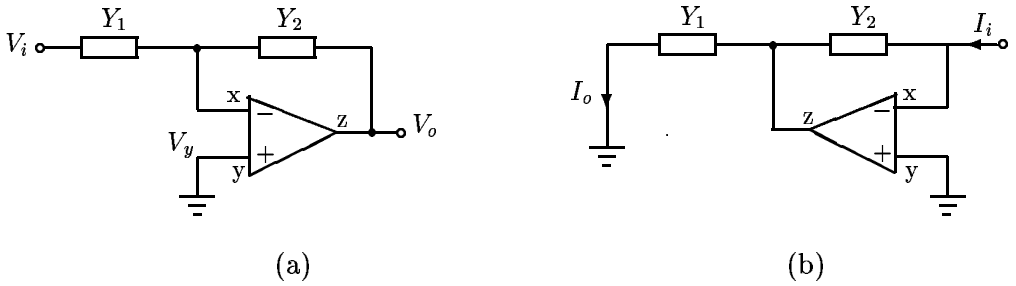


Fig. 2.2. OA based (a) VM and (b) CM circuits.

where V_x $[\overline{V}_x]$ and I_x $[\overline{I}_x]$ are the voltage and current at terminal x in Fig. 2.1(a) [(b)]. Note that (2.1) and (2.2) are independent of I_z and $\overline{I}_z$, respectively. Thus, it is immaterial, whether there is a flow of I_z $[\overline{I}_Z]$ in the z terminal of the active device or not. The two transfer functions will be the same, if

$$T(s) = \frac{V_o}{V_i} = \frac{I_o}{I_i} \tag{2.3}$$

which requires that

$$\frac{V_x}{V_i}\left(1 + \frac{Y_1}{Y_2}\right) + \frac{I_x}{V_i Y_2} = \frac{\overline{V}_x Y_1}{I_i} + \frac{\overline{I}_x Y_1}{I_i Y_2}. \tag{2.4}$$

This can be satisfied under the following 3 cases.

Case A

$$V_x = \overline{V}_x = 0,\ I_x = \overline{I}_x = 0. \tag{2.5}$$

These terminal characteristics are satisfied when the active network $\mathrm{N_a}$ is an OA ($V_x = V_y,\ I_x = I_y = 0$), an FTFN ($V_x = V_y,\ I_x = I_y = 0,\ I_z = \pm I_w$) or a CCII± ($V_x = V_y,\ I_y = 0,\ I_z = \pm I_x$) as shown in Figs. 2.2, 2.3 and 2.4, respectively,

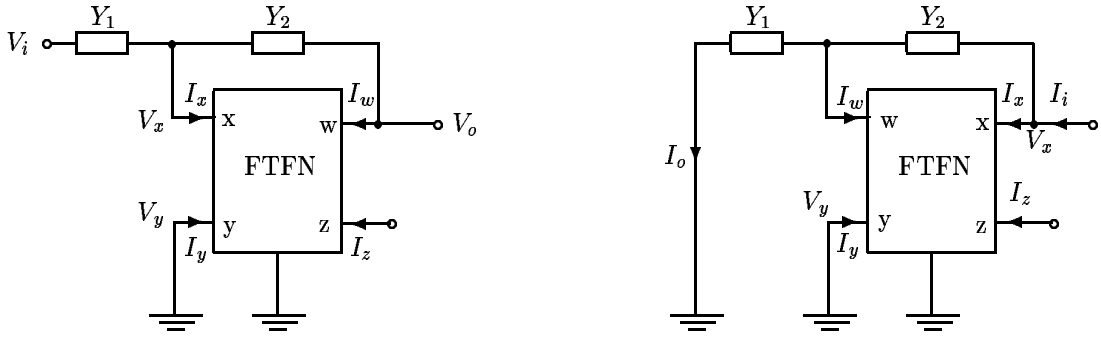


Fig. 2.3. FTFN based (a) VM and (b) CM circuits.

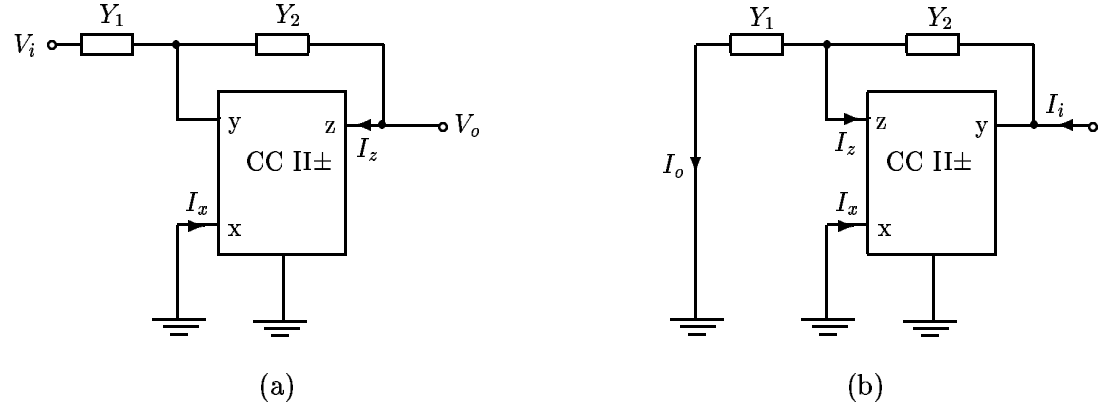


Fig. 2.4. CC based (a) VM and (b) CM circuits.

wherein terminal x (y) is maintained at virtual ground by making V_y $(V_x) = 0$. For these circuits

$$T(s) = \frac{V_o}{V_i} = \frac{I_o}{I_i} = -\frac{Y_1}{Y_2}. \tag{2.6}$$

From these figures, we see that the VM circuit can be converted into the CM circuit by interchanging the terminals x and z in case of OA, the terminals x and w in case of FTFN, the terminals y and z in case of CCII, and replacing the input-output sources. Connections of passive elements remain unchanged.

Let us consider a multi-input (V_1 and V_2) VM circuit shown in Fig. 2.5(a) and its transformed multi-output (I_{o1} and I_{o2}) circuit shown in Fig. 2.5(b). The output of the VM circuit is given as

$$V_o = -\frac{Y_1}{Y_2}V_1 - \frac{Y_3}{Y_2}V_2. \tag{2.7}$$

The two current outputs of the CM circuit are given as

$$I_{o1} = -\frac{Y_1}{Y_2}I_i, \quad I_{o2} = -\frac{Y_3}{Y_2}I_i. \tag{2.8}$$

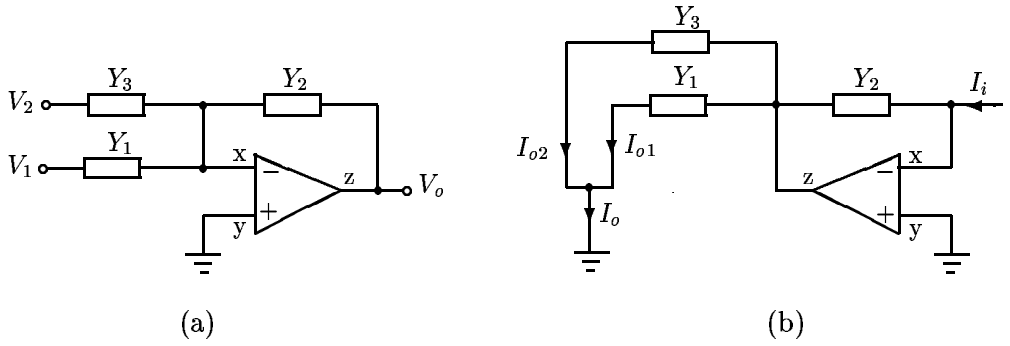


Fig. 2.5. OA based (a) multi-input VM circuit and (b) multi-output CM circuit.

These circuits can be used as the basic building blocks for realizing more complex functions. For an example, let us consider the Lovering's circuit, discussed earlier in Chapter 1 and redrawn, for convenience, in Fig. 2.6(a). Sub-networks A and B can be identified as the OA based multi-input blocks. Equation (2.7) is used for each building block and then solved for $T(s) = \frac{V_o}{V_i}$ to yield (1.18). A corresponding circuit using the multi-output CM blocks is shown in Fig. 2.6(b). Equation (2.8) is used for each building block in Fig. 2.6(b) and solved for $T(s) = \frac{I_o}{I_i}$, where $I_o = I_{o1} + I_{o4}$. It is interesting to note that this $T(s)$ is the same as given by (1.18). The procedure can be extended for converting VM circuits with n OAs (each with the non-inverting terminal grounded) into OA based CM circuits by interchanging x and z terminals of each OA and replacing the input-output sources.

The above procedure can be carried forward to VM circuits with n FTFN (CCII) circuits in which all the FTFNs (CCIIs) have V_y (V_x) = 0. For an example, it is applied on the Akerberg and Mossberg's 3-OA VM biquad [108] and Thomas's 4-OA VM biquad [2] (pp. 345-347), [109] shown in Figs. 2.7 and 2.8, respectively. The transfer function of the circuits shown in Fig. 2.7 is

$$\frac{V_o}{V_i} = \frac{I_o}{I_i} = \frac{Y_b Y_e Y_g - Y_a Y_c Y_e - Y_b Y_d Y_h}{Y_b Y_d Y_f + Y_c Y_e Y_i} \tag{2.9}$$

and that of the circuits shown in Fig. 2.8 is

$$\frac{V_o}{V_i} = \frac{I_o}{I_i} = \frac{Y_a Y_c Y_e Y_h + Y_a Y_d Y_f Y_i - Y_b Y_d Y_f Y_j - Y_c Y_e Y_g Y_j}{Y_b Y_d Y_f Y_k + Y_c Y_e Y_g Y_k}. \tag{2.10}$$

It may be mentioned that the method used for determing the current transfer function in the above example can be considered as a more simplified one compared to the one by applying the KCL at each node of the circuit.

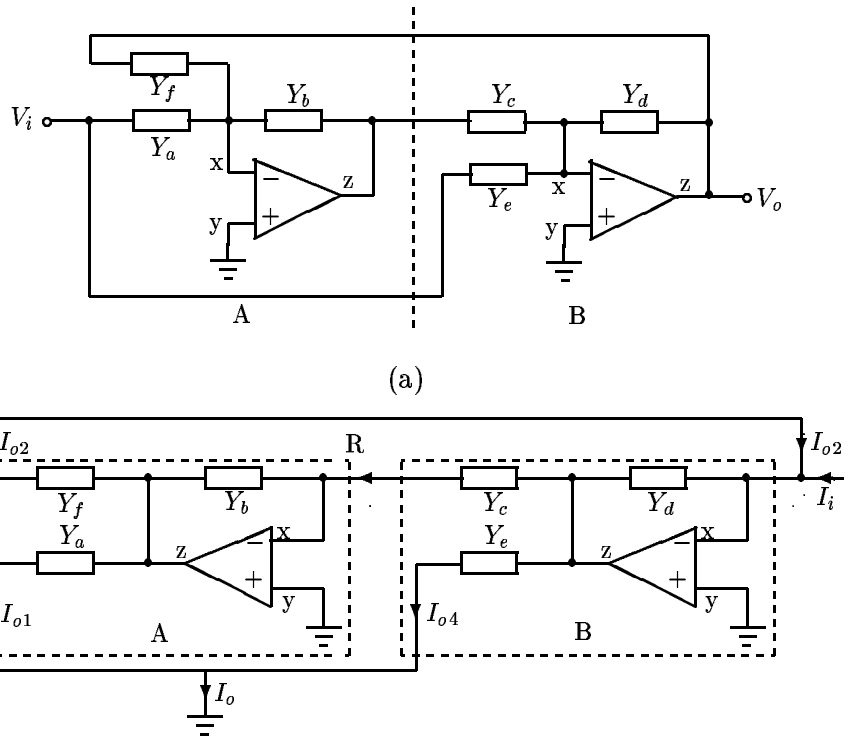


Fig. 2.6. (a) OA based VM Lovering's circuit, (b) corresponding OA based CM circuit.

Case B

$$V_x = \overline{V}_x = 0,\ I_x \neq 0,\ \overline{I}_x \neq 0. \tag{2.11}$$

Under these conditions, (2.4) reduces to

$$\frac{I_x}{\overline{I}_x} = \frac{V_i Y_1}{I_i} \tag{2.12}$$

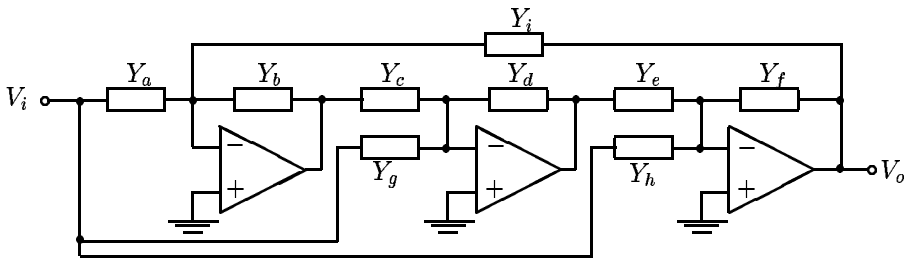
Using (2.3), we get

$$\frac{I_x}{\overline{I}_x} = \frac{V_o Y_1}{I_o} = \frac{V_z}{\overline{V}_z}. \tag{2.13}$$

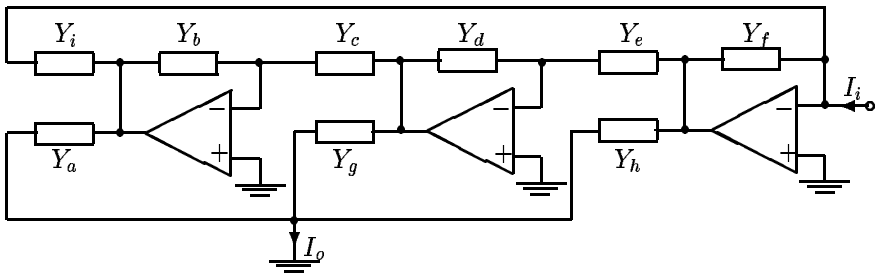
This condition, and those in (2.11) are satisifed when the active network $\mathrm{N_a}$ is a CFA ($I_z = I_x,\ V_w = V_z,\ V_x = V_y$) as shown in Fig. 2.9. For both the Figs. 2.9(a) and (b), we have

$$I_x = I_z = -V_w Y = -V_z Y \tag{2.14}$$

where $Y \neq \infty$. Thus, the current I_x, as desired for the transformation to hold, satisfies the condition in (2.13).



(a)



(b)

Fig. 2.7. (a) 3-OA VM biquad circuit, (b) 3-OA CM biquad circuit.

Now, from (2.1)

$$T(s) = -\frac{Y_1}{Y_2} + \frac{I_x}{V_i Y_2} = -\frac{Y_1}{Y_2} - \frac{V_w Y}{V_i Y_2} = -\frac{Y_1}{Y_2} - \frac{V_o Y}{V_i Y_2} \tag{2.15}$$

which leads to

$$T(s) = -\frac{Y_1}{Y_2 + Y}. \tag{2.16}$$

From Fig. 2.9, we note that the CFA based VM circuit (with terminal y grounded and the output tapped from the terminal w) can be converted into CFA based CM circuit by interchanging the terminals x and w of the CFA and replacing input-output sources. Connections of passive elements remain unchanged. Thus, the procedure is the same as that for the OA based circuits under case A.

In a manner similar to the one used in case of OA based circuits, it can be shown that the procedure is applicable to CFA based VM circuits having more number of CFAs and with terminal y grounded.

As an example, let us consider the VM circuit shown in Fig. 2.10(a). Following the above procedure, we obtain the CM circuit as shown in Fig. 2.10(b). The two circuits have the same transfer function as given by (1.18). In (1.18), if $Y_b = Y_c = 1$ S,

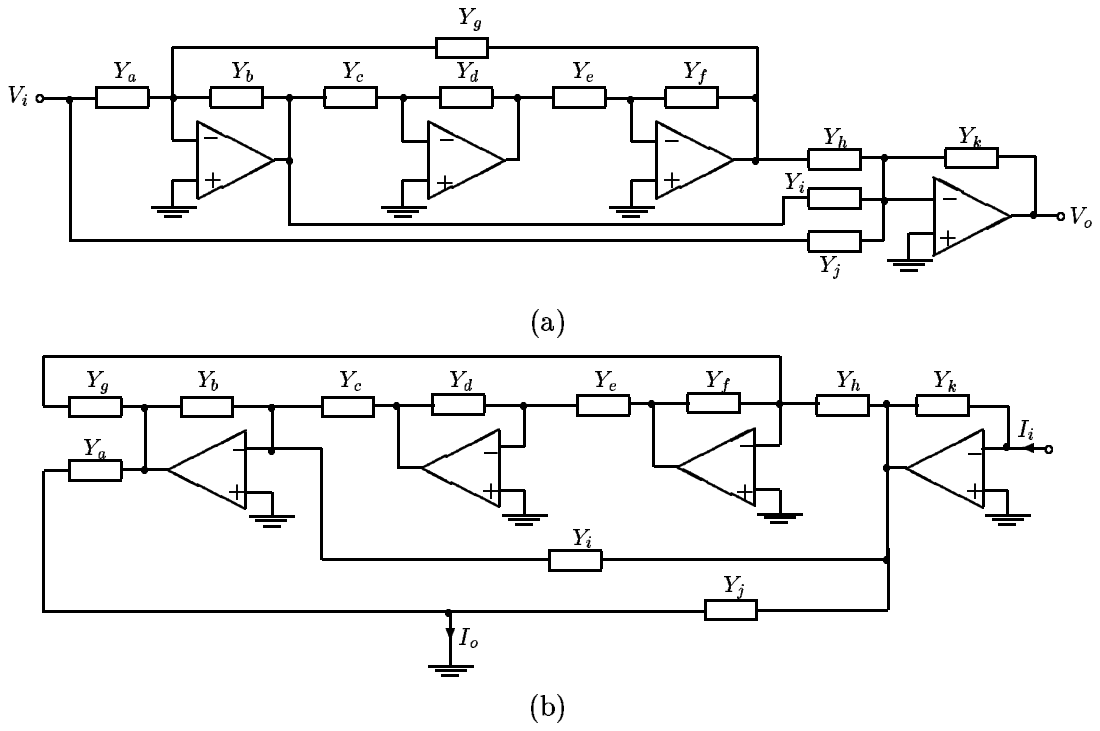


Fig. 2.8. (a) 4-OA VM biquad circuit, (b) 4-OA CM biquad circuit.

the transfer function becomes

$$T(s) = \frac{Y_a - Y_e}{Y_d - Y_f}. \tag{2.17}$$

As an example, the realization of $T(s) = \frac{s^2 - s + 1}{s^2 + s + 1}$ is obtained using (2.17) and is shown in Fig. 2.11.

In both these cases, it is required that the active devices should have virtual ground.

Case C

$$V_x \neq 0,\ \overline{V}_x \neq 0,\ I_x = 0,\ \overline{I}_x = 0. \tag{2.18}$$

Under these conditions, (2.4) results in

$$\frac{\left(1 + \frac{Y_1}{Y_2}\right) V_x}{\overline{V}_x} = \frac{V_i Y_1}{I_i} = \frac{V_z}{\overline{V}_z}. \tag{2.19}$$

The conditions given in (2.18) and (2.19) are satisfied when $\mathrm{N_a}$ is an amplifier of gain $A\left(1 + \frac{Y_1}{Y_2}\right)$ in voltage mode and A in current mode as shown in Fig. 2.12.

In the VM circuit, the amplifier gain is complex (a function of Y_1 and Y_2) whereas it is positive real in the CM circuit. Hence, the VM circuit will require a larger

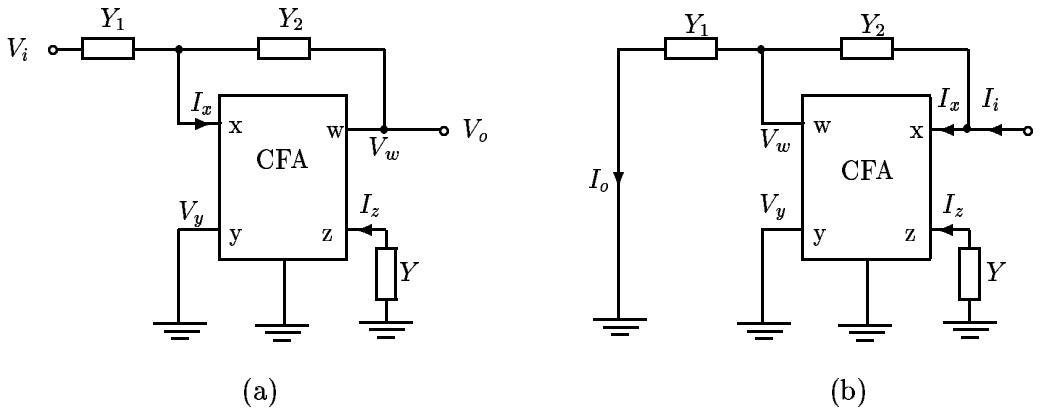


Fig. 2.9. CFA based (a) VM and (b) CM circuits.

number of passive elements than the CM circuit. Moreover, both these circuits are more complex than those shown in Figs. 2.2, 2.3, 2.4, and 2.9. For these circuits

$$T(s) = \frac{V_o}{V_i} = \frac{I_o}{I_i} = -\left(\frac{A}{A-1}\right)\frac{Y_1}{Y_2}. \tag{2.20}$$

This relation does not offer any special advantage of these circuits over those of Figs. 2.2, 2.3, 2.4, and 2.9. Hence, this case will not be dealt with any more.

2.3 Applications of transformation method to general circuits

More general circuits in voltage mode and their transformed circuits in current mode corresponding to the cases A and B are obtained from Figs. 2.2 and 2.9, by replacing 2-terminal passive elements by 3-terminal passive networks $\mathrm{N_A}$ and $\mathrm{N_B}$ or $\mathrm{N_{\overline{B}}}$ and these circuits are shown in Figs. 2.13 and 2.14, respectively. Analysis of these two circuits gives

$$T(s) = \frac{V_o}{V_i} = \frac{I_o}{I_i} = -\frac{-Y_{21\mathrm{A}}}{-Y_{21\mathrm{B}}} \tag{2.21}$$

and

$$T(s) = \frac{V_o}{V_i} = \frac{I_o}{I_i} = -\frac{-Y_{21\mathrm{A}}}{(-Y_{21\overline{\mathrm{B}}}) + Y} = -\frac{-Y_{21\mathrm{A}}}{-Y_{21\mathrm{B}}}, \tag{2.22}$$

respectively. Here $Y_{21\mathrm{A}}$, $Y_{21\mathrm{B}}$, and $Y_{21\overline{\mathrm{B}}}$ are the transfer admittances of networks $\mathrm{N_A}$, $\mathrm{N_B}$, and $\mathrm{N_{\overline{B}}}$, respectively, and $Y_{21\mathrm{B}} = Y_{21\overline{\mathrm{B}}} - Y$.

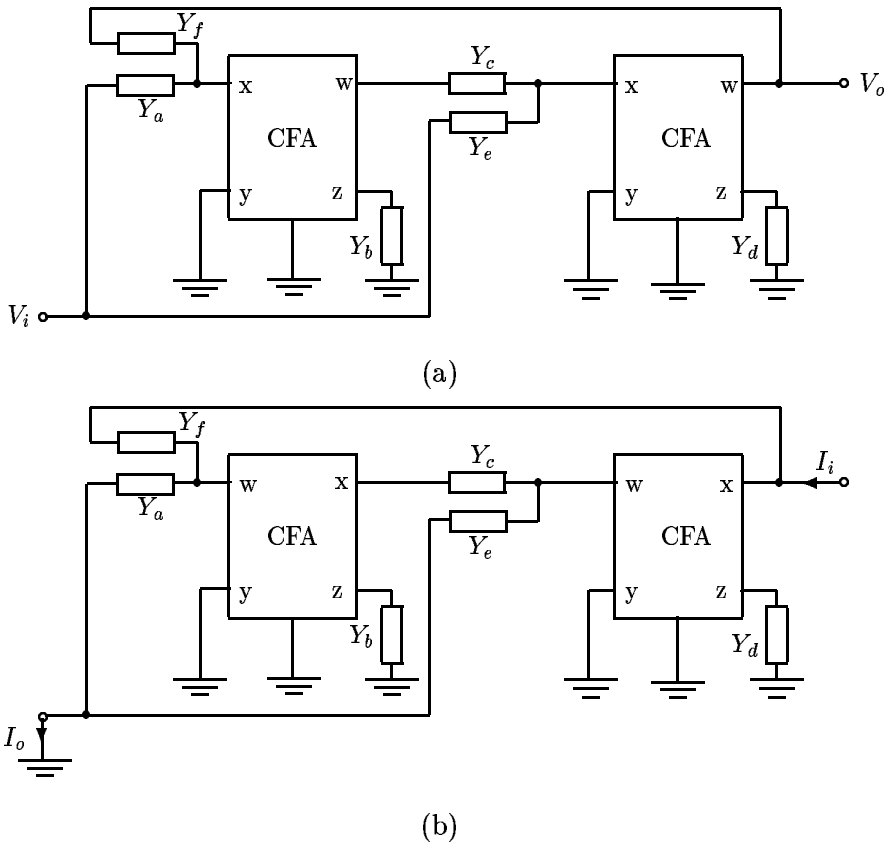


Fig. 2.10. (a) VM and (b) CM circuits with more number of CFAs.

Special features

1. A close examination of (2.21) and (2.22) shows that the following procedure can be used for converting OA based VM/CM circuit of Fig. 2.13 into CFA based circuit shown in Fig. 2.14 without increasing the number of passive components.

> Take out a suitable driving point admittance Y from $Y_{21\mathrm{B}}$ of the OA based circuit and realize the remaining admittance $Y_{21\overline{\mathrm{B}}}$ as transfer admittance by the network $\mathrm{N}_{\overline{\mathrm{B}}}$.

For example, the OA based VM low-pass filter shown in Fig. 2.15(a) is converted into four CFA based CM low-pass filters shown in Fig. 2.15(b). One can now easily visualize that CFA based CM circuit of Fig. 2.10(b) is derivable from the OA based VM circuit of Fig. 2.6(a).

2. All the linear operations performed by single-input OA circuits can also be performed by CFA circuits in both voltage and current modes. As an example, a CM phase shift oscillator shown in Fig. 2.16 is derived from the OA based one.

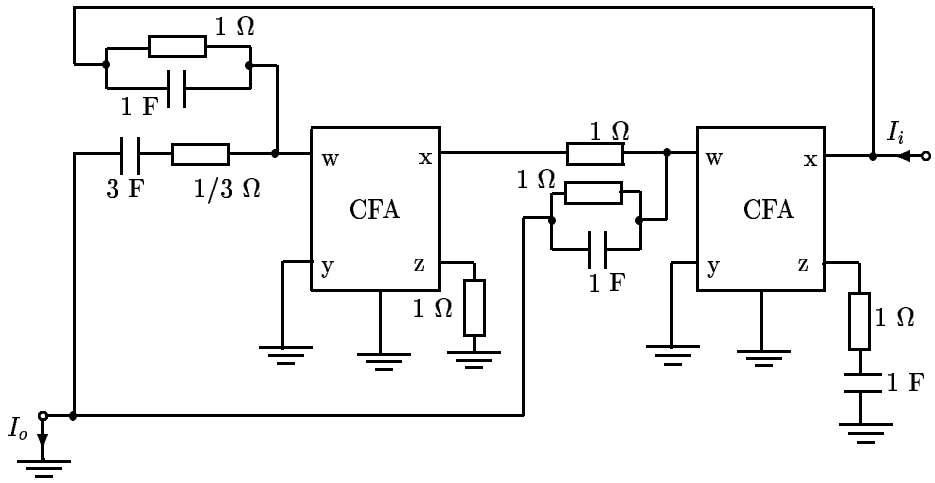


Fig. 2.11. CM all-pass filter.

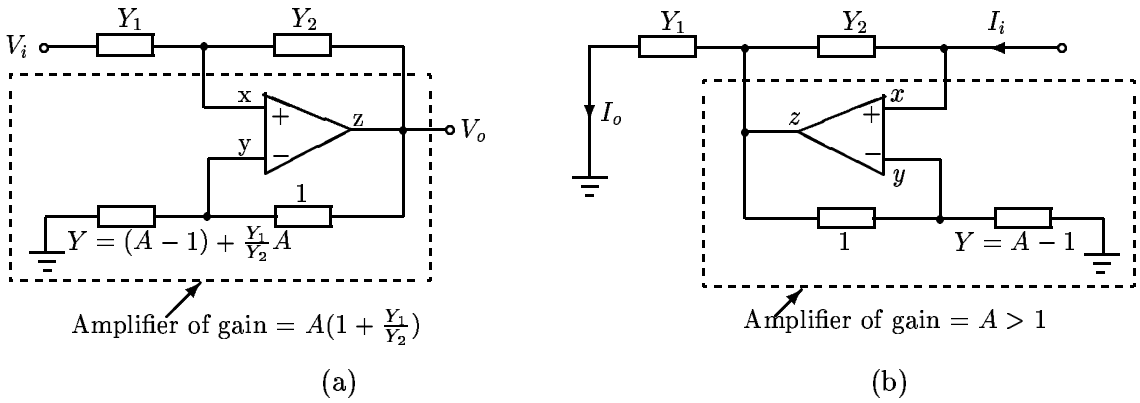


Fig. 2.12. (a) VM circuit and (b) CM circuit with active device having no input terminal at virtual ground.

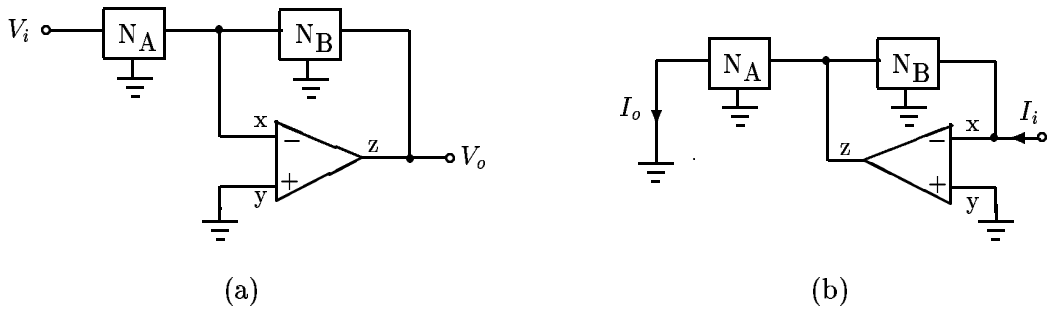


Fig. 2.13. Generalized OA based (a) VM and (b) CM circuits with 3 terminal passive network.

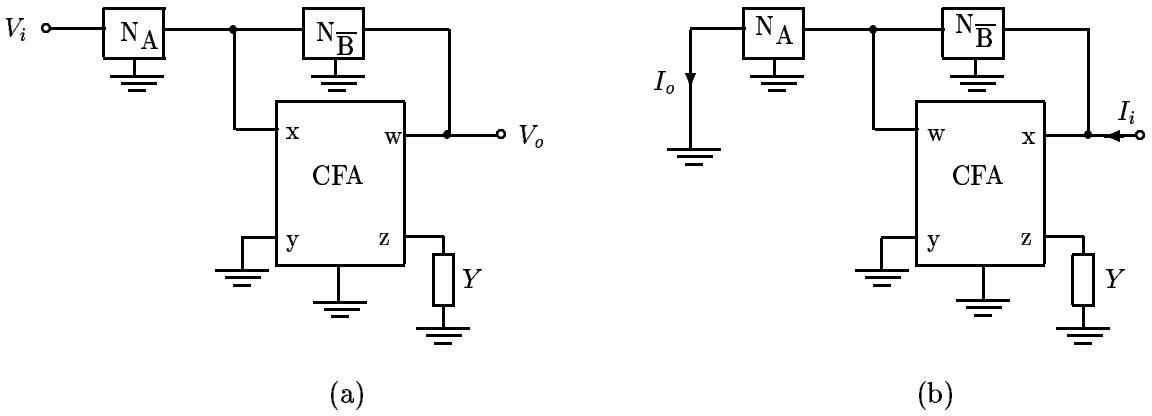


Fig. 2.14. Generalized CFA based (a) VM and (b) CM circuits.

3. It may be noted from (2.21) that $T(s)$ being a ratio of two transfer admittances, any stable voltage or current transfer function with zeros off the positive real axis can be realized using just one OA [1] and hence by one CFA. As an example, the realization of the notch function $T(s) = -\dfrac{(s^2+2)}{(s^2+0.2s+2)}$, following the procedure in [1] (p. 474) (after making corrections), is given in Fig. 2.17.

The procedure outlined is also applicable to more generalized OA based VM and CM circuits shown in Fig. 2.18 where N is a 4-terminal passive network. As an example, the OA based circuit of the VM band-pass filter [2] is transformed into four CM circuits shown in Fig. 2.19.

Table 2.1 gives a comparision of our VM-to-CM transfromation technique with those reported earlier. The proposed technique leads to the transformation without any additional elements.

2.4 Sensitivity to nonidealities

Considering the nonidealities arising from the physical implementation of the CFA, its terminal relationship can be given as

$$\begin{bmatrix} V_x \\ I_y \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & \gamma & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha & 0 & 0 & 0 \\ 0 & 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ I_w \end{bmatrix}. \tag{2.23}$$

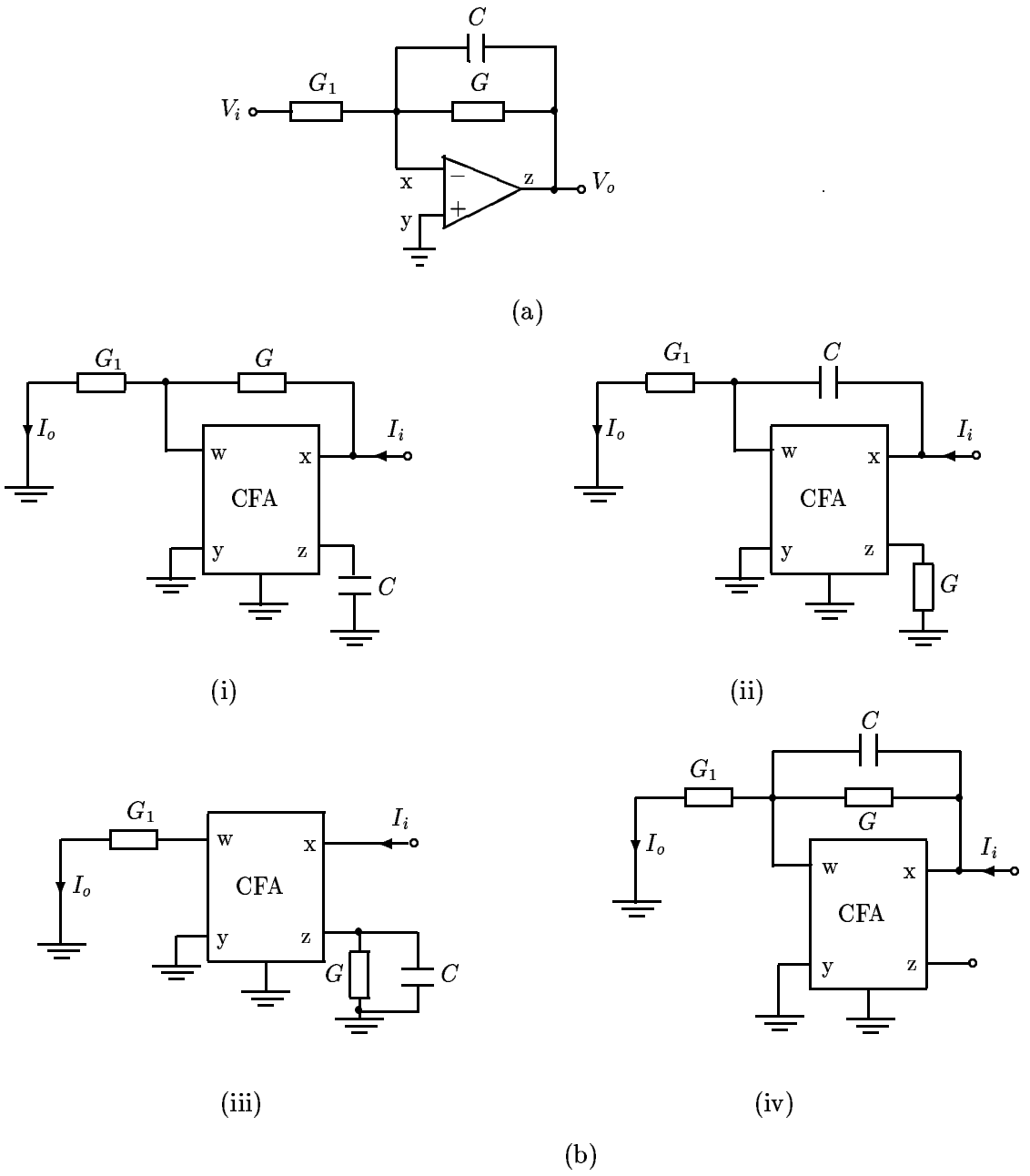


Fig. 2.15. (a) OA based VM low-pass filter and (b) four CFA based CM low-pass filters.

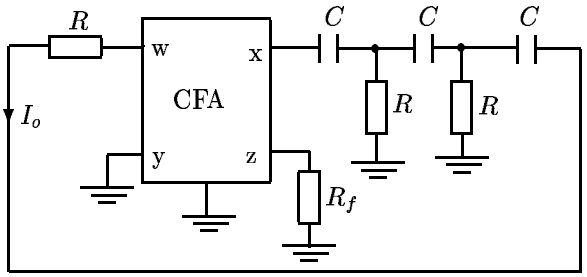


Fig. 2.16. CM phase shift oscillator.

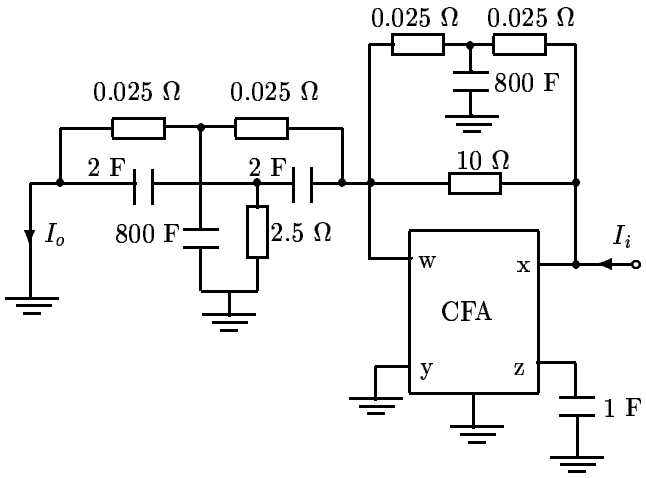
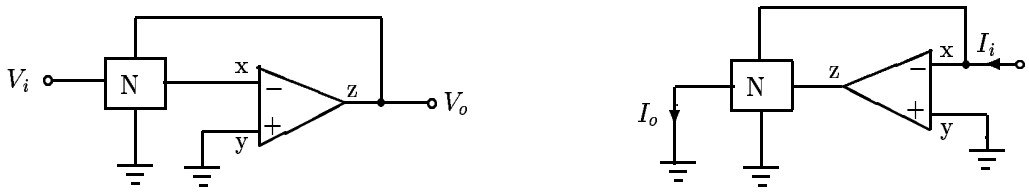


Fig. 2.17. CM notch filter.



(a) (b)

Fig. 2.18. Generalized OA based (a) VM and (b) CM circuits with 4 terminal passive network.

Table 2.1. A comparision of various VM-to-CM transformations.

Transformation Technique	Grounded capacitor realizations	Change of active/passive elements	Need of additional elements	Transformation using any active device
Robert and Sedra [36]: Adjoint network	No	No	No	No
Carlosena and Moschytz [43]: Nullators-norators for OA	No	No	Yes	No
Aronhime and Lata [44]: Adding o/p admittances	No	Yes	Yes	No
Uzunhisarcikli and Alci [45]: Nullators-norators for FTFN/CC	No	Yes	Yes	No
Proposed [102]: Input-output interchange	Yes	No	No	Yes

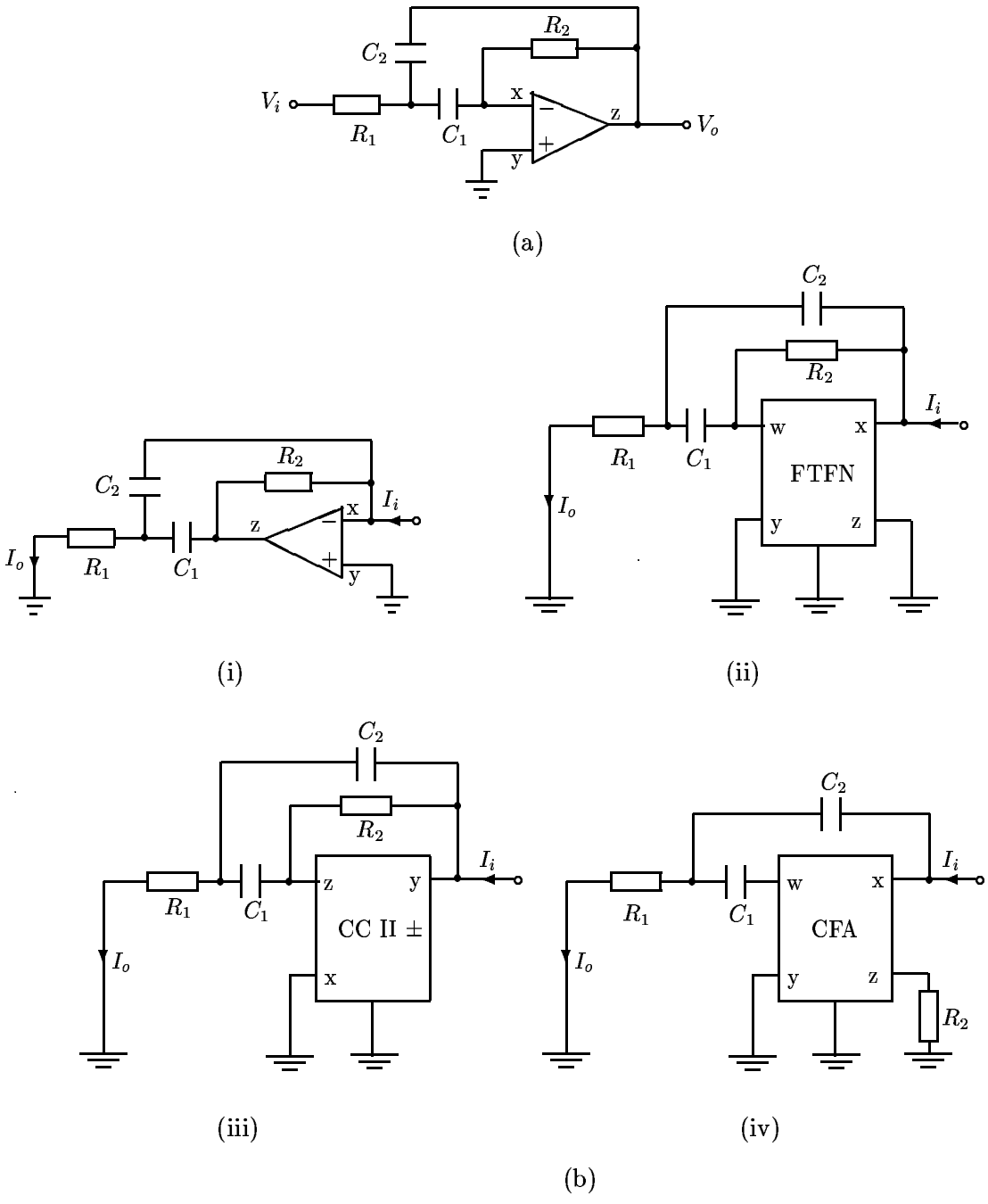


Fig. 2.19. (a) OA based VM band-pass filter and (b) four CM band-pass filters.

where α is the current gain and β and γ are the voltage gains which can be expressed as $\alpha = 1 - \epsilon_1$, $\beta = 1 - \epsilon_2$, and $\gamma = 1 - \epsilon_3$. Here, ϵ_1 ($\epsilon_1 << 1$) denotes the current tracking error of the CFA and ϵ_2 ($\epsilon_2 << 1$), ϵ_3 ($\epsilon_3 << 1$) are the voltage tracking errors. There is no effect of the voltage tracking error ϵ_3 as the y terminal of the CFA is grounded. The transfer function I_o/I_i of the low-pass filter shown in Fig. 2.15(b) can be written as

$$\frac{I_o}{I_i} = \frac{-\frac{\alpha\beta G_1}{C}}{s + \frac{\alpha\beta G}{C}}. \tag{2.24}$$

As the y terminal of CFA is grounded, the voltage gain γ does not appear in the transfer function. Applying the usual definition of sensitivity

$$S_y^x = \frac{y}{x}\frac{\partial x}{\partial y} \tag{2.25}$$

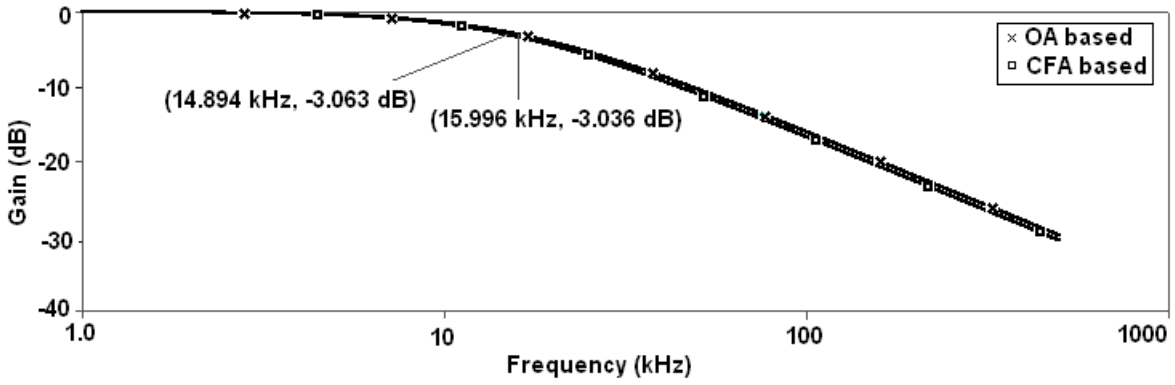
it is found that the passive and active sensitivities of these low-pass filters are

$$S_G^{\omega_0} = -S_C^{\omega_0} = 1, \quad S_{G_1}^{\omega_0} = 0,$$
$$S_\alpha^{\omega_0} = S_\beta^{\omega_0} = 1. \tag{2.26}$$

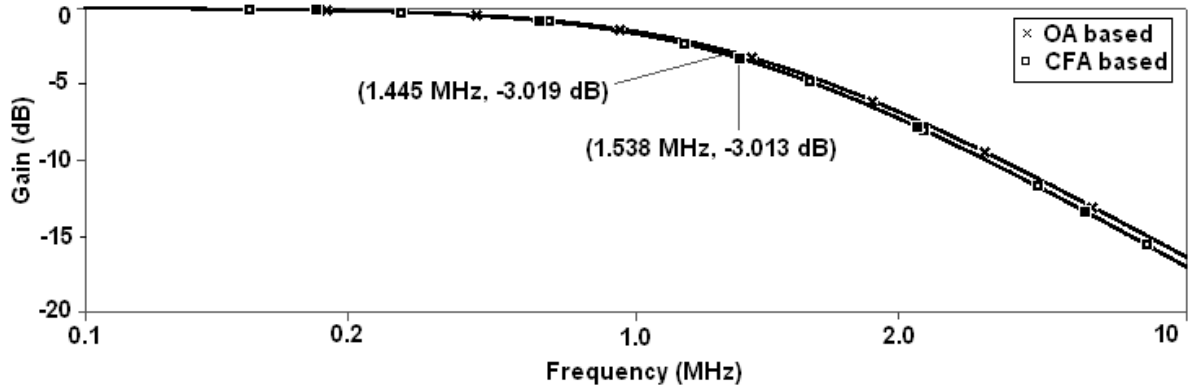
Thus the passive and active sensitivities for the presented filters are low, no more than unity in magnitude.

2.5 Simulation results

All the low-pass filters shown in Fig. 2.15 were simulated for 3-dB cutoff frequency of 15.9 kHz, using CFA AD844 and high frequency OA AD817 with supply voltages of $\pm$15 V, and employing PSPICE software [110]. The circuit components were $R = R_1 = 1$ kΩ, $C = 10$ nF. All the filters gave nearly the same magnitude response as shown in Fig. 2.20(a). The low-pass filters were also simulated for cutoff frequency as high as 1.59 MHz. The circuit components used for this purpose were $R = R_1 = 1$ kΩ, $C = 100$ pF. The corresponding magnitude responses are shown in Fig. 2.20(b). The phase shift oscillator of Fig. 2.16 was also simulated and the output waveform, as shown in Fig. 2.21, has peak-to-peak amplitude of 10 mA. It may be noted that, the oscillator circuit does not have a separate amplitude stabilizer and the oscillation levels are limited by the supply voltages. For supply voltages of $\pm$6 V, the simulation resulted in peak-to-peak amplitude of 2 mA.



(a)



(b)

Fig. 2.20. Simulation results - Frequency responses of low-pass filters shown in Fig. 2.15 with (a) $R = R_1 = 1$ kΩ, $C = 10$ nF for $f_0 = 15.9$ kHz and (b) $R = R_1 = 1$ kΩ, $C = 100$ pF for $f_0 = 1.59$ MHz.

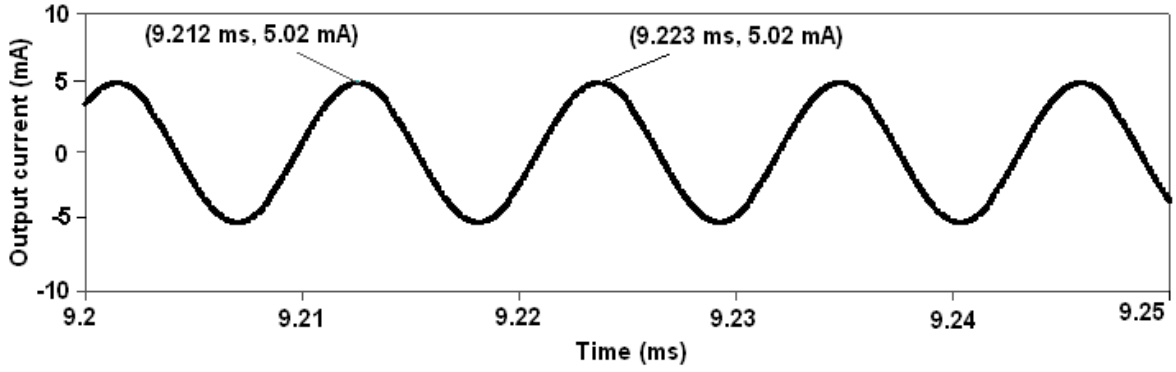


Fig. 2.21. I_o waveform of the phase shift oscillator with $R = 649.74$ Ω, $C = 1$ nF, $R_f = 25$ kΩ.

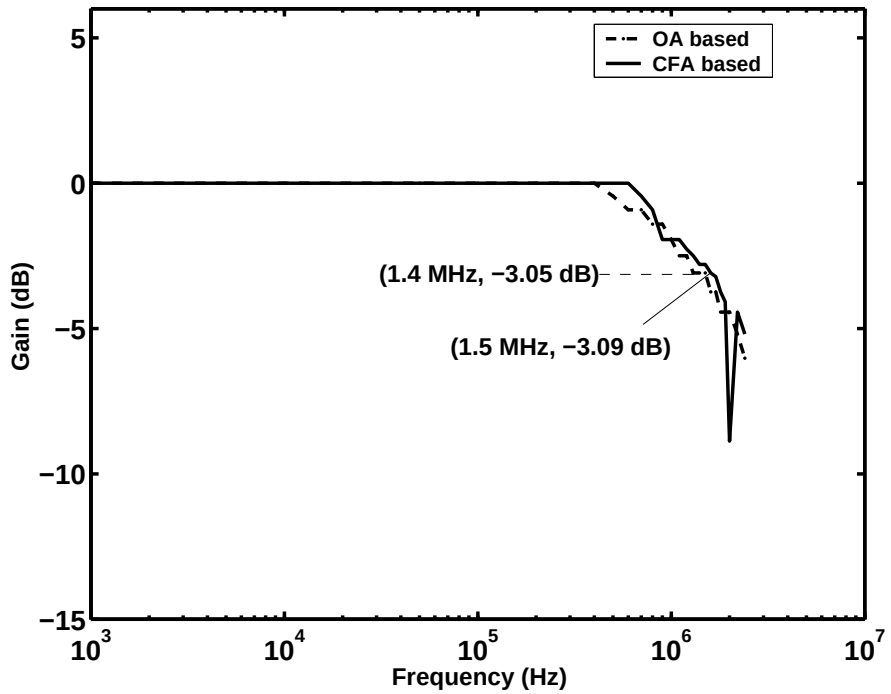


Fig. 2.22. Experimental results - Frequency responses of low-pass filters shown in Fig. 2.15 with $R = R_1 = 1$ kΩ, $C = 100$ pF for $f_0 = 1.59$ MHz.

2.6 Practical results

To validate the transformation at high cutoff frequencies of the filters, the circuit for low-pass filter shown in Fig. 2.15(a) was assembled using a high frequency OA AD817 and that for low-pass filter shown in Fig. 2.15(b)(i) was assembled using CFA AD844. In case of CFA, to generate the input current, 1 kΩ resistor was connected in series with the input voltage source. The other circuit elements chosen for the cutoff frequency of 1.59 MHz are R=R_1=1 kΩ and C= 100 pF. Both the low-pass filters performed almost identically for the cutoff frequency as high as 1.59 MHz as shown in Fig. 2.22.

2.7 Concluding remarks

A procedure for converting a class of VM circuits, which have the active devices with virtual ground, into CM circuits without altering the transfer function and without requiring any additional components has been developed. It covers the circuits having active devices like OA, FTFN, CC, and CFA. Since voltage and current trans-

fer functions (assuming the same active devices) are the same, the characteristics such as stability, tunability, sensitivity etc. remain unaltered. The procedure has been demonstrated by examples. Thus, a single circuit can be used in either mode. The validity of the proposed transformation procedure has been tested by simulating the transformation of the low-pass filter and phase shift oscillator with the help of PSPICE. The experimental results show that the frequency responses of both the VM and CM low-pass filters are identical. The active and passive sensitivities for the presented filters are very low. It has been shown that a single FTFN, CCII, and CFA based circuits can realize both stable voltage and current transfer functions with zeros off the positive real axis.

Chapter 3

SYNTHESIS TECHNIQUES FOR ACTIVE FILTERS

3.1 Introduction

In this chapter, new synthesis techniques for the filter circuits employing CM building blocks for improved frequency response and to achieve circuit topologies suitable for IC technology are presented. Different systematic synthesis procedures for realizing a class of current/voltage transfer functions of *any order with negative real poles* using only one active device are proposed in Section 3.2. One of the procedures requires the least number of elements and can yield all the capacitors grounded with the minimum total capacitance. These synthesis procedures are restricted to the transfer functions with distinct negative real poles only and therefore, are restricted to low Q values. Section 3.3 presents a technique to overcome this restriction. Later in Section 3.4, apart from grounded capacitor and minimum total capacitance realization, equal-valued capacitor realization of filters is also proposed which is capable of realizing any desired gain constant and/or accommodating any specified source conductance. The resulting filters have low passive sensitivities. Such a realization allows easy compensation for the parasitic capacitors [9], eliminates the etching process and reduces the number of gold contacts thereby increasing the circuit reliability [10] and helps in saving silicon area and easy processing in IC technology [6], [11], [12] (pp. 10-12), [13]-[15].

3.2 Realization of active filters employing CM building blocks

Filters employing CM building blocks are attractive because of their wider bandwidth and lower power consumption compared to their VM counterparts [3]. Recently, CM circuits using single FTFN [27], [50], [51] or several FTFNs [28], [49] have been proposed for filters with specific orders.

Çiçekoğlu's biquad [28] requires 3 FTFNs and 4 passive elements, with all the capacitors not necessorily grounded. It realizes second order low-pass/high-pass and band-pass filters simultaneously. The circuit provides high output impedance, but its input impedance is also high. The filter proposed by Liu and Lee [49] realizes second order low-pass and band-pass filters with two FTFNs, two grounded capacitors, and three resistors. Only the band-pass filter has high output impedance.

Abuelma'aati's single FTFN circuit [50] requires 6 passive elements for all types of second order filters except the band-pass filter which requires 7 elements. Only the low-pass filter has both the capacitors grounded. Higashimura's first order all-pass filter [27] requires two resistors and a grounded capacitor. The filter proposed by Liu and Hwang [51] realizes all-pass, band-pass, notch, high-pass and low-pass filters with 7, 6, 7, 4 and 4 passive elements, respectively, with a high output impedance.

Here, we introduce three systematic synthesis procedures for realizing a class of current transfer functions of any order with negative real poles using only one active device.

Let us consider the circuit shown in Fig. 3.1, where Y_1, Y_2, Y_3, and Y_4 are the 2-terminal RC driving point admittances (DPAs). Analysis of the circuit gives

$$T(s) = \frac{I_o}{I_i} = K\frac{N(s)}{D(s)} = \frac{Y_1Y_4 - Y_2Y_3}{Y_4(Y_1 + Y_2)} \tag{3.1}$$

where K is a gain constant, $N^\circ \leq D^\circ$. The derivation of (3.1) is given in Appendix. It is interesting to note that scaling of Y_1, Y_2 by one factor and Y_3, Y_4 by another factor does not change the $T(s)$.

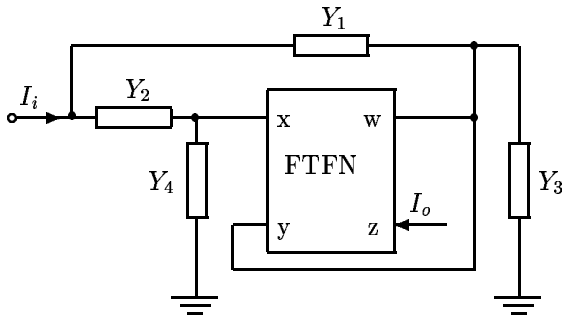


Fig. 3.1. The FTFN circuit.

3.2.1 Synthesis I

In Fig. 3.1, if $Y_3 = Y_4$, then (3.1) reduces to

$$T(s) = K\frac{N(s)}{D(s)} = \frac{(Y_1 - Y_2)}{(Y_1 + Y_2)}. \tag{3.2}$$

Let

$$\frac{Y_1 - Y_2}{Y_1 + Y_2} = K\frac{\Pi_{j=1}^{m}(s + z_j)}{\Pi_{i=1}^{n}(s + y_i)} = K\frac{N(s)/Q(s)}{D(s)/Q(s)} \tag{3.3}$$

where $Q(s)$ is defined in (3.5) and $m \leq n$. In (3.3), let

$$Y_1 - Y_2 = K\frac{N(s)}{Q(s)}, \qquad Y_1 + Y_2 = \frac{D(s)}{Q(s)}. \tag{3.4}$$

Since $Y_1 + Y_2$, being the sum of two RC DPAs, is also an RC DPA, it must have poles and zeros on the negative real axis, interlaced and the lowest (highest) critical frequency a zero (pole). With these restrictions,

$$Q(s) = \Pi_{k=1}^{n-1}(s + p_k) \tag{3.5}$$

where $y_{k+1} > p_k > y_k$, $k = 1,2, \ldots n-1$. A factor $(s + p_n)$ such that $p_n > y_n$ could be added in $Q(s)$, but the above choice is made to have less number of elements in Y_1 and Y_2. Equation (3.4) can be expressed as

$$Y_1 + Y_2 = \left[A_\infty s + \sum_{k=0}^{n-1}\frac{A_k s}{(s + p_k)}\right] \tag{3.6}$$

and

$$Y_1 - Y_2 = \left[KB_\infty s + K\sum_{k=0}^{n-1}\frac{B_k s}{(s + p_k)}\right] \tag{3.7}$$

where

$$p_0 = 0, \tag{3.8}$$

$$A_\infty = \begin{cases} 0, & m < n \\ \dfrac{D(s)}{sQ(s)}\Big|_{s\to\infty}, & m = n, \end{cases} \tag{3.9}$$

$$B_\infty = \begin{cases} 0, & m < n \\ \dfrac{N(s)}{sQ(s)}\Big|_{s\to\infty}, & m = n, \end{cases} \tag{3.10}$$

$$A_k = \left.\frac{(s+p_k)D(s)}{sQ(s)}\right|_{s=-p_k}, \tag{3.11}$$

and

$$B_k = \left.\frac{(s+p_k)N(s)}{sQ(s)}\right|_{s=-p_k}. \tag{3.12}$$

A_k, being the residues at the poles of an RC DPA, will be positive real. Thus

$$A_k > 0. \tag{3.13}$$

From (3.6) and (3.7), after scaling by a factor of 2,

$$Y_1 = \left[s(A_\infty + KB_\infty) + s\sum_{k=0}^{n-1}\frac{A_k + KB_k}{s+p_k}\right] \tag{3.14}$$

and

$$Y_2 = \left[s(A_\infty - KB_\infty) + s\sum_{k=0}^{n-1}\frac{A_k - KB_k}{s+p_k}\right]. \tag{3.15}$$

For Y_1 and Y_2 to be RC DPAs, the residues at the poles must be positive real, i.e.,

$$A_k \pm KB_k \geq 0, k = 0, 1, 2, \ldots n-1, \infty. \tag{3.16}$$

Thus, K must be chosen such that (3.16) satisfies for both Y_1 and Y_2 to be RC realizable, that is,

$$K \leq \min\left[\frac{A_k}{|B_k|}\right], k = 0, 1, 2, \ldots n-1, \infty. \tag{3.17}$$

It may be noted from (3.2) that the poles of $T(s)$ are the zeros of the RC DPA $(Y_1 + Y_2)$. *Hence, the method can realize the current transfer functions with distinct negative real poles only.*

Total number of elements: If K is chosen such that the equality condition in (3.17) holds, one element will reduce when $k = 0$ or ∞, and two elements when $k \neq 0$ or ∞.

For reducing the number of circuit elements, admittances Y_3 and Y_4 can be selected to be purely conductive. Therefore, the total number of elements required is

$$\begin{aligned} N &= \text{total number of elements in } (Y_1, Y_2, Y_3, Y_4) \\ &\quad - (0,\ 1 \text{ or } 2 \text{ elements depending upon the value of } K \text{ chosen}) \\ &= ([2(n-1)+2]+[2(n-1)+2]+1+1) - (0,\ 1 \text{ or } 2) \\ &= (4n+2) - (0,\ 1 \text{ or } 2). \end{aligned} \tag{3.18}$$

Thus, the number of elements will lie between $4n$ and $4n + 2$.

The same method can be used for the realization of transfer function using OTRA. In a recent brief by Cakir *et al.* [31], realizations of all-pass filters of first and second orders were proposed employing the circuit configuration shown in Fig. 3.2 where OTRA has the following terminal characteristics:

$$\begin{bmatrix} V_x \\ V_y \\ V_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ -R_m & R_m & 0 \end{bmatrix} \begin{bmatrix} I_x \\ I_y \\ I_z \end{bmatrix}. \tag{3.19}$$

These filters use four and six passive elements for first and second order all-pass filters, respectively. Sensitivity analysis has shown that all the passive sensitivities are lower than unity in magnitude [31]. These filters, however, are restricted to the distinct negative real pole(s) only and, therefore, they are restricted to low Q values.

Here, the same circuit configuration has been exploited for realizing a *general class of transfer functions of arbitrary order*. Since, the gain-bandwidth product of OTRA ($\approx$ 1 GHz) is much higher than that of an OA ($\approx$ 1 MHz), the filters are capable of working efficiently even at much higher frequency [31]. Owing to the internal grounding of the OTRA input terminals, effects of input parasitics are significantlly reduced. Assuming ideal OTRA ($R_m = \infty$), the voltage transfer function of the circuit is

$$T(s) = K\frac{N(s)}{D(s)} = \frac{(Y_1 - \mu Y_2)}{(Y_1 + Y_2)} \tag{3.20}$$

where $\mu = \dfrac{Y_3}{Y_4}$ (real) (derivation given in Appendix).

Thus, following a procedure similar to the one for synthesis with FTFN, we get

$$Y_1 = \left[s(\mu A_\infty + KB_\infty) + \sum_{k=0}^{n-1} \frac{(\mu A_k + KB_k)s}{s + p_k}\right] \times \left(\frac{1}{1+\mu}\right) \tag{3.21}$$

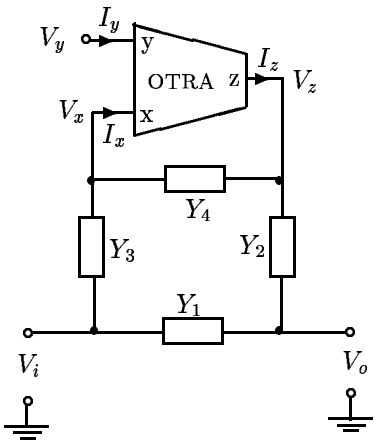


Fig. 3.2. The circuit configuration using OTRA.

and

$$Y_2 = \left[s(A_\infty - KB_\infty) + \sum_{k=0}^{n-1} \frac{(A_k - KB_k)s}{s + p_k} \right] \times \left(\frac{1}{1+\mu} \right). \tag{3.22}$$

For Y_1 and Y_2 to be RC DPAs, the residues at the poles must be positive real, i.e.,

$$\mu A_k + KB_k \geq 0, \quad k = 0, 1, 2, \ldots n-1, \infty \tag{3.23}$$

and

$$A_k - KB_k \geq 0, \quad k = 0, 1, 2, \ldots n-1, \infty. \tag{3.24}$$

Thus, K must be chosen such that (3.23) and (3.24) satisfy for both Y_1 and Y_2 to be RC realizable, that is,

$$K \leq \min \left[\frac{\mu A_k}{B_k^-}, \frac{A_k}{B_k^+} \right], \quad k = 0, 1, 2, \ldots, n-1, \infty. \tag{3.25}$$

Total number of elements: Each of Y_1 and Y_2, as given in (3.21) and (3.22), will require $2(n-1)+2$ elements. However, if K and μ are chosen such that one or more equality conditions in (3.25) hold, the number of elements reduces. Therefore, the total number of elements required is

$$\begin{aligned} N &= \text{total number of elements in } (Y_1, Y_2, Y_3, Y_4) \\ &\quad - (0,\ 1,\ 2,\ 3 \text{ or } 4 \text{ elements depending upon the values of } K \text{ and } \mu \text{ chosen}) \\ &= (4n+2) - (0,\ 1,\ 2,\ 3 \text{ or } 4). \end{aligned} \tag{3.26}$$

Thus, a maximum of four elements can be reduced. The number of elements will lie between $(4n-2)$ and $(4n+2)$.

Example 3.1

Let us consider the realization of all-pass transfer function

$$T(s) = K\frac{(s-1)(s-3)}{(s+1)(s+3)}. \tag{3.27}$$

Choosing $Q(s) = (s+2)$ and subsequently $K = 1/15$ for minimum number of elements, we get from (3.14) and (3.15),

$$Y_1 = \frac{16}{15}s + \frac{8}{5} \tag{3.28}$$

and

$$Y_2 = \frac{14}{15}s + \frac{7}{5} + \frac{s}{s+2}. \tag{3.29}$$

The complete realization of $T(s)$ is given in Fig. 3.3 with normalized elements.

Example 3.2

Let us consider the realization of transfer function

$$T(s) = -K\frac{s(s+3.5)(s+4.5)}{(s+1)(s+3)(s+5)}. \tag{3.30}$$

Let $Q(s) = (s+2)(s+4)$. According to (3.25), $K \leq \min[\mu, 6\mu, \frac{3\mu}{7.5}]$. Choosing $K = \frac{9}{7.5}$ and $\mu = 3$, we get

$$Y_1 = 1.4 + \frac{1.8}{4}s + \frac{0.975}{4}\frac{s}{(s+4)}, \tag{3.31}$$

$$Y_2 = \frac{2.2}{4}s + 0.468 + \frac{3}{4}\frac{s}{(s+2)} + \frac{0.525}{4}\frac{s}{(s+4)}, \tag{3.32}$$

and

$$Y_3 = 3, \quad Y_4 = 1. \tag{3.33}$$

The complete realization of $T(s)$ is given in Fig. 3.4 with normalized elements.

3.2.2 Synthesis II

If $T(s)$ has only *distinct negative real poles*, (3.1) can be expressed after RC:$-RC$ decomposition as

$$T(s) = KY_A - KY_B = \frac{Y_1}{Y_1+Y_2} - (Y_3/Y_4)\frac{Y_2}{Y_1+Y_2}. \tag{3.34}$$

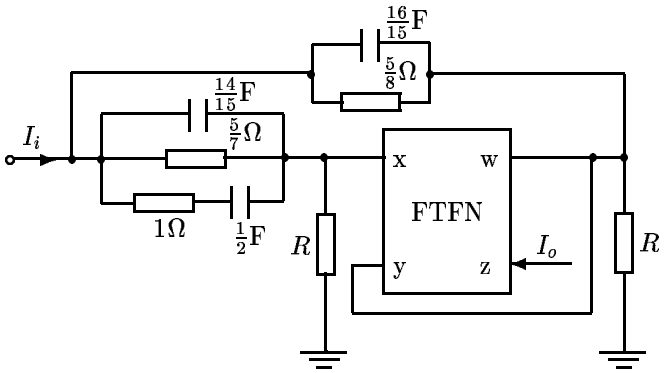


Fig. 3.3. Realization of $T(s)$ given in (3.27) by Synthesis I.

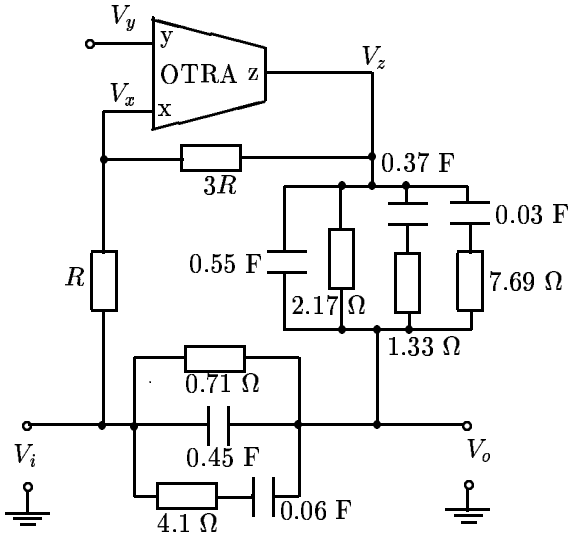


Fig. 3.4. Realization of $T(s)$ given in (3.30) by Synthesis I.

We identify in (3.34)

$$\frac{Y_1}{Y_1+Y_2} = KY_A = K\frac{N_A}{D_A} \tag{3.35}$$

and

$$\left(\frac{Y_3}{Y_4}\right)\frac{Y_2}{Y_1+Y_2} = KY_B = K\frac{N_B}{D_B}. \tag{3.36}$$

From (3.35) and (3.36)

$$\beta_1 = \frac{Y_1}{Y_2} = \frac{KY_A}{1-KY_A} = \frac{KN_A}{D_A-KN_A} \tag{3.37}$$

and

$$\beta_2 = \frac{Y_3}{Y_4} = \frac{KY_B}{1-KY_A} = K\left[\frac{N_B}{D_B}\right]\left[\frac{D_A}{D_A-KN_A}\right]. \tag{3.38}$$

Y_1 and Y_2 can be identified as DPAs from (3.37), if the poles and zeros of β_1 arranged in pairs starting from the rightmost pair, each pair consists of a pole and a zero in

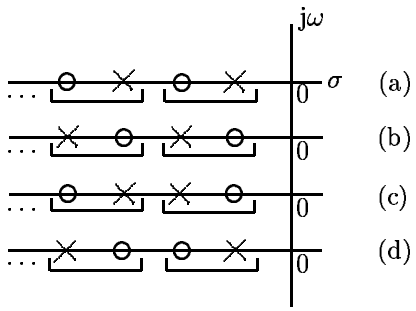


Fig. 3.5. Admissible pole-zero patterns.

either order [67]. The four admissible pole-zero patterns are shown in Fig. 3.5. In pattern (c) [(d)], it may be noted that the two consequtive poles [zeros] may overlap. Y_3 and Y_4 can be identified as DPAs, if the pole-zero pattern of β_2 is one of the 4 cases shown in Fig. 3.5. The zeros of β_1 are the zeros of Y_A and the poles of β_1 are the roots of the equation $D_A - KN_A = 0$. The root-loci start from the poles of Y_A when $K = 0$ and terminate into the zeros of Y_A when $K = \infty$. Thus, by taking K sufficiently small, all the poles of β_1 can be made to lie on the negative real axis. Thus, the pole-zero pattern would be as type (b) in Fig. 3.5. Here, the number of poles (including the pole at infinity) of β_1 equals the number of zeros of Y_A.

One set of poles and zeros of β_2 are the poles and zeros of Y_B and has the pattern as type (b) in Fig. 3.5. The other set of poles and zeros are due to the zeros of $D_A - KN_A$ (which are the same as the poles of β_1) and the zeros of D_A, respectively. Thus, this set will also have a pole-zero pattern as type (b) in Fig. 3.5. It may be possible that the overall pole-zero pattern of β_2 may not match with any one of those shown in Fig. 3.5. For example, if

$$T(s) = K\frac{s - 1/3}{(s+1)(s+3)}, \tag{3.39}$$

β_2 has the zeros at –1/2, and –1 and poles at –3, and anywhere between –1 and ∞ (depending upon the value of K chosen) which is different than what are shown in Fig. 3.5.

Thus, Y_1, Y_2 can always be identified as *RC* DPAs from β_1, but Y_3, Y_4 cannot always be identified as *RC* DPAs from β_2.

Total number of elements: If n_1 (n_2) represents the number of poles in β_1 (β_2), then the total number of elements required for Y_1 and Y_2 (Y_3 and Y_4) will be $(2n_1+2)$

[67]. However, the number of elements will reduce by one if a zero (pole) of β_1 or β_2 happens to be at the origin (infinity) after choosing a suitable value of K. Thus, the total number of elements required is

$$\begin{aligned} N &= (2n_1+2)+(2n_2+2)-2(\text{if a pole in } \beta_1 \text{ or } \beta_2 \text{ is at } \infty) \\ &\quad -1(\text{if a zero of } \beta_1 \text{ is at } 0)-1(\text{if a zero of } \beta_2 \text{ is at } 0) \\ &= 2n_1+2n_2+4-(0,1,2,3, \text{ or } 4). \end{aligned} \tag{3.40}$$

Thus, the total number of elements will be from $2n_1+2n_2$ to $2n_1+2n_2+4$.

Alternative realization can be obtained by having RC:$-RC$ decomposition in terms of RC driving point impedances.

Example 3.3

Let us consider the realization of the same all-pass transfer function given by (3.27). From (3.27)

$$T(s) = K\left[\frac{5s+3}{s+3}-\frac{4s}{s+1}\right]. \tag{3.41}$$

From (3.37)

$$\frac{Y_1}{Y_2} = \frac{K(5s+3)}{s(1-5K)+3(1-K)}. \tag{3.42}$$

Choosing K=1/5, for minimum number of elements, we get

$$\frac{Y_1}{Y_2} = \frac{5(s+3/5)}{12}. \tag{3.43}$$

One possible identification is

$$Y_1 = \frac{5(s+3/5)}{12} \quad \text{and} \quad Y_2 = 1. \tag{3.44}$$

From (3.38), we get

$$\frac{Y_3}{Y_4} = \frac{s(s+3)}{3(s+1)}. \tag{3.45}$$

One possible identification is

$$Y_3 = \frac{s(s+3)}{3(s+1)} \quad \text{and} \quad Y_4 = 1. \tag{3.46}$$

The complete realization of $T(s)$ is given in Fig. 3.6 with normalized elements.

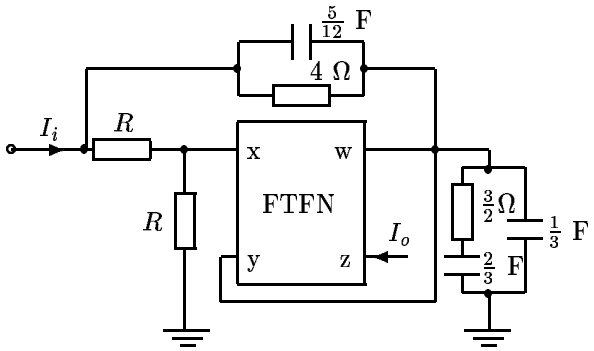


Fig. 3.6. Realization of $T(s)$ given in (3.27) by Synthesis II.

3.2.3 Synthesis III

Let

$$Y_1 = (1-K)G \quad \text{and} \quad Y_2 = KG. \tag{3.47}$$

Then, (3.1) gives

$$K\frac{N(s)}{D(s)} = (1-K) - K\frac{Y_3}{Y_4}. \tag{3.48}$$

Thus,

$$\beta_2 = \frac{Y_3}{Y_4} = \frac{(1-K)D(s) - KN(s)}{KD(s)}. \tag{3.49}$$

It may be noted that the poles of β_2 are the poles of $T(s)$. Zeros of β_2 are the roots of

$$(1-K)D(s) - KN(s) = 0. \tag{3.50}$$

The root-loci start from the zeros of $D(s)$, i.e., the poles of $T(s)$, when $K = 0$ and terminate on the zeros of $N(s)$ when $K = 1$. Thus, β_2 can be made to have one of the pole-zero patterns shown in Fig. 3.5 if the poles of $T(s)$ are negative real of multiplicity not greater than 2 and the two root-loci starting from any of the multiple poles do not break away leaving the negative real axis. For example,

$$T(s) = K\frac{s-1}{(s+1)^2} \tag{3.51}$$

will not yield any of the pole-zero patterns shown in Fig. 3.5. However, in such cases, the difficulty can be overcome by realizing $-T(s)$ instead of $T(s)$.

Thus, choosing suitable value of K, Y_3 and Y_4 can always be identified as RC DPAs from β_2 for any $T(s)$ which has negative real poles of multiplicity not greater than 2.

If the admittances Y_3 and Y_4 are synthesized using Foster second (parallel) form, all the capacitors can be grounded and the total capacitance will be minimum [17]. Such realizations are attractive for fabrication in IC technology.

Total number of elements: Here, Y_3 and Y_4 can be realized by $(n+1)$ elements. It may be possible that a choice of K may force the lowest (highest) critical frequency in β_2 to move to origin (infinity). This will help in reducing 2 elements. The choice of $K = 1$ leads to $\frac{Y_1}{Y_2} = 0$. This will further help in removing Y_1 ($Y_1 = 0$) and Y_2 ($Y_2 = \infty$). Thus, the total number elements can be reduced maximum by 4. Therefore, the total number of elements required for realizing $T(s)$ is

$$\begin{aligned} N &= \text{elements in } (Y_1 \text{ and } Y_2) \\ &\quad + \text{elements in } (Y_3 \text{ and } Y_4) - (0, 1, 2, 3 \text{ or } 4) \\ &= 2n + 4 - (0, 1, 2, 3 \text{ or } 4). \end{aligned} \tag{3.52}$$

Thus, the total number of elements can be $2n$ to $2n + 4$.

It can be noted from (3.26), (3.40), and (3.52) that the Synthesis III requires the least number of elements for $n > 1$.

Example 3.4

Let us consider the realization of the same all-pass transfer function given by (3.27). From (3.49)

$$\frac{Y_3}{Y_4} = \frac{(1-K)(s^2+4s+3) - K(s^2-4s+3)}{K(s^2+4s+3)}. \tag{3.53}$$

Choosing $K = 1/2$,

$$\frac{Y_3}{Y_4} = \frac{8s}{(s+1)(s+3)}. \tag{3.54}$$

One possible identification is

$$Y_3 = \frac{8s}{s+1} \quad \text{and} \quad Y_4 = (s+3). \tag{3.55}$$

Complete realization is shown in Fig. 3.7 with normalized elements. The same method can be used for the realization of transfer function using OTRA.

Example 3.5

Let us consider the realization of transfer function given by (3.30)

$$T(s) = -K\frac{s(s+3.5)(s+4.5)}{(s+1)(s+3)(s+5)}. \tag{3.56}$$

From (3.49)

$$\frac{Y_3}{Y_4} = \frac{s^3 + (9-K)s^2 + (23 - 7.25K)s + (15 - 15K)}{K(s^3 + 9s^2 + 23s + 15)}. \tag{3.57}$$

The maximum possible value of $K = 1$ forces the lowest critical frequency to origin as shown in Fig. 3.8 and thus helps in reduction of number of elements. This choice of K leads to $\frac{Y_1}{Y_2} = 0$, thus further helps in removal of Y_1 and Y_2. Therefore, choosing $K = 1$,

$$\frac{Y_3}{Y_4} = \frac{s(s + 3.5)(s + 4.5)}{(s + 1)(s + 3)(s + 5)}. \tag{3.58}$$

One possible identification is

$$Y_3 = \frac{s(s + 3.5)}{(s + 1)(s + 5)} \quad \text{and} \quad Y_4 = \frac{(s + 3)}{(s + 4.5)}. \tag{3.59}$$

The complete realization is shown in Fig. 3.9 with normalized elements.

Example 3.6

Let us consider the all-pass transfer function

$$T(s) = K\frac{(s-1)^2}{(s+1)^2}. \tag{3.60}$$

This cannot be realized by Synthesis I and II because of multiple poles. From (3.49)

$$\frac{Y_3}{Y_4} = \frac{(s+1)^2 - 2K(s-1)^2}{(s+1)^2}. \tag{3.61}$$

Choosing K=1/2, we get

$$\frac{Y_3}{Y_4} = \frac{4s}{(s+1)^2}. \tag{3.62}$$

One possible identification is

$$Y_3 = \frac{4s}{s+1} \quad \text{and} \quad Y_4 = s + 1. \tag{3.63}$$

The complete realization of $T(s)$ using FTFN and OTRA is given in Fig. 3.10 with normalized elements.

3.3 Realization of stable transfer functions employing CM building blocks

The synthesis procedures discussed in earlier section are restricted to the transfer functions with distinct negative real poles only and therefore, are restricted to low Q

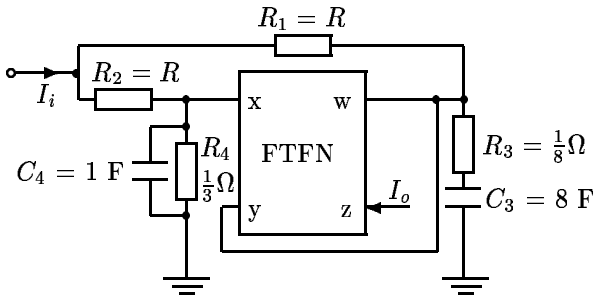


Fig. 3.7. Realization of $T(s)$ given in (3.27) by Synthesis III.

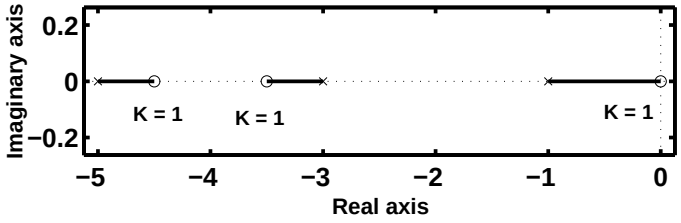


Fig. 3.8. Zero-Loci of $\frac{Y_3}{Y_4}$.

values. To overcome this drawback, a Synthesis III is extended further as follows so as to realize any stable current/voltage transfer function of any order with only one active element.

3.3.1 Synthesis IV

Let us consider the configuration of Fig. 3.2 as shown in Fig. 3.11 where Y_3 and Y_4 are replaced by 3-terminal networks $\mathrm{N_a}$ and $\mathrm{N_b}$, respectively. Let

$$T(s) = K\frac{N(s)}{D(s)} = K\frac{\sum_{i=0}^{n} a_i s^i}{\sum_{j=0}^{n} b_j s^j} \tag{3.64}$$

where zeros of $T(s)$ are located anywhere in the s plane and those of $D(s)$ are in the open left-half plane.

Let, y_a and y_b be the short-circuit transfer admittances of the networks $\mathrm{N_a}$ and $\mathrm{N_b}$, respectively. Then

$$T(s) = -K\frac{y_a}{y_b} + (1-K) \tag{3.65}$$

which gives

$$\gamma = \frac{y_a}{y_b} = \frac{-KN(s) + (1-K)D(s)}{KD(s)} \tag{3.66}$$

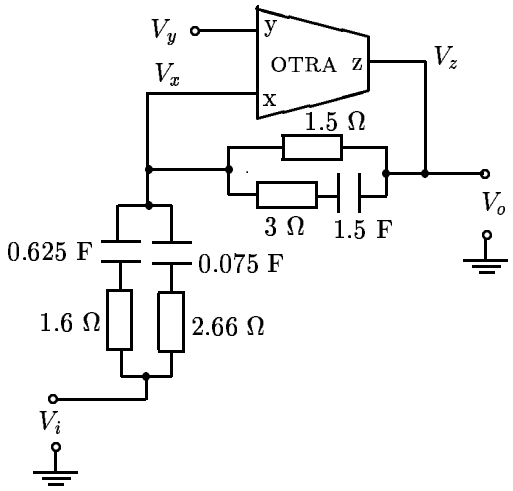


Fig. 3.9. Realization of $T(s)$ given in (3.30) using Synthesis III.

$$\gamma = \frac{y_a}{y_b} = \frac{\sum_{j=0}^{n} c_j s^j}{KD(s)} \tag{3.67}$$

$$\gamma = \frac{y_a}{y_b} = \frac{\sum_{j=0}^{n} c_j s^j / Q(s)}{KD(s)/Q(s)} \tag{3.68}$$

where

$$c_j = -Ka_j + (1-K)b_j, \quad j = 0, 1, \ldots, n, \tag{3.69}$$

$$Q(s) = \Pi_{i=1}^{m}(s + a_i), \tag{3.70}$$

a_is are distinct, real and positive and m is chosen to yield a realization with the minimum number of elements.

Poles of γ are the same as those of T, while the zeros are shifted to new locations determined by K. The loci of these zeros start at $K = 0$ from the zeros of $D(s)$ which are in the open left half plane, and end at $K = 1$ on the zeros of $N(s)$. Thus, by judicious choice of K, in the range

$$0 < K \leq 1, \tag{3.71}$$

the locations of zeros of γ can be controlled. The zeros will, however, lie in the open left half plane, if

$$0 \leq c_j \leq b_j. \tag{3.72}$$

From (3.69), $c_j \geq 0$, if

$$K \leq \frac{1}{1 + R_n} \tag{3.73}$$

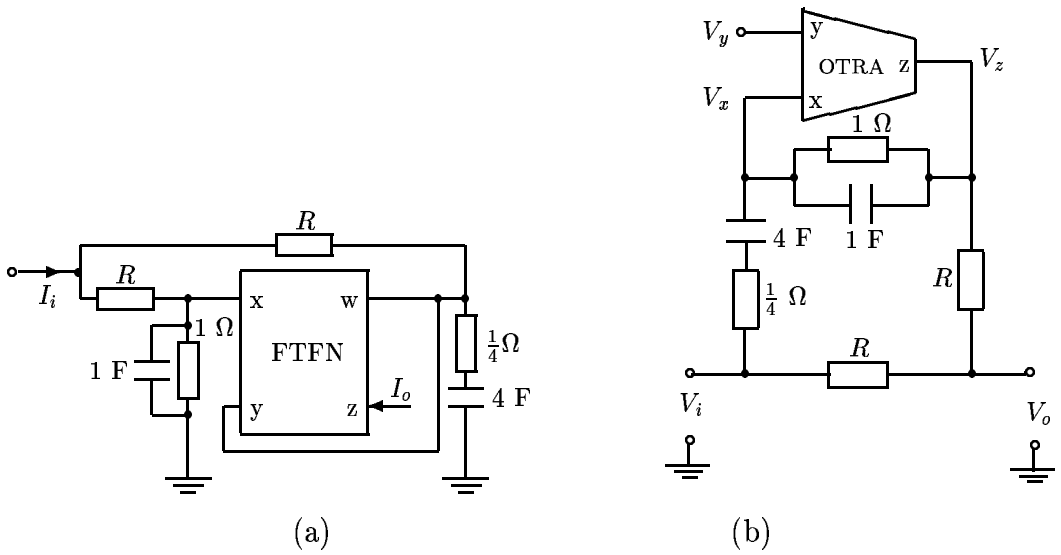


Fig. 3.10. Realization of $T(s)$ given in (3.60) using (a) FTFN and (b) OTRA.

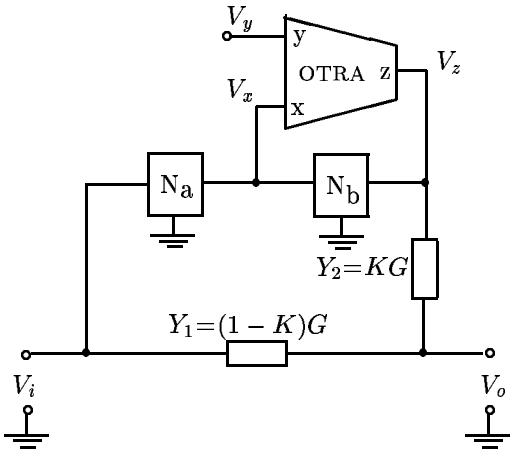


Fig. 3.11. Modified circuit configuration of Fig. 3.2.

where R_n is the maximum value amongst the magnitude ratios of negative a_is and the corresponding b_js in $T(s)$. In view of (3.73), condition in (3.71) can always be satisfied.

After choosing K as per the condition in (3.73), y_a and y_b should be identified such that all the negative real poles (zeros) present in γ are included as the poles of y_a (y_b). They are synthesized as single or parallel RC ladder networks [1], [111] after choosing suitable $Q(s)$. Since y_a and y_b do not have negative numerator coefficients, polynomial augmentation is not necessary and hence they will require much less number of elements.

3.3.2 Design of an nth order all-pass transfer function

Let the nth-order all-pass transfer function be expressed as

$$T(s) = K\frac{D(-s)}{D(s)} = K\left[\frac{\sum_{i=0}^{n} a_i(-s)^i}{\sum_{i=0}^{n} a_i s^i}\right]. \tag{3.74}$$

From (3.68)

$$\begin{aligned}\frac{y_a}{y_b} &= \frac{(1-2K)\sum_{k=1}^{p} a_{2k-2}s^{2k-2}}{KD(s)} \\ &+ \frac{\sum_{k=1}^{q} a_{2k-1}s^{2k-1}}{KD(s)}\end{aligned} \tag{3.75}$$

where $p = q = \frac{n+1}{2}$ for n odd and $p = \frac{n}{2}+1$, $q = \frac{n}{2}$ for n even.

Choosing the maximum possible value of K as $1/2$ as per (3.73), we get,

$$\gamma = \frac{y_a}{y_b} = 2\left[\frac{\sum_{k=1}^{q} a_{2k-1}s^{2k-1}}{D(s)}\right] \tag{3.76}$$

$$\gamma = \frac{y_a}{y_b} = 2\left[\frac{\sum_{k=1}^{q} a_{2k-1}s^{2k-1}/Q(s)}{D(s)/Q(s)}\right]. \tag{3.77}$$

Now y_a and y_b can be identified and realized by RC networks after choosing $Q(s)$ suitably.

When $K = 0.5$, numerator polynomial of γ is an odd polynomial. Hence all the zeros of $\frac{y_a}{y_b}$ will be located on the imaginary axis with one at $s = 0$. When n is odd, $K < 0.5$ will shift the latter zero to $s = -\sigma$ (real) (say). This zero can be cancelled by including a similar factor in $Q(s)$, reducing the elements by two. However, the number of elements can be reduced further if (3.74) can be rearranged as

$$T(s) = K\left[\frac{[\sum_{i=0}^{n-1} a_{i+1}(-s)^i]}{[\sum_{i=0}^{n-1} a_{i+1}(s)^i]}\right]\frac{(\sigma_1 - s)}{(\sigma_1 + s)} \tag{3.78}$$

$$T(s) = K\left[\frac{[\sum_{i=0}^{n-1} a_{i+1}(-s)^i]}{D_1}\right]\frac{(\sigma_1 - s)}{(\sigma_1 + s)}. \tag{3.79}$$

Using (3.68) and choosing

$$K = \frac{a_{n-1}}{2(a_{n-1} + \sigma_1 a_n)}, \tag{3.80}$$

we get

$$\frac{y_a}{y_b} = A\frac{[a_n s^{n-1}(s+\sigma_1) + \sum_{m=1}^{\frac{n-1}{2}} R_m s^{2m-2}(s+\delta_m)]/Q(s)}{(s+\sigma_1)D_1/Q(s)} \tag{3.81}$$

where

$$A = \frac{2(a_{n-1} + \sigma_1 a_n)}{a_{n-1}}, \tag{3.82}$$

$$\delta_m = \left(\frac{a_{2m-2} + \sigma_1 a_{2m-1}}{a_{2m-1} + \sigma_1 a_{2m}}\right)\left(\frac{\sigma_1 a_n}{a_{n-1} + \sigma_1 a_n}\right), \tag{3.83}$$

$R_m = (a_{2m-1} + \sigma_1 a_{2m})$ for $m = 1$ to $\frac{n-1}{2}$, and $a_0 = 0$. Here, the factor $(s + \sigma_1)$ in the first term created by the choice of K given by (3.80), gets cancelled by the $(s + \sigma_1)$ factor in $D(s)$. This will reduce the number of elements. Choosing

$$Q(s) = \Pi_{m=1}^{\frac{n-1}{2}}(s + \delta_m), \tag{3.84}$$

one can identify

$$y_a = A\left[\frac{a_n s^{n-1}}{Q(s)} + \left\{\frac{1}{(s+\sigma_1)}\sum_{m=1}^{\frac{n-1}{2}}\frac{R_m s^{2m-2}(s+\delta_m)}{\Pi_{m=1}^{\frac{n-1}{2}}(s+\delta_m)}\right\}\right], \tag{3.85}$$

$$y_b = \frac{D_1}{\Pi_{m=1}^{\frac{n-1}{2}}(s+\delta_m)}. \tag{3.86}$$

It may be noted that there is a cancellation of $(s + \delta_i)$ in the ith term inside $\{\ \}$ brackets by $(s+\delta_i)$ factor in $Q(s)$. Such a cancellation is not possible when n is even. This is illustrated with an example.

Example 3.7

Let us consider a 3rd order all-pass transfer function

$$T(s) = K\frac{(1 - s + s^2)(1 - s)}{(1 + s + s^2)(1 + s)}. \tag{3.87}$$

Here $|T(s)| = K$ and

$$\phi = -2\pi\eta - 2\tan^{-1}\omega\left(\frac{2 - \omega^2}{1 - 2\omega^2}\right) \tag{3.88}$$

where $\eta = 0$ for $\omega \leq \frac{1}{\sqrt{2}}$ and $\eta = 1$ for $\omega > \frac{1}{\sqrt{2}}$. From (3.68)

$$\frac{y_a}{y_b} = \frac{s^3 + 2(1 - 2K)s^2 + 2s + (1 - 2K)}{K(s^3 + 2s^2 + 2s + 1)}. \tag{3.89}$$

From the zero-loci of $\frac{y_a}{y_b}$ shown in Fig. 3.12, one can see that one loci is always on the negative real axis and the other two are having complex roots with negative real part and crosses imaginary axis when $K = 0.5$.

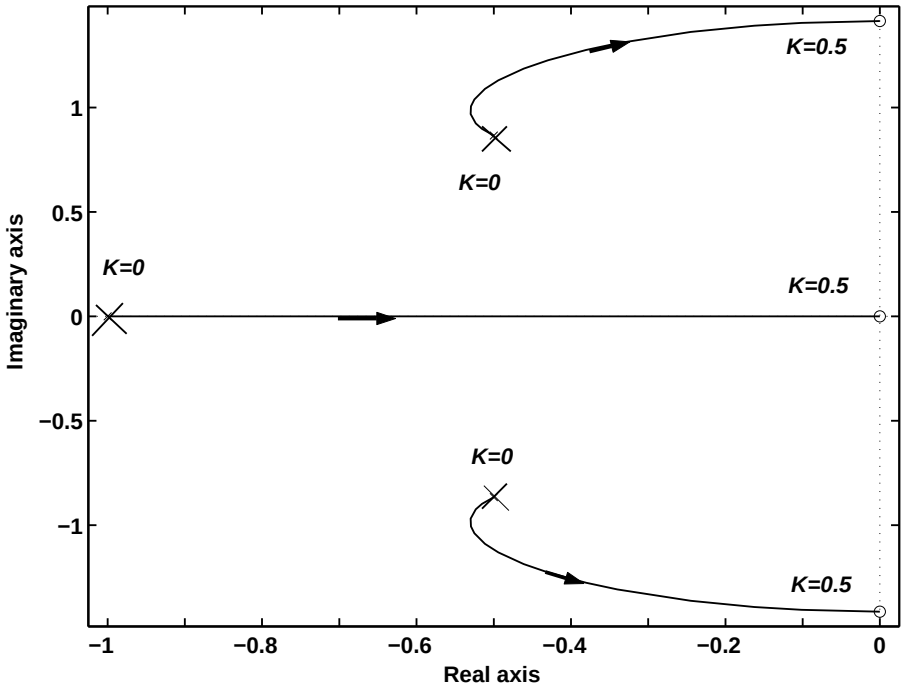


Fig. 3.12. Zero-Loci of $\frac{y_a}{y_b}$ given in (3.89).

Case I: For $K = \frac{1}{2}$, we get from (3.89)

$$\frac{y_a}{y_b} = \frac{2s(s^2+2)}{(s^2+s+1)(1+s)}. \tag{3.90}$$

Now, identifying

$$y_a = \frac{2s(s^2+2)}{(s+1)Q(s)} = \frac{2s^3}{(s+1)Q(s)} + \frac{4s}{(s+1)Q(s)}, \tag{3.91}$$

$$y_b = \frac{s^2+s+1}{Q(s)} \tag{3.92}$$

and choosing $Q(s) = (s + \frac{1}{4})$, the complete realization of (3.87) is shown in Fig. 3.13(a). Here, all the component values are normalized one. The total number of passive elements required is 16.

Case II: For $K < \frac{1}{2}$, all the zeros have negative real parts. For example, when $K = 0.25$, we get from (3.89)

$$\frac{y_a}{y_b} = \frac{4(s+0.2799)(s^2+0.7221s+1.8)}{(s^2+s+1)(s+1)}. \tag{3.93}$$

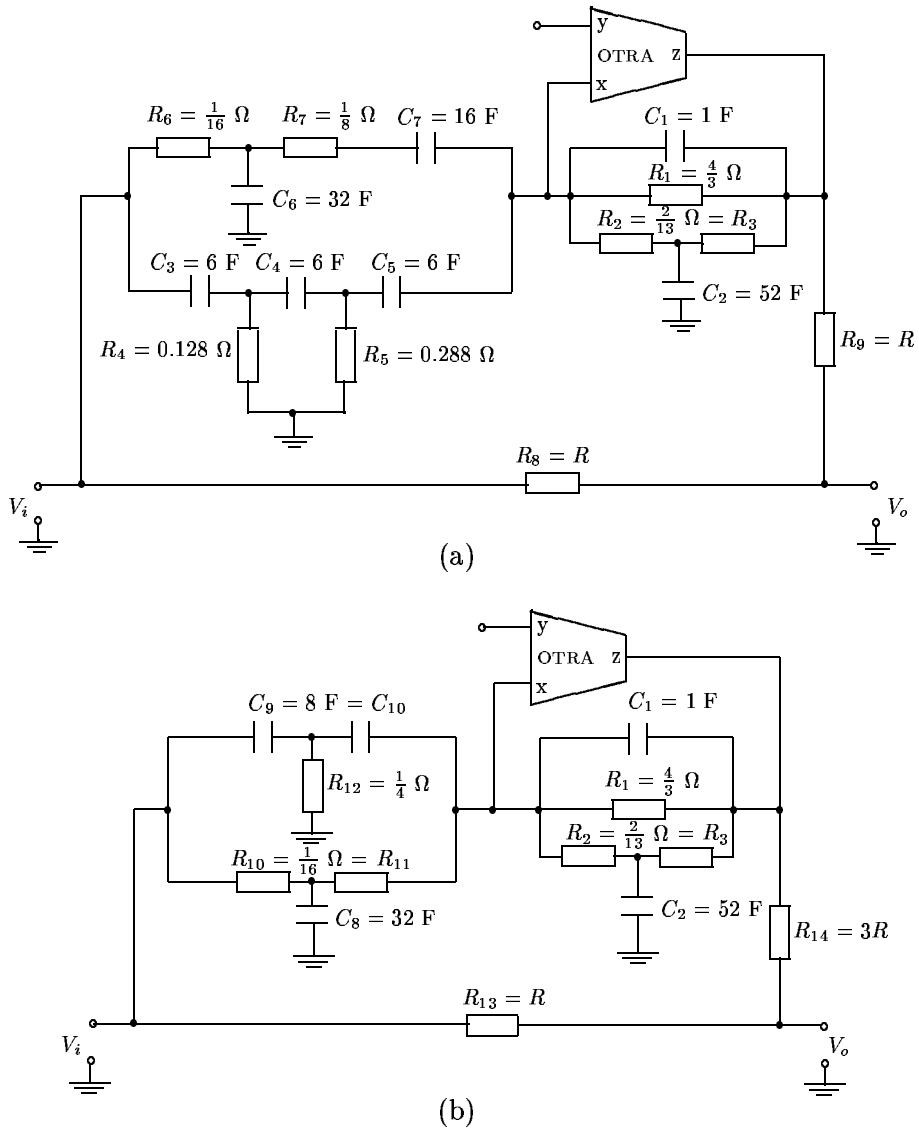


Fig. 3.13. Realization of $T(s)$ given in (3.87) for (a) $K = 1/2$ and (b) $K = 1/4$.

Identifying

$$y_a = \frac{4(s+0.2779)(s^2+0.7221s+1.8)}{(s+1)Q(s)}, \tag{3.94}$$

$$y_b = \frac{s^2+s+1}{Q(s)} \tag{3.95}$$

and choosing $Q(s) = (s + 0.2779)$, the complete realization requires 14 passive elements.

More number of elements can, however, be reduced. Choosing $K = \frac{1}{4}$ according to (3.80), (3.81) gives

$$\frac{y_a}{y_b} = \frac{\left[4s^2(s+1) + 8(s+\frac{1}{4})\right]/Q(s)}{(s^2+s+1)(1+s)/Q(s)}. \tag{3.96}$$

Identifying

$$y_a = \frac{4s^2(s+1)+8(s+\frac{1}{4})}{(s+1)Q(s)} = \frac{4s^2}{Q(s)} + \frac{8(s+\frac{1}{4})}{(s+1)Q(s)}, \tag{3.97}$$

$$y_b = \frac{s^2+s+1}{Q(s)}, \tag{3.98}$$

and choosing $Q(s) = (s + \frac{1}{4})$, according to (3.84), for minimum number of elements, the complete realization will require 13 passive elements as shown in Fig. 3.13(b). Here, all the component values are normalized one. It may be noted that Acar and Ozoguz's method [30] would have required 4 active and 14 passive elements to realize the same all-pass function.

3.4 Equal-valued grounded-capacitor realization of low-pass filters

Among many high-Q, low-pass filters reported, equal-valued grounded capacitor (EVGC) filters proposed by Sallen and Key [112], Rao and Murti [113] and Soliman [114] are attractive from the view point of fabrication in IC form. However, they require two differential input OAs and do not possess a simple arrangment for the gain adjustment and/or for accommodating the source conductance. Here, we introduce single CFA based EVGC low-pass filters in voltage mode and current mode with extremely low sensitivities.

3.4.1 Filter realization

Let us consider the VM low-pass filter shown in Fig. 3.14, where CFA has the terminal characteristics [25]

$$\begin{bmatrix} V_x \\ I_y \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ I_w \end{bmatrix} \tag{3.99}$$

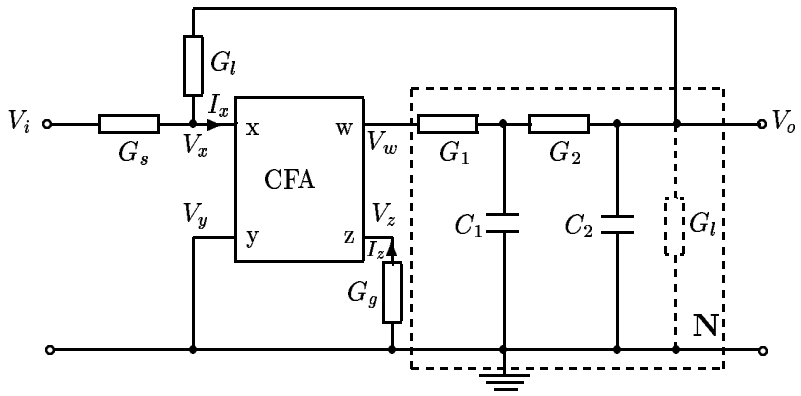


Fig. 3.14. VM low-pass filter.

and N is a three terminal RC network with the voltage transfer function (assuming $R_1 = R_2 = R$ and $C_1 = C_2 = C$)

$$T_o(s) = \frac{H}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}, \qquad Q_p < \frac{1}{2} \tag{3.100}$$

where

$$H = \frac{G^2}{C^2}, \tag{3.101}$$

$$\frac{\omega_p}{Q_p} = \frac{3G + G_l}{C} = \alpha, \tag{3.102}$$

and

$$\omega_p^2 = \frac{G^2 + 2GG_l}{C^2} = \beta. \tag{3.103}$$

The overall transfer function of the network can be expressed as

$$T(s) = -\frac{K}{s^2 + \frac{\omega_a}{Q_a}s + \omega_a^2} \tag{3.104}$$

where

$$\frac{\omega_a}{Q_a} = \frac{\omega_p}{Q_p}, \tag{3.105}$$

$$\omega_a^2 = \omega_p^2 + H\frac{G_l}{G_g}, \tag{3.106}$$

and

$$K = H\frac{G_s}{G_g}. \tag{3.107}$$

Thus, from the given filter function, ω_p and Q_p can be obtained using (3.105) and (3.106) such that $Q_p < \frac{1}{2}$ by choosing $H\frac{G_l}{G_g}$ suitably. Then $T_o(s)$ can be realized as follows.

Assuming $C = 1$, and solving for G and G_l from (3.102) and (3.103), we get

$$G = \frac{\alpha}{5} \pm \left[\frac{\alpha^2}{25} - \frac{\beta}{5}\right]^{1/2} \tag{3.108}$$

and

$$G_l = \alpha - 3G. \tag{3.109}$$

It can easily be seen that G and G_l are non-negative real, if

$$\left(\frac{1}{9}, 0\right) < Q_p^2 \leq \frac{1}{5}. \tag{3.110}$$

The two left hand values are, respectively, for the positive and negative signs in (3.108). The realization procedure can now be formulated as follows.

Choose Q_p in accordance with (3.110). Determine ω_p, G, G_l, H, and G_g from (3.105), (3.108), (3.109), (3.101), and (3.106), respectively. Finally, G_s is adjusted in (3.107) for the desired value of K.

3.4.2 Realization with specified K and G_S

From (3.105)-(3.109),

$$\frac{K}{G_s} = \frac{\omega_a^2 - \omega_p^2}{\frac{2\omega_a}{5Q_a} \mp 3\sqrt{\frac{1}{25}\left(\frac{\omega_a}{Q_a}\right)^2 - \frac{1}{5}\omega_p^2}}. \tag{3.111}$$

Thus, for real value of K/G_s, $\omega_p^2 \leq \frac{1}{5}(\frac{\omega_a}{Q_a})^2$. Further, $K/G_s > 0$ when $0 < \omega_p^2 \leq \frac{1}{5}(\frac{\omega_a}{Q_a})^2$ for the positive sign in (3.111) and $\frac{1}{9}(\frac{\omega_a}{Q_a})^2 \leq \omega_p^2 \leq \frac{1}{5}(\frac{\omega_a}{Q_a})^2$ for the negative sign in (3.111). Thus, K/G_s is 1 and ∞ when $\omega_p^2 = 0$ and $\frac{1}{9}(\frac{\omega_a}{Q_a})^2$, respectively. Hence, any value of K/G_s between 1 and ∞ can be realized by suitably choosing the value of ω_p. It is interesting to note that there are two possible values of $\frac{K}{G_s}$ for $\frac{1}{9}(\frac{\omega_a}{Q_a})^2 \leq \omega_p^2 < \frac{1}{5}(\frac{\omega_a}{Q_a})^2$, one with the positive sign and the other with the negative sign in (3.111).

For the specified values of ω_a, Q_a, K, and G_s, the values of ω_p, Q_p, G, G_l, H, and G_g may be determined from (3.111), (3.105), (3.108), (3.109), (3.101), and (3.107), respectively.

As an illustration, let us consider the realization of

$$T(s) = -\frac{K}{s^2 + s + 1}. \tag{3.112}$$

Here, $\omega_a = Q_a = 1$. With these values, (3.111) reduces to

$$\frac{K}{G_s} = \frac{1 - \omega_p^2}{0.4 \mp 3\sqrt{0.04 - 0.2\omega_p^2}}. \tag{3.113}$$

A plot of K/G_s against ω_p^2 is obtained from (3.113) and shown in Fig. 3.15(a). If we choose, $K = 1$ and $G_s = 1/2$, then $\omega_p = Q_p = 1/\sqrt{5}, G = 1/5,\ G_l = 2/5,\ H = 1/25$, and $G_g = 1/50$. The complete realization is shown in Fig. 3.15(b). If the network shown in Fig. 3.15(c), which has the transfer function $\frac{1 - G_s}{s + 1}$, $G_s < 1$, is connected at the input side of the circuit shown in Fig. 3.15(b), the resulting circuit realizes the third order Butterworth low-pass filter. Here, all the component values are normalized one. The conductance G_s in Fig. 3.15(c) represents the loading effect of the following second order filter. The overall gain constant of the filter is $2G_s(1 - G_s)$ which is maximum when $G_s = 1/2$ for $K/G_s = 2$.

3.4.3 Sensitivity analysis

The expressions of ω_a and Q_a for the proposed filter configuration of Fig. 3.14 are given by

$$\omega_a = \left[\frac{(G_1 + G_2)G_l + G_1G_2}{C_1C_2} + \frac{G_1G_2G_l}{C_1C_2G_g}\right]^{1/2} \tag{3.114}$$

and

$$Q_a = \frac{\omega_a}{D}, \quad D = \frac{G_1 + G_2}{C_1} + \frac{G_2 + G_l}{C_2}. \tag{3.115}$$

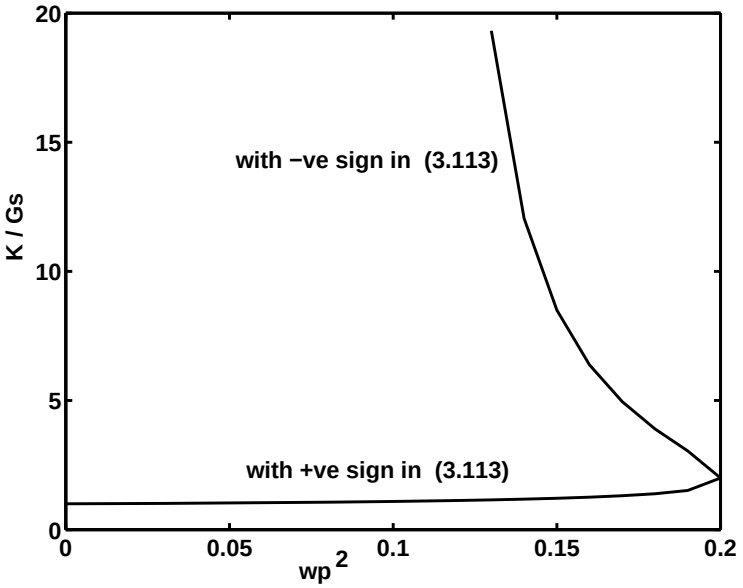
Applying the usual definition of sensitivity

$$S_y^x = \frac{y}{x}\frac{\partial x}{\partial y} \tag{3.116}$$

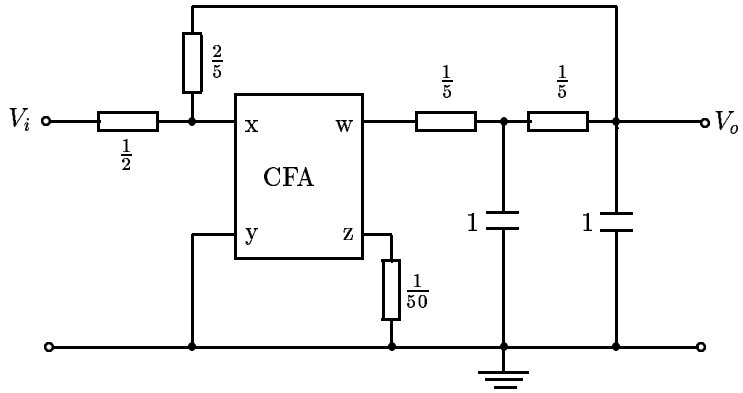
it is found that all the magnitudes of sensitivities are ≤ 0.5. The passive sensitivities for the realization of Fig. 3.15(b) are given in Table 3.1.

3.4.4 CM low-pass filter

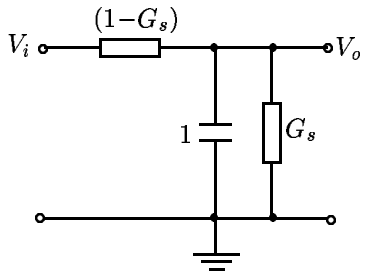
The proposed CM filter circuit is shown in Fig. 3.16. It is interesting to note that the current transfer function I_o/I_i is the same as the voltage transfer function given by (3.104). Hence, both the VM and the CM low-pass filter configurations show the same frequency response and exhibit the same sensitivities.



(a)



(b)



(c)

Fig. 3.15. (a) Plot of $\frac{K}{G_s}$ versus ω_p^2, (b) Realization of $T(s)$ given by (3.112), and (c) Realization of $(1 - G_s)/(s + 1)$.

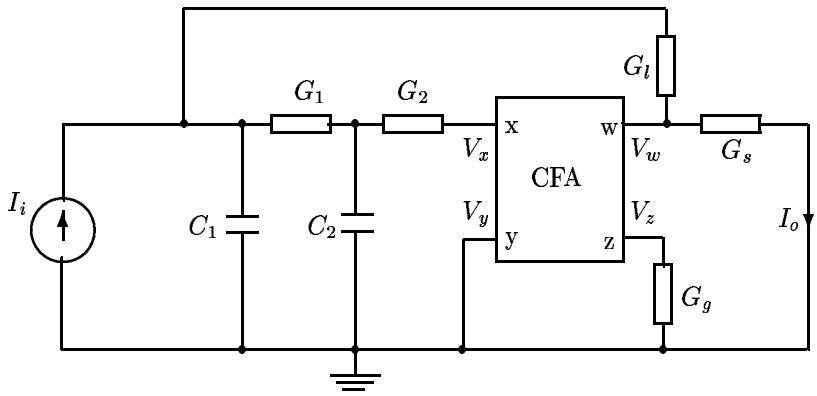


Fig. 3.16. CM low-pass filter configuration.

Table 3.1. Passive sensitivities.

x	y					
	G_1	G_2	G_l	G_g	C_1	C_2
ω_a	0.46	0.46	0.48	–0.40	–0.5	–0.5
Q_a	0.26	0.06	0.08	–0.40	–0.1	0.1

3.5 Simulation results

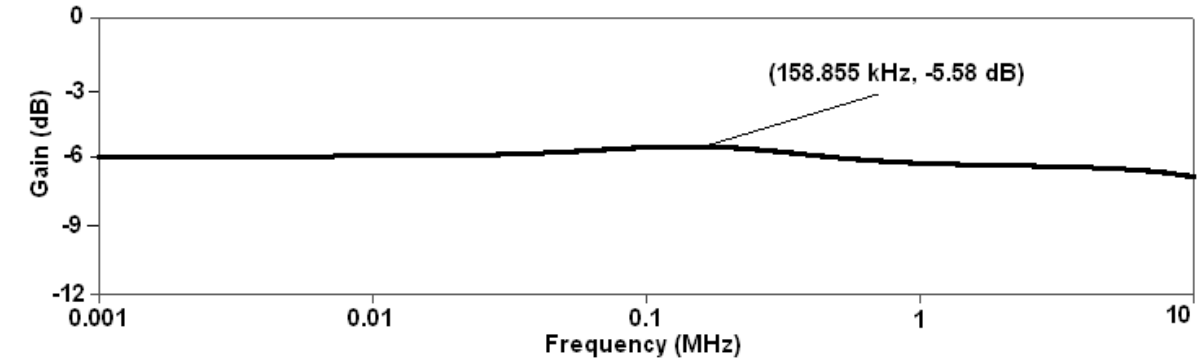
For verification of the theory, all-pass circuit of Fig. 3.7 for a pole frequency of 159 kHz is simulated using PSPICE. The FTFN is implemented with two AD844 as given in [29] with supply voltages of ±12 V. The component values chosen are $C_3 = 400$ pF, $C_4 = 50$ pF, $R = 34.7$ kΩ, $R_3 = 4.3$ kΩ, and $R_4 = 11.5$ kΩ. The gain and phase responses of the simulated circuit are shown in Figs. 3.17(a) and (b), respectively. Phase response is in good agreement with the theory but the magnitude response is flat up to 10 kHz and within ± 3.6% up to 2 MHz. The distortion in the magnitude response after 10 kHz can be justified by the group delay response.

The group delay $D(w)$ for a second order all-pass filter is given by [3] (pp. 399-411)

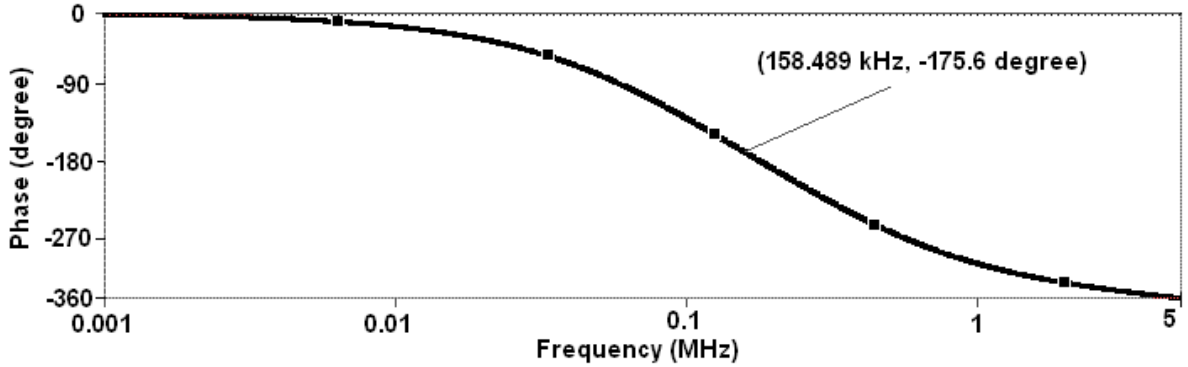
$$D(w) = -\frac{d\theta(w)}{dw} = \frac{1}{w_0}\left[\frac{(2/Q)(1+w_n^2)}{(1-w_n^2)^2 + (w_n/Q)^2}\right] \tag{3.117}$$

where $\theta(w)$ is the phase angle, $w_n = w/w_0$ is the normalized frequency, w_0 is the pole frequency, w is the input frequency, and Q is the quality factor.

The group delay plot of the simulated circuit is shown in Fig. 3.18 and it is in



(a)



(b)

Fig. 3.17. Frequency response of second order all-pass filter shown in Fig. 3.7: (a) Gain response and (b) Phase response.

good agreement with the theoretical plot obtained from (3.117) using MATLAB. The constant group delay up to 10 kHz signifies that all the frequency components in the signal up to 10 kHz are equally delayed without any distortion. The gain, phase, and group delay errors are -7.27%, -2.44%, and -3.62%, respectively, at $f_0 = 159$ kHz.

Both the all-pass circuits of Fig. 3.13 are simulated using PSPICE, with the OTRA realized using commercially available CFAs, AD844s [115]. The element values for a phase shift of -270^0 (middle of the total range) at a frequency 1.59 MHz are: $R_1 = 1.33$ kΩ, $R_2 = R_3 = 153.8$ Ω, $R_4 = 128$ Ω, $R_5 = 288$ Ω, $R_6 = 62.5$ Ω, $R_7 = 125$ Ω, $R_8 = R_9 = 1$ kΩ, $R_{10} = R_{11} = 62.5$ Ω, $R_{12} = 250$ Ω, $R_{13} = 1$ kΩ, $R_{14} = 3$ kΩ, $C_1 = 0.1$ nF, $C_2 = 5.2$ nF, $C_3 = C_4 = C_5 = 0.6$ nF, $C_6 = 3.2$ nF, $C_7 = 1.6$ nF, $C_8 = 3.2$ nF, $C_9 = C_{10} = 0.8$ nF. Realization of the corresponding current transfer function is obtained by VM-to-CM transformation [102]. The simulation results for both the voltage and current transfer functions obtained are identical. The simulation results obtained from the circuits of Figs. 3.13(a) and 3.13(b) are shown in Figs. 3.19

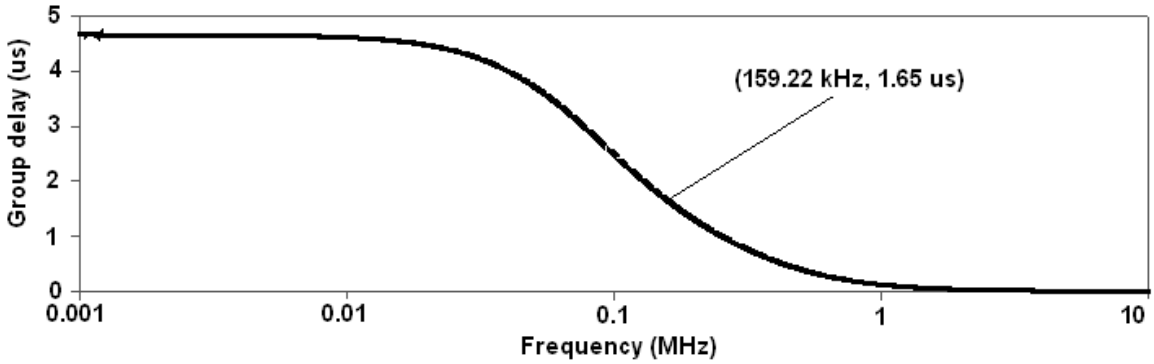


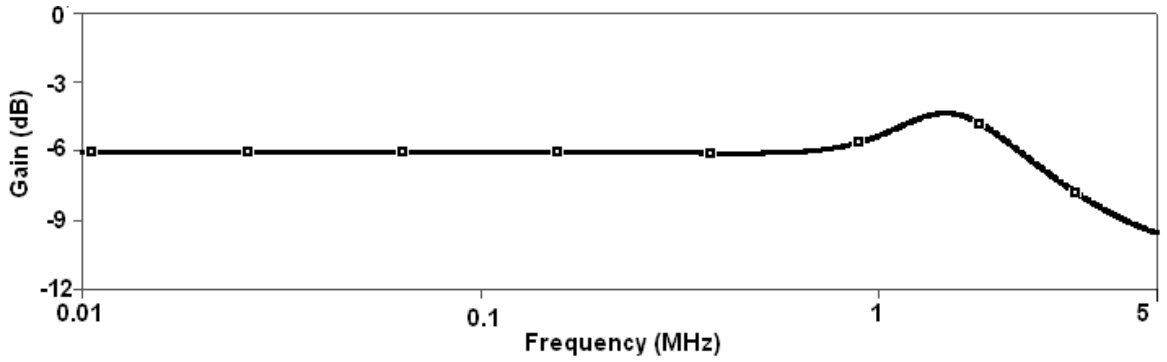
Fig. 3.18. Group delay frequency response of second order all-pass filter shown in Fig. 3.7.

and 3.20, respectively, and are in close agreement with the theoretical ones except for frequencies beyond 5 MHz which could be due to the input resistance of the OTRA [116].

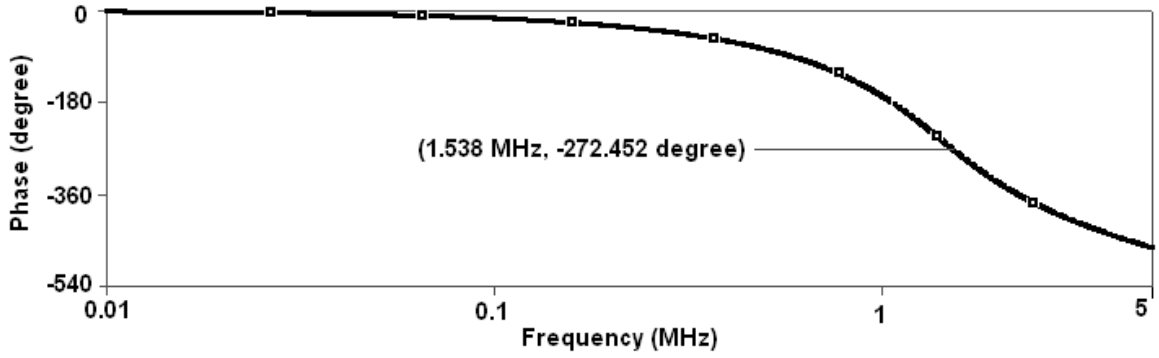
Both the VM and CM third order Butterworth low-pass filters shown in Fig. 3.15 and 3.16, respectively, are designed for $K = 10^{14}$ rad^2/s^2, $R_s = 200\ \Omega$, $\omega_a = 10$ Mrad/s and simulated using PSPICE. The designed components are $R_s = 200\ \Omega$, $R_l = 250\ \Omega$, $R_g = 5$ kΩ, $R = 500\ \Omega$, $C = 1$ nF, and CFA AD844 with ± 15 V supply voltages. The cutoff frequency is increased from low to high value by decreasing the value of the capacitors till the peak starts appearing around the cutoff frequency at 1.59 MHz. Above 1.59 MHz, the response becomes +3 dB at 2.47 MHz and again $-$3dB at 3.54 MHz. Thus the circuit can be used as a low-pass filter for cutoff frequency up to 3.54 MHz. However, for cutoff frequency above 1.59 MHz, the magnitude response in the pass band exhibits a ripple of 3 dB. Results obtained for both VM and CM filters were identical and are shown in Fig. 3.21 for one of them only. The simulation of the filter is also carried out with the high frequency OA LM675 available on the simulator, and the circuit does not work satisfactorily beyond a cutoff frequency of 1 MHz.

3.6 Experimental results

A breadboard prototype circuit of Fig. 3.13(b) was assembled to verify the theoretical analysis and simulated results. The OTRA was constructed with two AD844s as given in Subsection 1.1.5. The circuit elements chosen are $R_1 = 1.5$ kΩ, $R_2 = R_3 = 150\ \Omega$,



(a)



(b)

Fig. 3.19. Frequency response of the third order all-pass filter shown in Fig. 3.13(a): (a) Gain response and (b) Phase response.

$R_{10} = R_{11} = 68\ \Omega$, $R_{12} = 270\ \Omega$, $R_{13} = 1\ \text{k}\Omega$, $R_{14} = 3.3\ \text{k}\Omega$, $C_1 = 0.1$ nF, $C_2 = 4.7$ nF, $C_8 = 3.3$ nF, $C_9 = C_{10} = 1$ nF. The gain plot of the circuit is shown in Fig. 3.22 and it is in close agreement with the simulated one. The slight variation in the gain value may be attributed to the tolerances in the circuit elements.

3.7 Concluding remarks

Four different synthesis procedures for realizing current/voltage transfer functions of any order with negative real poles using only one active device have been given. The Synthesis IV, as presented in Subsection 3.3.1, can realize a transfer function with complex poles too. The circuit of Fig. 3.1 is more general than the previous ones [27], [50], [51] as they realize only specific order filter functions while others [28], [49] use more than one active device.

Synthesis I and II are restricted to a class of transfer functions with distinct

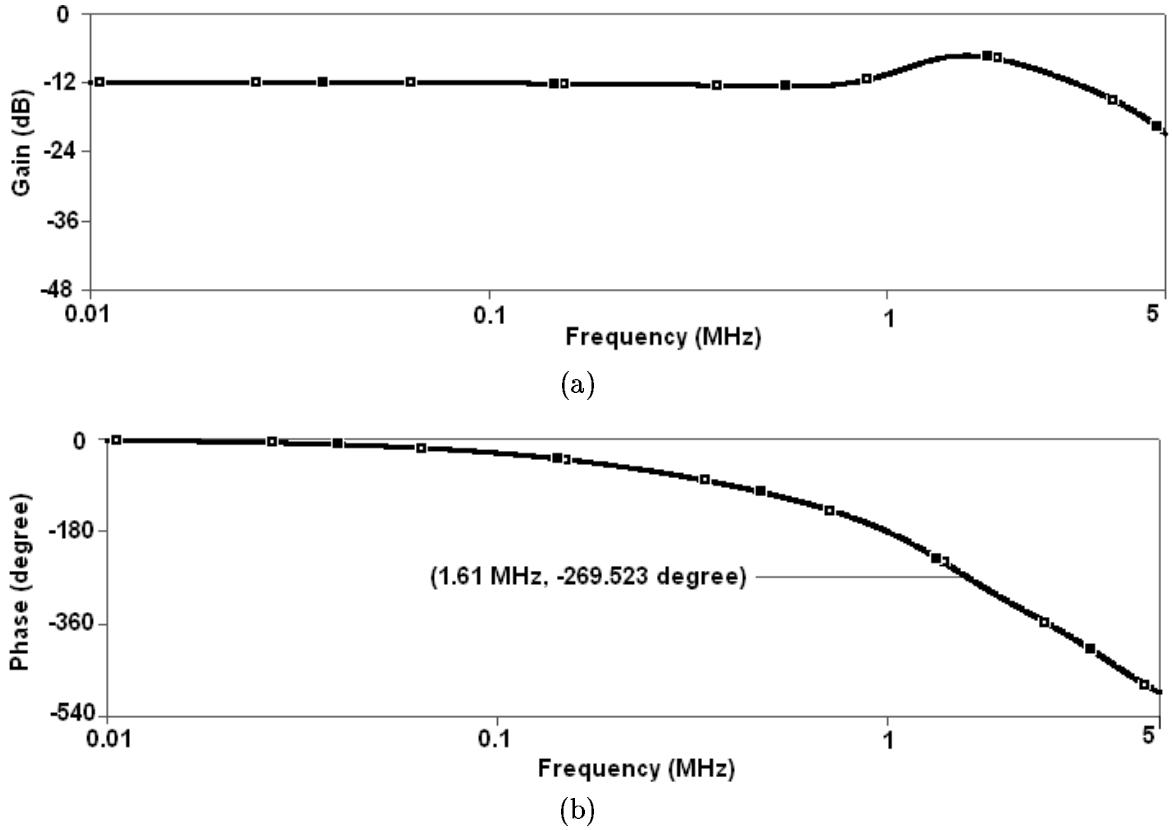


Fig. 3.20. Frequency response of the third order all-pass filter shown in Fig. 3.13(b): (a) Gain response and (b) Phase response.

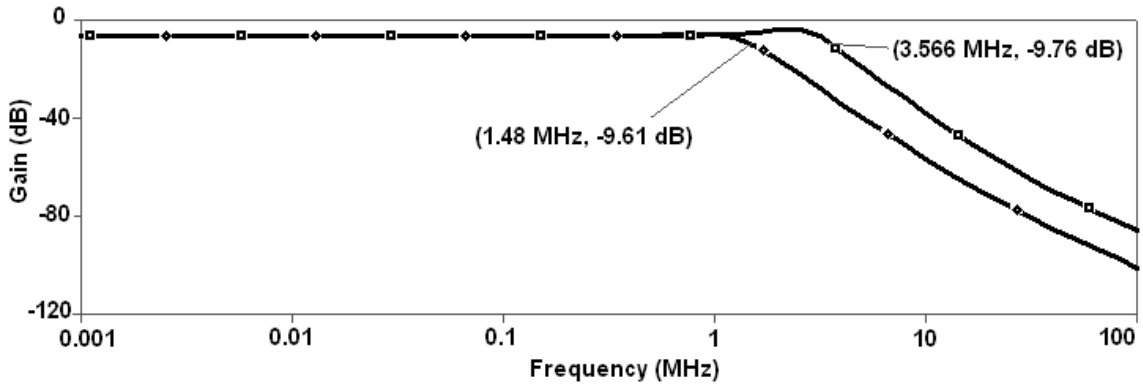


Fig. 3.21. Frequency response of the third order Butterworth low-pass filter shown in Fig. 3.15.

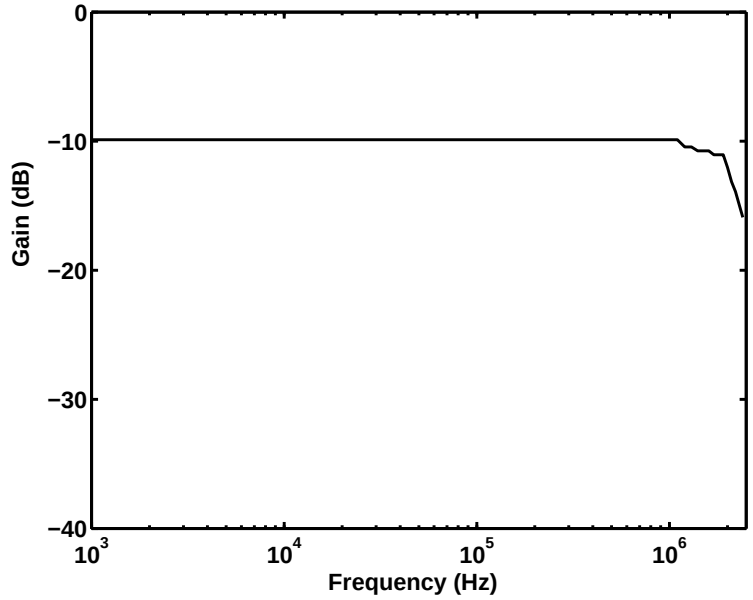


Fig. 3.22. Gain plot of the third order all-pass filter shown in Fig. 3.13(b).

negative real poles only. Synthesis III requires the least number of passive elements and can realize any transfer function with negative real poles of multiplicity not exceeding 2. Further, it can yield a realization with all the capacitors grounded and the total capacitance a minimum, a favourable condition for fabrication in IC technology. Since all the three procedures require 4 passive elements for a *first order* all-pass function, Higashimura's filter [27] should be preferred.

The phase and group time delay responses of the simulated all-pass circuit are in good agreement with theory. The magnitude response is constant up to 10 kHz and is within $\pm$ 3.6% up to 2 MHz.

In Synthesis IV, it is shown that the higher gain constant requires in general a large number of elements. By comparison, Acar and Ozoguz's method requires n additional active elements for an nth order function. The realizations using OTRA are insensitive to input parasitics and, therefore, can work at a much higher frequency.

Finally, EVGC realizations of VM and CM low-pass filters employing only one active device have been introduced. It requires fewer active and/or passive components as compared to the other EVGC low-pass filters [112]-[114]. Besides, any desired gain constant can be adjusted and/or any specified source conductance can be accommodated. The passive sensitivities are extremely low. VM and CM third

order Butterworth filters have been designed and tested using PSPICE and found to work satisfactorily for a cutoff frequency as high as 1.59 MHz, whereas the low-pass filter designed with the high frequency OA, such as LM 675, fails to work beyond 1 MHz.

Chapter 4

EQUAL-VALUED GROUNDED-CAPACITOR LADDER REALIZATION

4.1 Introduction

In this chapter, a systematic method for deriving active *RC* filters from the *RLC* ladder prototypes using the functional relation simulation approach is presented. The resulting filters require a minimum number of capacitors all of which are grounded and, in some cases, they can be made of equal value. If all the driving point impedances are realized in *RC* Foster II form, then these impedances will have minimum total capacitance [17]. Grounded-capacitors allow easy compensation for the parasitic capacitors, latter being in parallel with the grounded capacitors [9]. For thin film fabrication, the use of grounded capacitors eliminates the etching process and reduces the number of gold contacts, thereby improving the circuit reliability [10]. Equal-valued grounded capacitors help saving silicon area and easy processing in IC technology [6], [11], [12] (pp. 10-12), [13]-[15]. For low frequency applications, EVGC realization would facilitate time-multiplexing of all the capacitors and thereby reducing the area on the silicon wafer [16].

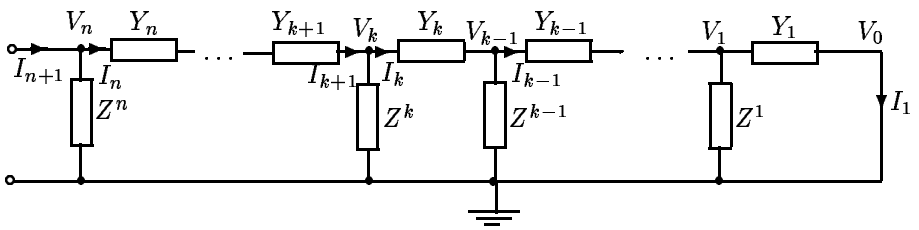


Fig. 4.1. Ladder network in current mode.

4.2 *RC* grounded-capacitor realization of a CM ladder network

A 2-port CM ladder network is shown in Fig. 4.1. We shall develop the simulation for this circuit by simulating the functional relations for various node voltages and branch currents. Simulations of node voltage V_k and branch current I_k are dealt with special attention given to grounded capacitors. To represent the elements in series (shunt) branch and its simulation, subscript k (superscript k) is used. For the simulation of the ladder, we have to simulate the voltage V_k and current I_k. These can be expressed as

$$I_{k+1}Z^k - I_kZ^k = V_k \tag{4.1}$$

and

$$V_kY_k - V_{k-1}Y_k = I_k. \tag{4.2}$$

It may be noted that for the simulation of V_k, we need two branch currents I_k and I_{k+1} and for the simulation of I_k, we need two node voltages V_k and V_{k-1}. Thus the simulations are inter-related. We shall simulate the voltage V_k and current I_k under two cases depending upon the nature of Y_k $(=\frac{1}{Z_k})$ and Z^k $(=\frac{1}{Y^k})$.

4.2.1 Case A

In this case, we have to simulate the voltage V_k and current I_k.

Simulation of V_k: Let the circuit shown in Fig. 4.2 represent the active *RC* simulation of V_k given by (4.1). Analysis of the circuit leads to

$$V_{w1} = V_{z1} = -\frac{I_{z1}}{Y_C} = -\frac{I_{x1}}{Y_C} = -\frac{V_AY_A + V_BY_B + V_{w3}Y_E}{Y_C}, \tag{4.3}$$

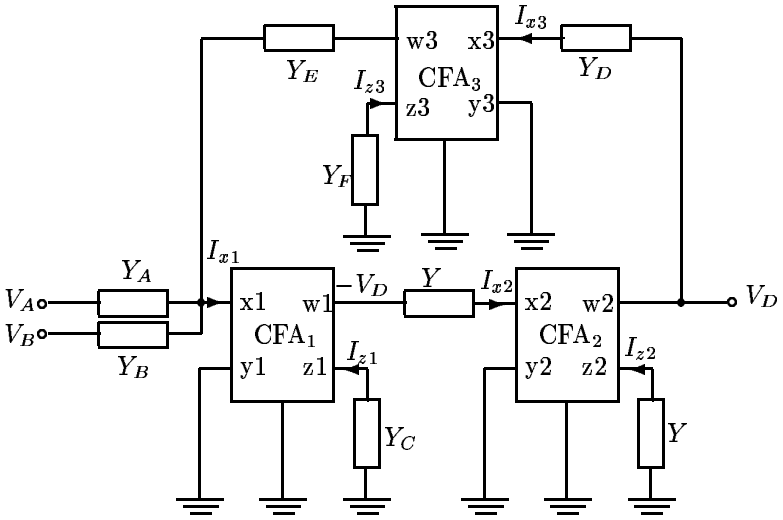


Fig. 4.2. Active RC simulation of V_k and I_k using CFA.

$$V_D = V_{w2} = V_{z2} = -\frac{I_{z2}}{Y} = -\frac{I_{x2}}{Y} = -V_{w1}, \tag{4.4}$$

and

$$V_{w3} = V_{z3} = -\frac{I_{z3}}{Y_F} = -\frac{I_{x3}}{Y_F} = -\frac{V_D Y_D}{Y_F}. \tag{4.5}$$

From (4.3), (4.4), and (4.5), we get

$$V_A \left(\frac{Y_A}{Y_C + \frac{Y_D Y_E}{Y_F}} \right) + V_B \left(\frac{Y_B}{Y_C + \frac{Y_D Y_E}{Y_F}} \right) = V_D. \tag{4.6}$$

Comparing (4.1) with (4.6), we identify

$$V_A \left(\frac{Y_A}{Y_C + \frac{Y_D Y_E}{Y_F}} \right) = I_{k+1} Z^k, \quad V_B \left(\frac{Y_B}{Y_C + \frac{Y_D Y_E}{Y_F}} \right) = -I_k Z^k, \tag{4.7}$$

and

$$V_D = V_k. \tag{4.8}$$

From (4.7)

$$V_A = \frac{I_{k+1}}{G}, \quad V_B = -\frac{I_k}{G}, \tag{4.9}$$

and

$$\frac{Y_A}{Y_C + \frac{Y_D Y_E}{Y_F}} = \frac{Y_B}{Y_C + \frac{Y_D Y_E}{Y_F}} = G Z^k \Rightarrow Y_A = Y_B \tag{4.10}$$

where G is the conductance introduced for balancing of dimensions. From (4.10)

$$Y^k = G \left(\frac{Y_C}{Y_B} + \frac{Y_D Y_E}{Y_B Y_F} \right). \tag{4.11}$$

Thus, the functional relation given in (4.1) can be simulated by the circuit of Fig. 4.2 if the voltages $\frac{I_{k+1}}{G}$ and $-\frac{I_k}{G}$ are available and Y^k is RC realizable. The currents I_k and I_{k+1} will be made available in the process of simulation of branch currents given by (4.2) (see (4.23)).

Since we are looking only for an all grounded-capacitor simulation, the grounded admittances Y_C and Y_F should only be RC DPAs. Choosing Y_C as Y_C^k and Y_F as Y_F^k RC DPAs and

$$Y_A = Y_B = G^k,\ Y_D = G_D^k,\ \text{and}\ Y_E = G_E^k, \tag{4.12}$$

we get from (4.11)

$$Y^k = \frac{N(s)}{Q(s)} = \left(\frac{G}{G^k}\right) Y_C^k + \left(\frac{GG_D^kG_E^k}{G^k}\right) \frac{1}{Y_F^k} \tag{4.13}$$

$$Y^k = \frac{N(s)}{Q(s)} = Y_{RC} + Y_{RL} \tag{4.14}$$

where

$$Y_{RC} = \left(\frac{G}{G^k}\right) Y_C^k = \text{an } RC \text{ admittance} \tag{4.15}$$

and

$$Y_{RL} = \left(\frac{GG_D^kG_E^k}{G^k}\right) \frac{1}{Y_F^k} = \text{an } RL \text{ admittance.} \tag{4.16}$$

Thus, we can simulate V_k with all the capacitors grounded provided Y^k can be decomposed as $Y_{RC}+Y_{RL}$ and

$$Y_C^k = \left(\frac{G^k}{G}\right) Y_{RC} \text{ and } Y_F^k = \left(\frac{GG_D^kG_E^k}{G^k}\right) \frac{1}{Y_{RL}} \tag{4.17}$$

are realized in the Foster II or Caur I form [3]. However, the former will yield the total capacitance a minimum [17]. Decomposition given by (4.14) imposes the following conditions [1].

(i) $N(s)$ must have positive leading coefficient and non-negative constant term.

(ii) $Q(s)$ must have all distinct non-positive real roots and positive leading coefficient and $Q(s)^o$ can be equal to either $N(s)^o$ or $N(s)^o - 1$.

If these conditions are satisfied, then partial fraction expansion gives

$$\frac{N(s)}{Q(s)} = \frac{A_\infty}{s} + k_\infty + A_0 s + \sum_i \frac{A_i}{s+p_i} - \sum_j \frac{A_j}{s+p_j} \tag{4.18}$$

$$\frac{N(s)}{Q(s)} = \left(k_\infty{}' + A_0 s - \sum_j \frac{A_j}{s+p_j}\right) + \left(\frac{A_\infty}{s} + k_\infty{}'' + \sum_i \frac{A_i}{s+p_i}\right) \tag{4.19}$$

$$\frac{N(s)}{Q(s)} = Y_{RC} + Y_{RL} \tag{4.20}$$

where $k_\infty = k_\infty{}' + k_\infty{}''$ and all A's and k'_∞s are real and non-negative such that

$$k_\infty{}' \geq \sum_j \frac{A_j}{p_j} \tag{4.21}$$

and $A_0 = 0$ if $Q(s)^o = N(s)^o$. Thus, active RC simulation of V_k with all capacitors grounded as shown in Fig. 4.2 is possible for any Y^k which satisfies the conditions (i) and (ii) above and (4.21).

If $Y_{RL} = 0$, it is easy to visualize from (4.16) that Y_D, Y_E, Y_F, and CFA_3 in Fig. 4.2 becomes redundant and hence can be omitted.

Simulation of I_k: Let I_k given by (4.2) also be simulated by the circuit of Fig. 4.2. Comparing (4.2) after dividing by G on both sides with (4.6), we identify

$$V_A\left(\frac{Y_A}{Y_C + \frac{Y_D Y_E}{Y_F}}\right) = \frac{V_k Y_k}{G}, \quad V_B\left(\frac{Y_B}{Y_C + \frac{Y_D Y_E}{Y_F}}\right) = -\frac{V_{k-1} Y_k}{G}, \tag{4.22}$$

and

$$V_D = \frac{I_k}{G}. \tag{4.23}$$

From these relations, we get

$$V_A = V_k, \quad V_B = -V_{k-1}, \tag{4.24}$$

$$Y_A = Y_B, \tag{4.25}$$

and

$$Z_k = \frac{1}{G}\left(\frac{Y_C}{Y_A} + \frac{Y_D Y_E}{Y_A Y_F}\right). \tag{4.26}$$

Thus, I_k can be simulated by Fig. 4.2 if Z_k is RC realizable. The voltages V_k and V_{k-1} are already generated in the process of simulation of node voltages given by (4.1) (see (4.8)).

For an all grounded-capacitor simulation, we choose Y_C as $Y_{Ck} = \frac{1}{Z_{Ck}}$ and Y_F as $Y_{Fk} = \frac{1}{Z_{Fk}}$ RC DPAs and

$$Y_A = Y_B = \frac{1}{R_k},\ Y_D = \frac{1}{R_{Dk}},\ \text{and}\ Y_E = \frac{1}{R_{Ek}}. \tag{4.27}$$

Then from (4.26), we get

$$Z_k = \frac{N(s)}{Q(s)} = \left(\frac{R_k}{G}\right)\frac{1}{Z_{Ck}} + \left(\frac{R_k}{GR_{Dk}R_{Ek}}\right)Z_{Fk} \tag{4.28}$$

$$Z_k = \frac{N(s)}{Q(s)} = Z_{RL} + Z_{RC} \tag{4.29}$$

where

$$Z_{RL} = \left(\frac{R_k}{G}\right)\frac{1}{Z_{Ck}} = \text{an } RL \text{ impedance} \tag{4.30}$$

and

$$Z_{RC} = \left(\frac{R_k}{GR_{Dk}R_{Ek}}\right)Z_{Fk} = \text{an } RC \text{ impedance.} \tag{4.31}$$

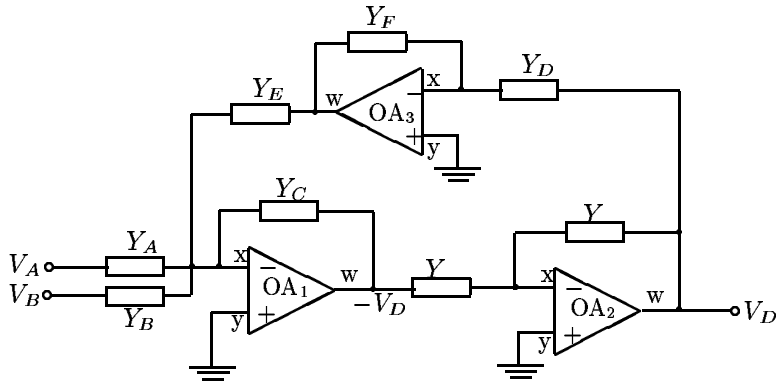
Thus, we can simulate I_k with all the capacitors grounded provided Z_k can be decomposed as $Z_{RL}+Z_{RC}$ and

$$Y_{Ck} = Z_{RL}\left(\frac{G}{R_k}\right) \text{ and } Y_{Fk} = \frac{1}{Z_{RC}}\left(\frac{R_k}{GR_{Dk}R_{Ek}}\right) \tag{4.32}$$

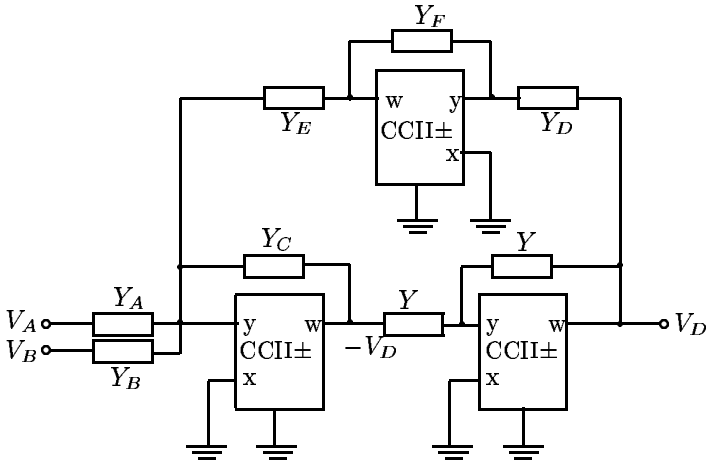
are realized in the Foster II or Caur I form [3]. The decomposition given by (4.29) imposes the conditions same as (i), (ii) and (4.21) given above for $Y_{RC} + Y_{RL}$ decomposition. Thus, active RC simulation of I_k with all capacitors grounded as shown in Fig. 4.2 is possible for any Z_k which satisfies the conditions (i) and (ii) and (4.21). If $Z_{RC} = 0$, Y_D, Y_E, Y_F and CFA_3 can be eliminated from Fig. 4.2.

Other simulation alternatives to Fig. 4.2 using OA ($V_x = V_y$, $I_x = I_y = 0$), CCII± ($V_x = V_y$, $I_y = 0$, $I_z = \pm I_x$), and FTFN ($V_x = V_y$, $I_x = I_y = 0$, $I_w = \pm I_z$) are shown in Fig. 4.3 but all of them have all the impedances floating. Obviously, none can yield an all grounded-capacitor simulation. Therefore, these circuits will not be considered further.

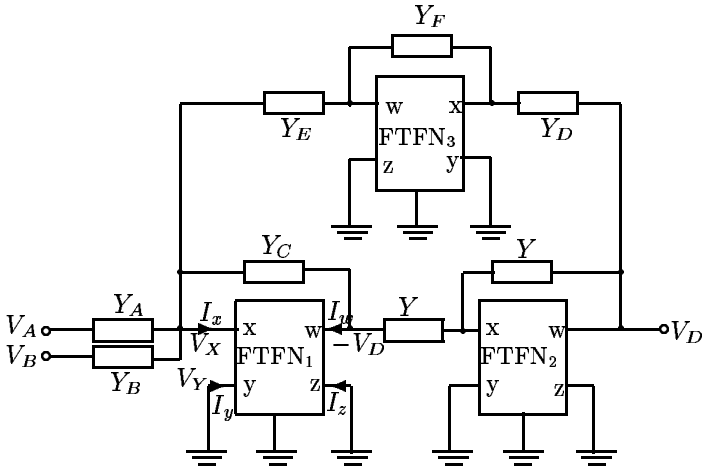
Based on the above theory, the complete all capacitor grounded simulation of the CM ladder of Fig. 4.1 is shown in Fig. 4.4.



(a)



(b)



(c)

Fig. 4.3. Active RC simulation of V_k and I_k using (a) OA, (b) CCII±, and (c) FTFN.

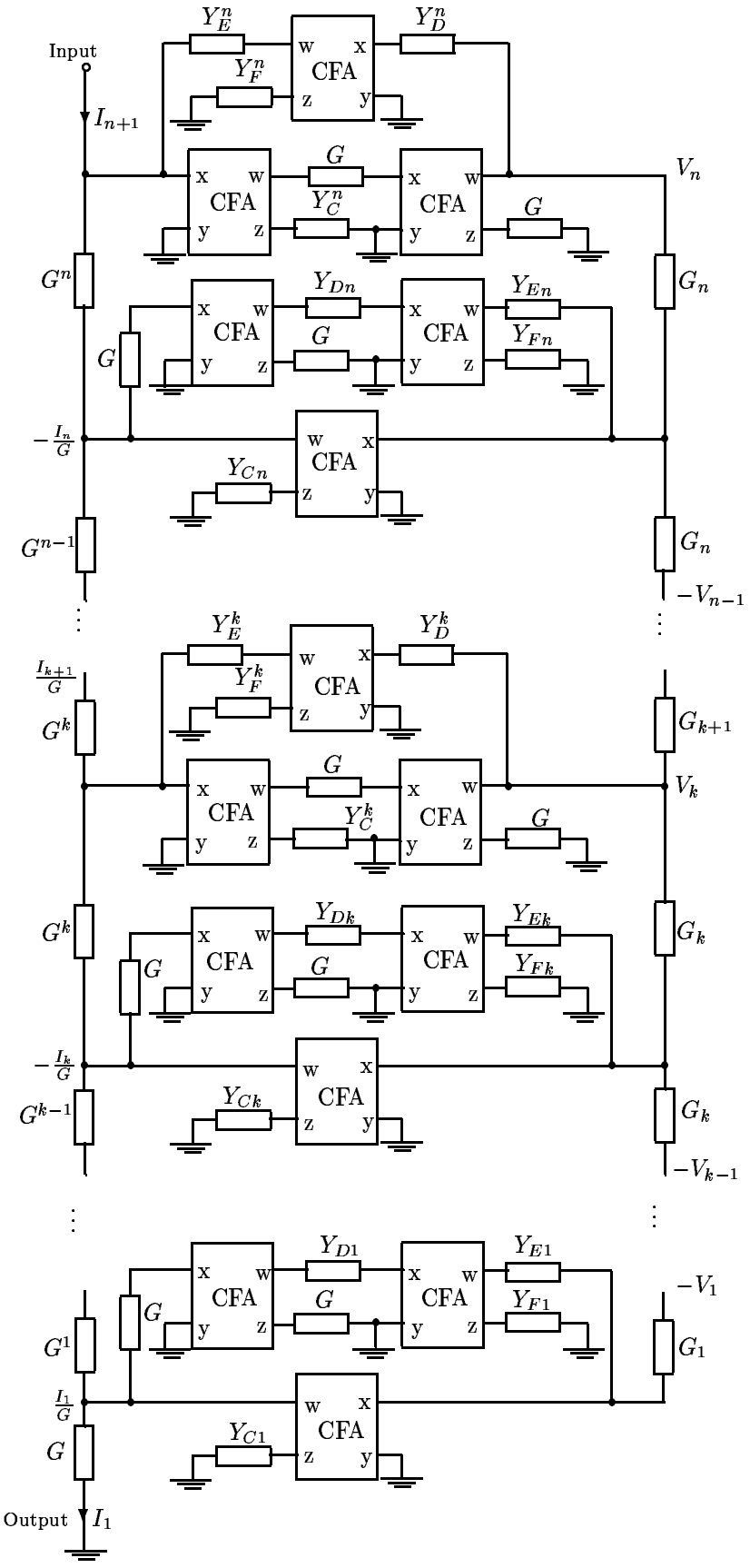


Fig. 4.4. CFA-*RC* simulation of the CM ladder.

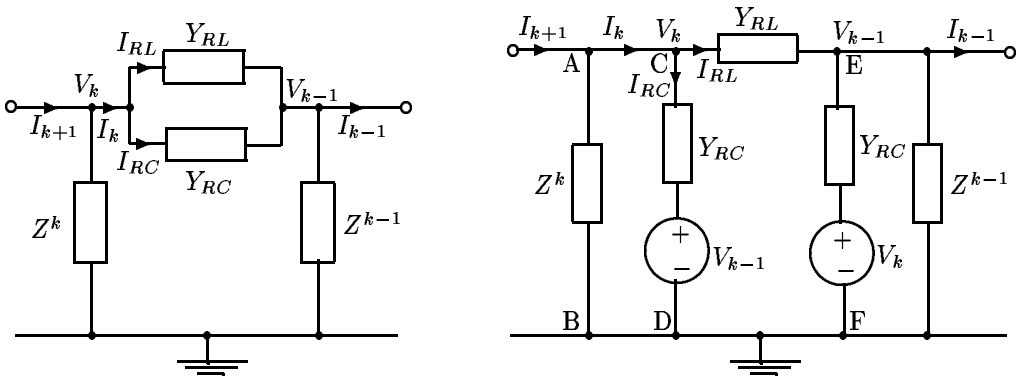


Fig. 4.5. kth section of ladder and its equivalent.

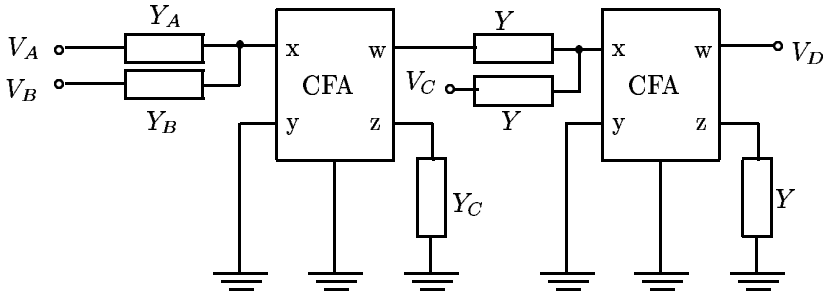


Fig. 4.6. Active RC simulation of V_k and I_{RL}.

Case A requires that shunt branch Y^k should be a parallel combination of Y_{RC} and Y_{RL}, and series branch Z_k should be a series combination of Z_{RC} and Z_{RL}. Now, we consider below the case B where shunt branch Z^k is a series combination of Z_{RL} and Z_{RC}, and series branch Y_k is a parallel combination of Y_{RC} and Y_{RL}.

4.2.2 Case B

In this case, the kth section of the ladder is replaced by its equivalent as shown in Fig. 4.5, and we have to simulate the voltage V_k and currents I_k and I_{RL}.

Simulation of V_k: Voltage V_k can be expressed as

$$\frac{I_k}{Y_{RC}} - \frac{I_{RL}}{Y_{RC}} + V_{k-1} = V_k. \tag{4.33}$$

Let the circuit shown in Fig. 4.6 be the active RC simulation of V_k given by (4.33). Analysis of the circuit leads to

$$V_A\left(\frac{Y_A}{Y_C}\right) + V_B\left(\frac{Y_B}{Y_C}\right) - V_C = V_D. \tag{4.34}$$

Handling (4.33) and (4.34) exactly as in Case A, we arrive at the following relations.

$$V_A = \frac{I_k}{G}, \quad V_B = -\frac{I_{RL}}{G}, \tag{4.35}$$

$$V_C = -V_{k-1}, \quad V_D = V_k. \tag{4.36}$$

$$Y_A = Y_B, \tag{4.37}$$

and

$$Y_{RC} = G\frac{Y_C}{Y_B}. \tag{4.38}$$

The voltages $-\frac{I_{RL}}{G}$ and $\frac{I_k}{G}$ will be generated through the simulation of current I_{RL} and I_k, respectively as shown below.

When $k = 1$, i.e. kth branch is a terminating branch, the above procedure leads to $V_C = V_0 = 0$ (refer (4.36)).

Simulation of I_{RL}: The current I_{RL} can be expressed as

$$V_k Y_{RL} - V_{k-1} Y_{RL} = I_{RL}. \tag{4.39}$$

Again, let us consider Fig. 4.6 for the simulation of I_{RL}. Comparing (4.34) with (4.39), we get

$$V_A = V_k, \quad V_B = -V_{k-1}, V_C = 0, \quad V_D = \frac{I_{RL}}{G}, \tag{4.40}$$

$$Y_A = Y_B, \tag{4.41}$$

and

$$Y_{RL} = G\frac{Y_A}{Y_C}. \tag{4.42}$$

Thus, I_{RL} can be simulated by Fig. 4.6. For an all-grounded capacitor simulation, choosing Y_C as Y_{Ck} RC DPA and $Y_A = Y_B = G_k$, we get from (4.42)

$$Y_{Ck} = (GG_k)\frac{1}{Y_{RL}} = \text{an } RC \text{ admittance.} \tag{4.43}$$

Thus, I_{RL} can be simulated with all the capacitors grounded.

Simulation of I_k: The current through Z^k can be written as

$$\frac{V_k}{Z^k} = (I_{k+1} - I_k). \tag{4.44}$$

Let the circuit shown in Fig. 4.2 also represent the active RC simulation of the functional relation given by (4.44). Comparing (4.44) with (4.6), we identify

$$V_A = V_k, \quad V_B = 0, \quad V_D = \left(\frac{I_{k+1}}{G} - \frac{I_k}{G}\right), \tag{4.45}$$

and

$$\frac{Y_A}{Y_C + \frac{Y_D Y_E}{Y_F}} = \frac{1}{GZ^k}. \tag{4.46}$$

For an all grounded-capacitor simulation, we choose Y_C as $Y_C^k = \frac{1}{Z_C^k}$ and Y_F as $Y_F^k = \frac{1}{Z_F^k}$ RC DPAs and

$$Y_A = \frac{1}{R^k}, \; Y_D = \frac{1}{R_D^k}, \text{ and } Y_E = \frac{1}{R_E^k}. \tag{4.47}$$

Then from (4.46), we get

$$Z^k = \frac{N(s)}{Q(s)} = \left(\frac{R^k}{G}\right)\frac{1}{Z_C^k} + \left(\frac{R^k}{GR_D^k R_E^k}\right) Z_F^k \tag{4.48}$$

$$Z^k = \frac{N(s)}{Q(s)} = Z_{RL} + Z_{RC} \quad \text{(given)} \tag{4.49}$$

where

$$Z_{RL} = \left(\frac{R^k}{G}\right)\frac{1}{Z_C^k} = \text{an } RL \text{ impedance} \tag{4.50}$$

and

$$Z_{RC} = \left(\frac{R^k}{GR_D^k R_E^k}\right) Z_F^k = \text{an } RC \text{ impedance.} \tag{4.51}$$

Thus, for grounded capacitor realization, Z^k should be Z_{RL}+Z_{RC} decomposible and

$$Y_C^k = Z_{RL}\left(\frac{G}{R^k}\right) \text{ and } Y_F^k = \frac{1}{Z_{RC}}\left(\frac{R^k}{GR_D^k R_E^k}\right) \tag{4.52}$$

are to be realized in the Foster II or Caur I form [3].

The voltage $\frac{I_k}{G}$ required in the simulation of V_k (see (4.44)) can be obtained as shown in Fig. 4.7.

As a special case of $Y^k = \alpha Y_{RC}$, the two branches AB and CD in Fig. 4.5 can be replaced by a single Thevenin equivalent and then the above procedure can be applied. This case is illustrated later in Example 4.2.

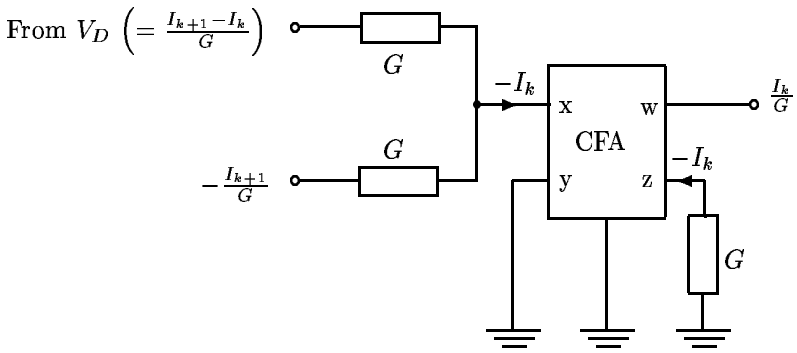


Fig. 4.7. An inverting adder.

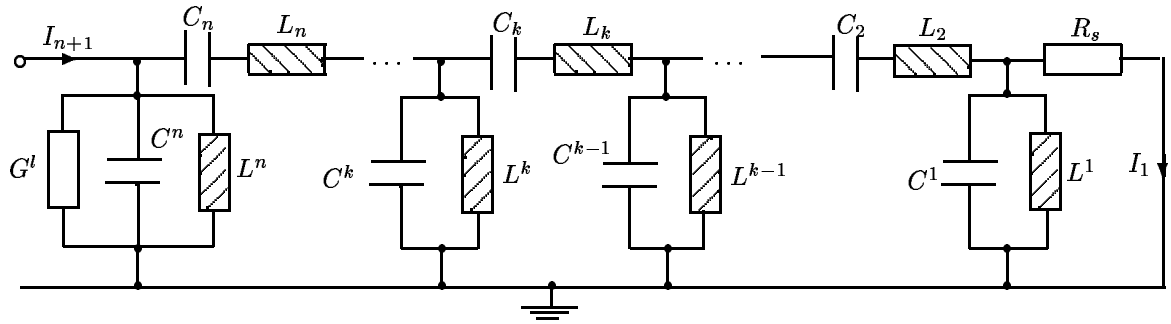


Fig. 4.8. CM all-pole Nth order band-pass filter.

4.3 Equal-valued capacitor design

Y_C and Y_F are the only admittances which may contain capacitors. As can be seen from (4.17) and (4.32), the magnitudes of Y_C^k, Y_F^k, Y_{Ck}, and Y_{Fk} can be adjusted by G^k, $G_D^k G_E^k$, R_k, and $R_{Dk}R_{Ek}$, respectively. Thus, if Y_k and Z^k have only one inductor and/or one capacitor for all k such as in low-pass, high-pass, band-pass and band-reject filters, it is possible to force all the capacitors of equal value.

The procedure discussed in Case A will now be illustrated with the simulation of a band-pass filter.

Example 4.1: Let us consider the simulation of the CM all-pole Nth ($N = 3n$) order band-pass filter shown in Fig. 4.8.

Here

$$\frac{1}{Y_k} = (R_{ks} + sL_k) + \frac{1}{sC_k}, \quad k = 1 \text{ to } n, \tag{4.53}$$

$$\frac{1}{Y_k} = Z_{RL} + Z_{RC} \tag{4.54}$$

where $R_{ks} = 0$ for $k \neq 1$, $R_{1s} = R_s$, $L_1 = 0$, $C_1 = \infty$, and

$$Y^k = \left(sC^k + G^{kl}\right) + \frac{1}{sL^k},\ k = 1 \text{ to } n, \tag{4.55}$$

$$Y^k = Y_{RC} + Y_{RL} \tag{4.56}$$

where $G^{kl} = 0$ for $k \neq n$ and $G^{nl} = G^l$. Thus, $Z_{RL} = R_{ks} + sL_k$, $Z_{RC} = \frac{1}{sC_k}$, $Y_{RC} = sC^k + G^{kl}$, and $Y_{RL} = \frac{1}{sL^k}$. From (4.17) and (4.32), we get

$$Y_C^k = sC_C^k + G_C^{kl}, \quad Y_F^k = sC_F^k, \text{ for } k = 1 \text{ to } n, \tag{4.57}$$

$$Z_{Ck} = \frac{1}{sC_{Ck}}, \quad Z_{Fk} = \frac{1}{sC_{Fk}}, \text{ for } k = 2 \text{ to } n, \quad \text{and} \quad Z_{C1} = \frac{R_1}{GR_s} \tag{4.58}$$

where

$$C_C^k = C^k\frac{G^k}{G}, \quad C_F^k = \frac{L^k G_D^k G_E^k G}{G^k}, \text{ for } k = 1 \text{ to } n, \tag{4.59}$$

$$G_C^{kl} = G_C^{nl} = \frac{G^n G^{nl}}{G} = \frac{G^n G^l}{G}, \tag{4.60}$$

$$C_{Ck} = \frac{L_k G}{R_k}, \quad \text{and} \quad C_{Fk} = \frac{C_k R_k}{GR_{Dk}R_{Ek}}, \text{ for } k = 2 \text{ to } n. \tag{4.61}$$

For equal-valued capacitor design, we choose $C_C^k = C_F^k = C_{Ck} = C_{Fk} = C$, and suitable values for G^1 and R_1. Then

$$G = \left(\frac{C^1}{C}\right) G^1, \tag{4.62}$$

$$Z_{C1} = \frac{R_1}{GR_s}, \tag{4.63}$$

$$G^k = \frac{C^1 G^1}{C^k} \text{ for } k = 2 \text{ to } n, \tag{4.64}$$

$$G_D^k G_E^k = \frac{C^k (G^k)^2}{(G)^2 L^k} \text{ for } k = 1 \text{ to } n, \tag{4.65}$$

$$R_k = \frac{L_k (G)^2}{C^k G^k} \text{ for } k = 2 \text{ to } n, \tag{4.66}$$

and

$$R_{Dk}R_{Ek} = \frac{C_k R_k}{C^k G^k} \text{ for } k = 2 \text{ to } n. \tag{4.67}$$

Following the above procedure, one can simulate the N^{th} $(N = 2n)$ order low-pass (high-pass) filter from the band-pass filter of Fig. 4.8 by making $C_k = L^k = \infty$ $(L_k = C^k = 0)$ in (4.53) and (4.55).

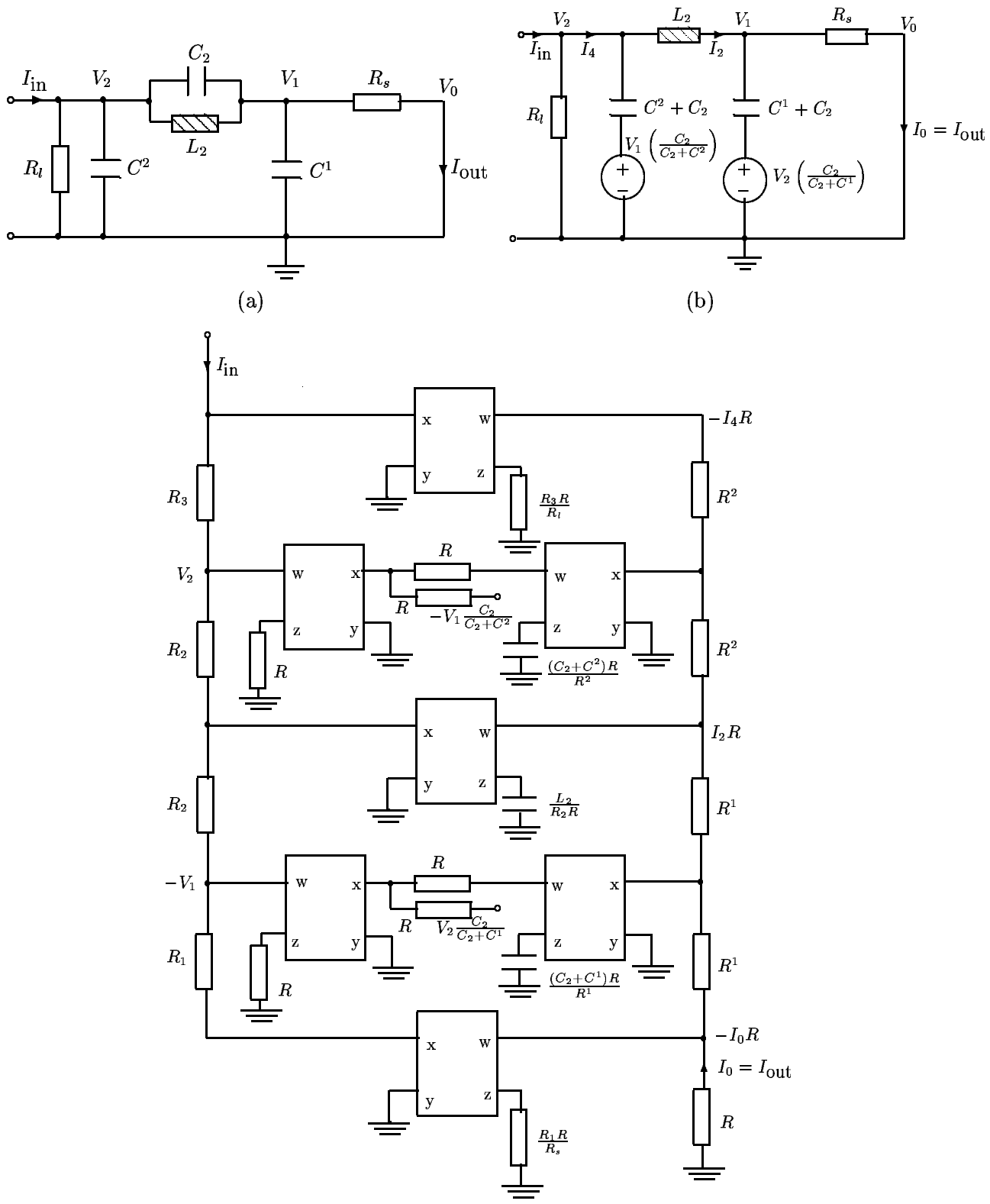


Fig. 4.9. (a) An *RLC* third order CM elliptic low-pass filter, (b) an equivalent form, and (c) CFA-*RC* simulation of third order elliptic low-pass filter.

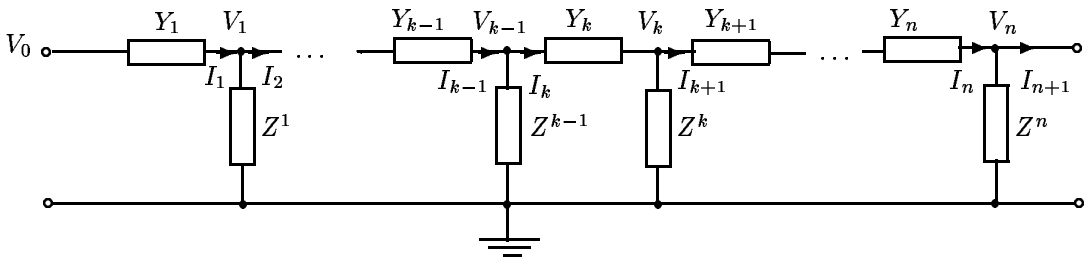


Fig. 4.10. Ladder network in voltage mode.

Example 4.2: Let us consider the third order CM elliptic low-pass filter shown in Fig. 4.9(a). Here

$$Y_1 = \frac{1}{R_s}, \quad Y_2 = sC_2 + \frac{1}{sL_2} = Y_{RC} + Y_{RL} \tag{4.68}$$

and

$$Y^1 = sC^1, \quad Y^2 = Y_{RC} + Y_{RL} = sC^2 + \frac{1}{R_l}. \tag{4.69}$$

The circuit shown in Fig. 4.9(a) is reduced to the equivalent form as shown in Fig. 4.9(b). The complete simulation of Fig. 4.9(b) is shown in Fig. 4.9(c). Choosing R^1, R_2, and R^2 of suitable values, all the capacitors can be forced to be of equal value. It may be noted that the branch like Y_2 in Fig. 4.9(a) cannot be simulated by Tangsrirat *et al.* method [89]. This is because of the limitation of their design procedure.

The CM ladder network shown in Fig. 4.1 can be converted into VM ladder network as shown in Fig. 4.10 [36], [102]. The two networks differ only in their end connections. Hence, their simulation will be the same, except for the end-connections shown in Fig. 4.11.

4.4 Simulation results

For verifying the circuit response developed by our technique, we have taken the all-pole sixth order band-pass ladder filter reported by Schaumann and Van Valkenburg [3] (pp. 596-597) as an example. They have realized the filter for a center frequency 31.8 kHz (ω= 0.2 Mrad/s) and midband gain with a nominal value of -6 dB with 1 dB passband ripple. This ladder filter can be derived by using 3 sections of ladder network shown in Fig. 4.10. The series branch Y_2 is made up of series combination

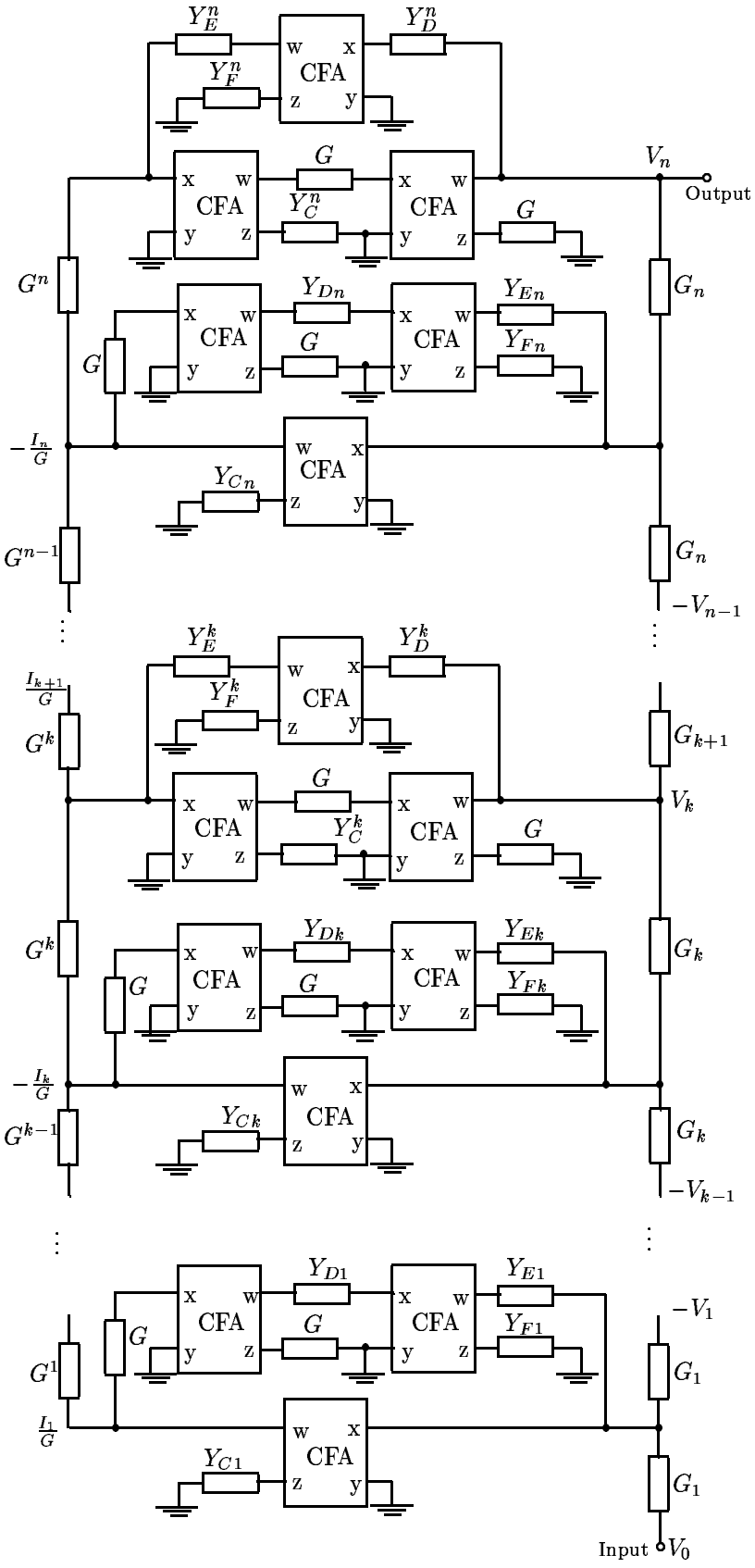


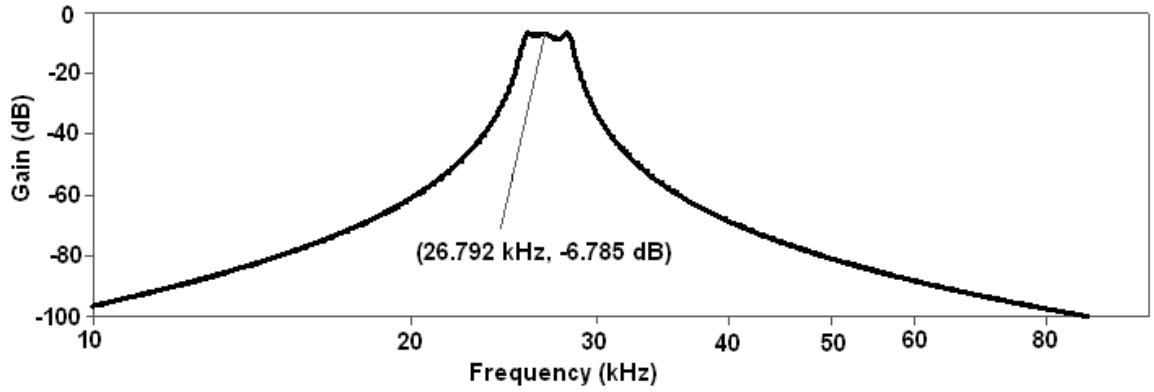
Fig. 4.11. CFA-*RC* simulation of the VM ladder.

of inductance and capacitance while Y_1 and Y_3 are made up of only resistances. The shunt branches Z^1 and Z^2 are made up of parallel combination of inductance and capacitance. The components used in this example were, $R_s = 800\ \Omega$, $L^1 = L^2 = 185\ \mu$H, $C^1 = C^2 = 135$ nF, $L_2 = 42.2$ mH, $C_2 = 0.59$ nF, and $R^l = 800\ \Omega$. From this passive ladder filter, the active RC ladder filter using op-amps was designed and simulated. They found the center frequency of 30.96 kHz and midband gain of -5.032 dB.

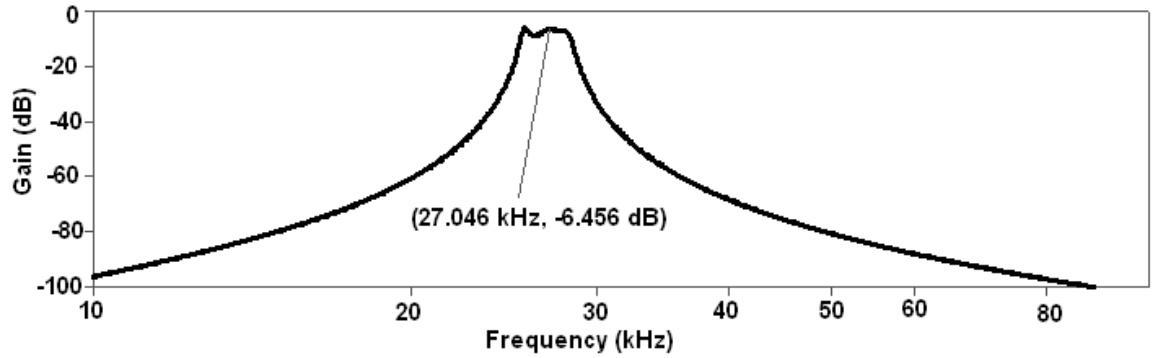
From the same passive ladder filter, we designed the active RC ladder filter with CM building blocks using our technique. Taking $C = 10$ nF and $R^1 = 2\ \text{k}\Omega$, we get $R = 148.148\ \Omega$. Taking $R_1 = 2\ \text{k}\Omega$, we get $R_{C1} = 370.37\ \Omega$, $R_2 = 28.48\ \text{k}\Omega$ and $R^2 = 1.99\ \text{k}\Omega$. Choosing $R_D^1 = R_{D2} = R_D^2 = 500\ \Omega$, we get $R_E^1 = 499.5\ \Omega$, $R_{E2} = 497.87\ \Omega$, $R_E^2 = 497\ \Omega$, and $R_C^{2l} = 10.8\ \text{k}\Omega$. The frequency responses of both the VM and CM filters are identical and hence only the frequency response of CM band-pass filter is shown in Fig. 4.12(a). Increasing the center frequency by decreasing C, it is observed that the filter performs well even at a frequency as high as 1 MHz. For the adjoint network obtained by interchanging x and w terminals of all the CFAs [37], it is observed that the frequency response becomes the mirror image about the vertical line at the centre frequency as shown in Fig. 4.12(b).

A CM third order band-reject filter [3] (pp. 600-601) having equal ripple passband with $\alpha_{\max} = 1$ dB in $f \leq 80$ kHz and $f \geq 180$ kHz and $\alpha_{\min} \geq 20$ dB in 100 kHz $\leq f \leq 150$ kHz is simulated with $Z_1 = R_s = 1\ \Omega$, Z^1 and Z^2 made up of series combinations of inductor and capacitor of values $L^1 = L^2 = 0.7865\ \mu$H and $C^1 = C^2 = 2.237\ \mu$F, Z_2 made up of a parallel combination of inductor and capacitor of values $L_2 = 1.099\ \mu$H and $C_2 = 1.601\ \mu$F terminated with $R^l = 1\ \Omega$. Taking $C = 1$ nF, $R_1 = 1\ \text{k}\Omega$ and $R_3 = 1\ \text{k}\Omega$, we get $R = 0.7865\ \Omega$, $R_{C1} = 786.5\ \Omega$, $R^1 = 1.259\ \text{k}\Omega$, $R_2 = 1.397\ \text{k}\Omega$, $R^2 = 1.259\ \text{k}\Omega$, $R_D^1 = R_E^1 = R_D^2 = R_E^2 = 1.326\ \text{k}\Omega$, and $R_C^{2l} = 786.5\ \Omega$. The frequency responses obtained for the prototype filter and its RC simulation are shown in Fig. 4.13 and they appear to be almost identical.

A CM third order high-pass notch ladder filter derived from the above band-reject filter by replacing the capacitors C^1 and C^2 by short circuits was also simulated. Because of the complexity of the circuit shown in Fig. 4.4, bread-boarding of these circuits was not feasible and hence, only the simulation results are given in Figs. 4.12



(a)



(b)

Fig. 4.12. (a) Frequency response of the CM sixth order all-pole band-pass filter and (b) frequency response of the adjoint network of CM sixth order all-pole band-pass filter.

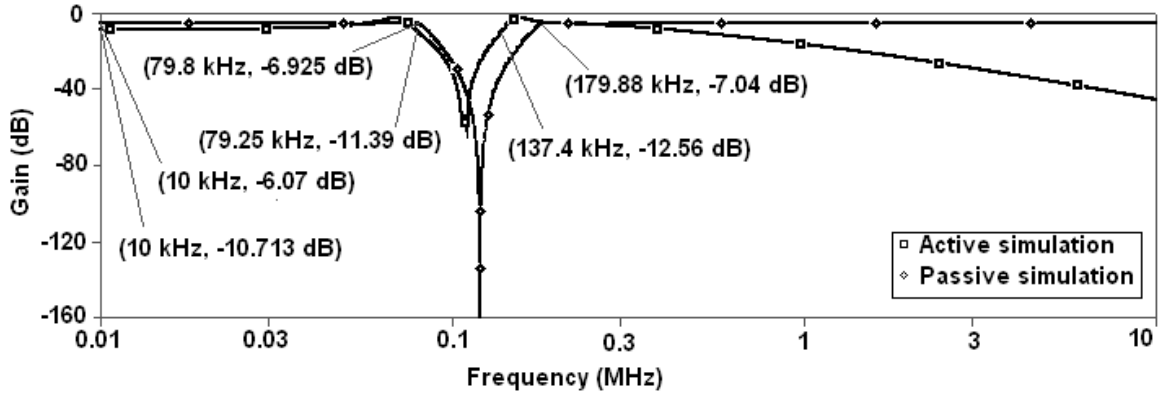


Fig. 4.13. Frequency response of the CM third order band-reject filter.

and 4.13. The simulation results were found to be in agreement with the theory.

4.5 Concluding remarks

A systematic method has been developed for deriving CFA based grounded-capacitor simulations from CM and VM *RLC* ladders. It is applicable when both the series and shunt branch admittances can be expressed as $Y + \frac{1}{Z}$ such that $Y = Y_{RC} + Y_{RL}$ and $Z = Z_{RL} + Z_{RC}$ types. This allows the simulations of all the generic filters except the all-pass one with all the capacitors of equal value. Such realizations are suitable for fabrication in IC technology. The CFA based filters work satisfactorily at high frequencies. Simulation results were in agreement with the theoretical calculations.

Chapter 5

SYNTHESIS OF AMPLITUDE EQUALIZERS

5.1 Introduction

The amplitude equalizers (AEs) are used in many systems to compensate for the deviations produced in the loss-frequency characteristics. In this chapter, some of the reported AEs are derived systematically in Section 5.2, and in the process some new AEs are obtained. A systematic design for AE is given in Section 5.3 where both the whole range and the value of variable resistor at which the flat response is required are accomodated. The AEs employing CM building blocks are derived in Section 5.4. They can operate satisfactorily at much higher frequencies compared to the OA based ones. Simulation results are presented and discussed in Section 5.5.

5.2 Active RC amplitude equalizers

Bode [90] suggested the transfer function

$$T(s) = \frac{1 + xH(s)}{x + H(s)} \tag{5.1}$$

suitable for AEs with a single variable resistor. Here, x is a function of variable resistor R_v and has no dimension. The transfer function $T(s)$ for three specific values

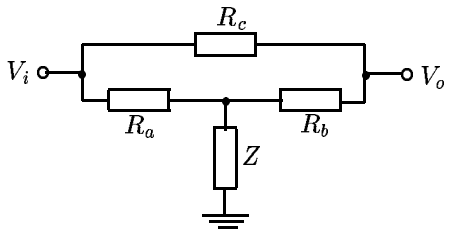


Fig. 5.1. The passive AE circuit.

of R_v is given as

$$T(s) = \begin{cases} 1/H(s), & R_v = R_{v1} \\ H(s), & R_v = R_{v2} \\ 1, & R_v = R_f. \end{cases} \tag{5.2}$$

Thus it has a symmetry around 0 dB line and has flat response for $R_v = R_f$. The whole range of the AE is given by $[R_{v1}, R_{v2}]$. Let the difference in the maximum and minimum value of this variable resistor is denoted by R_r. Several earlier reported active *RC* AEs [91]-[97] are derived systematically in the following subsections.

5.2.1 Amplitude equalizers using NIC

We realize AEs using NIC, by starting with (i) a passive equalizer and (ii) an active equalizer.

(i) *Circuit I*: Let us consider the passive equalizer circuit shown in Fig. 5.1. The analysis of the circuit leads to

$$T(s) = \frac{V_o}{V_i} = \left[\frac{Z(R_a + R_b) + R_a R_b}{(Z + R_a)R_a}\right] \frac{\left[1 + \left(\frac{R_c}{R_a}\right)\frac{ZR_a}{Z(R_a + R_b) + R_a R_b}\right]}{\left[\frac{R_c}{R_a} + \frac{Z(R_a + R_b) + R_a R_b}{(Z + R_a)R_a}\right]}. \tag{5.3}$$

The derivation of (5.3) can be seen in Appendix. In (5.3), let

$$x = \frac{R_c}{R_a} \tag{5.4}$$

and

$$\frac{Z(R_a + R_b) + R_a R_b}{(Z + R_a)R_a} = 1 \tag{5.5}$$

which results in

$$Z = R_a\left(\frac{R_a}{R_b} - 1\right). \tag{5.6}$$

Equation (5.6) cannot be satisfied as Z cannot be a resistive element. To overcome this difficulty, we take $R_c = R_v - R_0$ where R_0 is a reference resistance. Now (5.3) becomes

$$T(s) = \left[\frac{Z(R_a + R_b - R_0) + R_a R_b}{(Z + R_a)R_a}\right] \frac{\left[1 + \left(\frac{R_v}{R_a}\right) \frac{ZR_a}{Z(R_a + R_b - R_0) + R_a R_b}\right]}{\left[\frac{R_v}{R_a} + \frac{Z(R_a + R_b - R_0) + R_a R_b - R_a R_0}{(Z + R_a)R_a}\right]}. \tag{5.7}$$

In (5.7), let

$$x = \frac{R_v}{R_a} \tag{5.8}$$

and

$$\frac{Z(R_a + R_b - R_0) + R_a R_b}{(Z + R_a)R_a} = 1 \tag{5.9}$$

which results in

$$R_a = R_b = R_0. \tag{5.10}$$

Comparing (5.7) with (5.1), we get

$$H(s) = \frac{ZR_a}{Z(R_a + R_b - R_0) + R_a R_b} \tag{5.11}$$

and

$$\frac{ZR_a}{Z(R_a + R_b - R_0) + R_a R_b} = \frac{Z(R_a + R_b - R_0) + R_a R_b - R_a R_0}{(Z + R_a)R_a}. \tag{5.12}$$

With the condition in (5.10), (5.8) and (5.11) get simplified, respectively, to

$$x = \frac{R_v}{R_0} \tag{5.13}$$

and

$$H(s) = \frac{Z}{Z + R_0}. \tag{5.14}$$

With these relations, the circuit reduces to that shown in Fig. 5.2 which is the same as proposed by Saraga and Zyoute [91]. The fixed negative resistance $-R_0$ is achieved using NIC. The gain-loss response of this AE has a geometric symmetry around 0 dB line and has a flat response for $R_v = R_0$. The whole range of this AE is $[0, \infty]$. The circuit requires an additional buffer at the output to avoid loading.

(ii) *Circuit II*: Let us consider the active equalizer circuit shown in Fig. 5.3(a). The analysis of the circuit (derivation given in Appendix) leads to

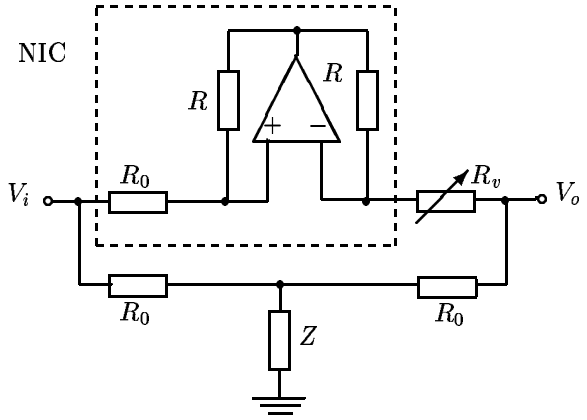


Fig. 5.2. Saraga and Zyoute's AE.

$$T(s) = \frac{V_o}{V_i} = \frac{\frac{R_b}{R_a}\left[\left(\frac{R_a}{R_b}\right)\frac{R_c}{Z_c} - 1\right]}{\frac{R_c}{Z_c} + 1} \tag{5.15}$$

$$T(s) = \frac{V_o}{V_i} = \frac{1 + \left(\frac{R_a R_c + R_b R_0}{R_a R_c - R_b R_0}\right)\frac{R_0 - Z_c}{R_0 + Z_c}}{\frac{R_c + R_0}{R_c - R_0} + \frac{R_0 - Z_c}{R_0 + Z_c}} \tag{5.16}$$

$$T(s) = \frac{V_o}{V_i} = \frac{1 + x'H'(s)}{x' + H'(s)}. \tag{5.17}$$

In (5.17), let

$$H'(s) = \frac{R_0 - Z_c}{R_0 + Z_c} = \frac{H(s) - 1}{H(s) + 1} \tag{5.18}$$

where

$$H(s) = \frac{R_0}{Z_c} \tag{5.19}$$

then

$$x' = \frac{R_c + R_0}{R_c - R_0} \tag{5.20}$$

and

$$\frac{R_a R_c + R_b R_0}{R_a R_c - R_b R_0} = \frac{R_c + R_0}{R_c - R_0} \tag{5.21}$$

which results in

$$R_a = R_b. \tag{5.22}$$

Thus, for x' to vary from 0 to ∞ so as to have $T(s)$ variation from $1/H'(s)$ to $H'(s)$, R_c should vary from $-R_0$ to $+R_0$. As a practical variable resistor cannot have negative

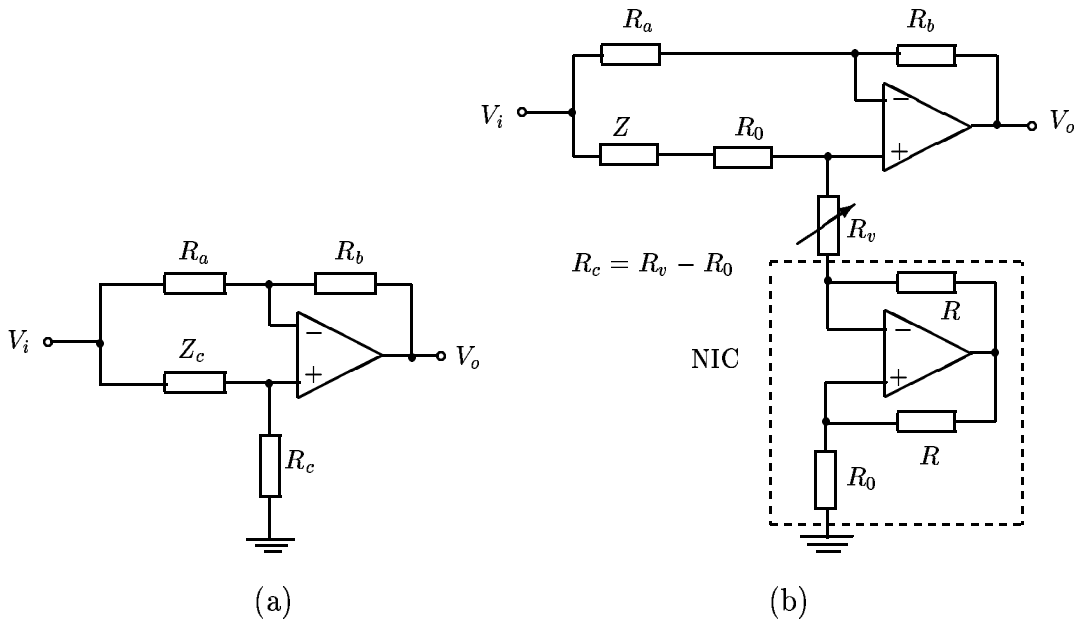


Fig. 5.3. (a) Active AE circuit and (b) Brglez's AE using NIC.

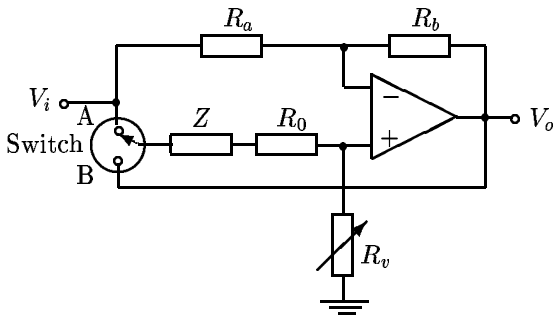


Fig. 5.4. Brglez's AE using switch.

value, we take $R_c = R_v - R_0$. Now with condition in (5.22), (5.17) becomes

$$T(s) = \frac{1 + \left(\frac{R_v}{R_v - 2R_0}\right) H'(s)}{\frac{R_v}{R_v - 2R_0} + H'(s)}. \tag{5.23}$$

The $T(s)$ now varies from $1/H'(s)$ to $H'(s)$ when R_v varies from 0 to $2R_0$. Thus the whole range is $[0,\ 2R_0]$. A flat response is obtained when $R_v = R_0$. Thus the circuit shown in Fig. 5.3(a) leads to the circuit shown in Fig. 5.3(b) which is the same as given by Brglez [92]. It can be noted that the Brglez's circuit uses Z_c as a series combination of the fixed resistance (R_0) and impedance (Z). This splitting of Z_c may not be required. To eliminate the NIC in the circuit of Fig. 5.3(b), Brglez [93] used a switch as shown in Fig. 5.4. The circuit provides the positive R_v range when the switch is connected to A terminal and the negative R_v range when connected to B

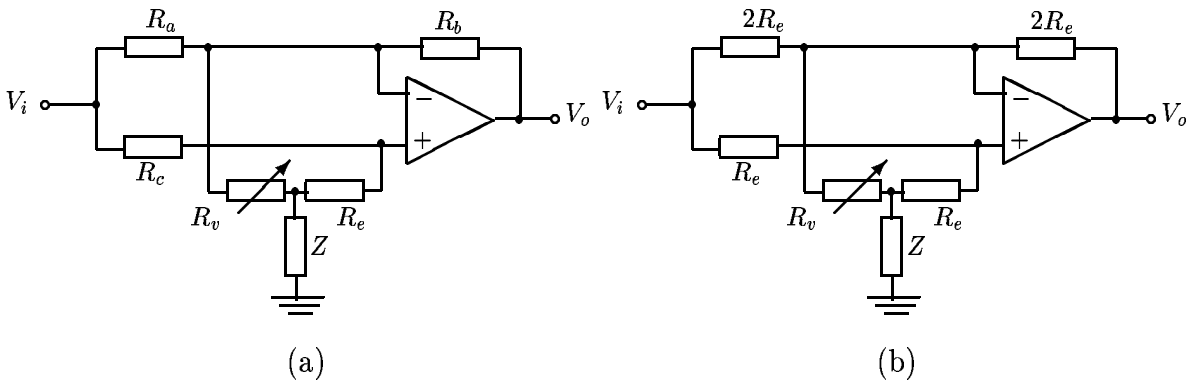


Fig. 5.5. (a) Zyoute's basic AE and (b) Zyoute's AE.

terminal. One can see that the toggling of the switch provides basically two inverse active networks [117].

5.2.2 Single OA amplitude equalizers

We realize the following two AE circuits using single OA.

(i) *Circuit I*: Let us consider the single OA circuit shown in Fig. 5.5(a) which gives a buffered output. The analysis gives

$$T(s) = \left[\frac{Z + R_b}{Z + R_c + R_e}\right] \frac{\left[1 + \left(\frac{R_v}{R_e}\right) \frac{ZR_a + R_eR_a - R_bR_c}{R_a(Z + R_b)}\right]}{\left[\frac{R_v}{R_e} + \frac{Z}{Z + R_c + R_e}\right]}. \tag{5.24}$$

In (5.24), Let

$$x = \frac{R_v}{R_e} \tag{5.25}$$

and

$$\frac{Z + R_b}{Z + R_c + R_e} = 1 \tag{5.26}$$

which results in

$$R_b = R_c + R_e. \tag{5.27}$$

By comparing (5.24) with (5.1), we get

$$H(s) = \frac{Z}{Z + R_c + R_e} \tag{5.28}$$

and

$$\frac{ZR_a + R_eR_a - R_bR_c}{R_a(Z + R_b)} = \frac{Z}{Z + R_c + R_e}. \tag{5.29}$$

Substituting the value of R_b from (5.27) in (5.29), we get

$$R_b = \frac{R_a R_e}{R_c}. \tag{5.30}$$

From (5.27) and (5.30), we get

$$R_c = \frac{-R_e \pm \sqrt{R_e^2 + 4R_a R_e}}{2}. \tag{5.31}$$

Equations (5.30) and (5.31) are the design relations for AE of Fig. 5.5(a) after choosing suitable value for R_a and/or R_e. Thus, there are many possible AEs. For example, two of them are given below.

(a) Let $R_a = 2R_e$. Then $R_c = R_e$, $R_b = 2R_e$, and

$$H(s) = \frac{Z}{Z + 2R_e}. \tag{5.32}$$

With these relations, the circuit of AE is shown in Fig. 5.5(b). This circuit is the same as given by Zyoute [94] when $R_e = R_0$.

(b) Let $R_a = \frac{15}{4}R_e$. Then $R_c = \frac{3}{2}R_e$, $R_b = \frac{5}{2}R_e$, and

$$H(s) = \frac{Z}{Z + \frac{5}{2}R_e}. \tag{5.33}$$

(ii) *Circuit II*: Talkhan *et al.* [95] used the same circuit topology as given in Fig. 5.5(a). Equation (5.24) can be rearranged as

$$T(s) = K\frac{1 + x_1 H(s)}{x_2 + H(s)} \tag{5.34}$$

where

$$K = \frac{1 + \dfrac{R_v R_a R_b R_e - R_b^2 R_c R_v - R_v R_a R_e Z}{R_a R_b R_e (Z + R_b)}}{1 - \dfrac{R_v}{R_b}}, \tag{5.35}$$

$$x_1 = \frac{\dfrac{R_v}{R_b}\left(1 + \dfrac{R_b}{R_e}\right)}{1 + \dfrac{R_v R_a R_b R_e - R_b^2 R_c R_v - R_v R_a R_e Z}{R_a R_b R_e (Z + R_b)}}, \tag{5.36}$$

$$x_2 = \frac{\dfrac{R_v}{R_b}\left[1 + \left(\dfrac{R_b}{R_e}\right)\dfrac{Z + R_c}{Z + R_b}\right]}{1 - \dfrac{R_v}{R_b}}, \tag{5.37}$$

and

$$H(s) = \frac{Z}{Z + R_b}. \tag{5.38}$$

In (5.34), let

$$K = \frac{1 + \dfrac{R_v R_a R_b R_e - R_b^2 R_c R_v - R_v R_a R_e Z}{R_a R_b R_e (Z + R_b)}}{1 - \dfrac{R_v}{R_b}} = 1 \tag{5.39}$$

which results in

$$R_b = \frac{2R_a R_e}{R_c}. \tag{5.40}$$

By comparing (5.34) with (5.1), we get

$$x_1 = x_2 \tag{5.41}$$

$$\frac{\dfrac{R_v}{R_b}\left(1 + \dfrac{R_b}{R_e}\right)}{1 + \dfrac{R_v - \dfrac{R_b R_c R_v}{R_a R_e} - \dfrac{R_v Z}{R_b}}{Z + R_b}} = \frac{\dfrac{R_v}{R_b}\left[1 + \left(\dfrac{R_b}{R_e}\right)\dfrac{Z + R_c}{Z + R_b}\right]}{1 - \dfrac{R_v}{R_b}}. \tag{5.42}$$

Substituting the value of R_b from (5.40) in (5.42), we get

$$R_b = R_c. \tag{5.43}$$

From (5.40) and (5.43), we get

$$R_c = \sqrt{2R_a R_e}. \tag{5.44}$$

Equations (5.43) and (5.44) are the design relations for AE of Fig. 5.5(a) after choosing suitable values for either R_a or R_e as follows.

(a) Let $R_a = \frac{1}{2}R_e$. Then $R_b = R_c = R_e$. With these relations, the circuit of AE is shown in Fig. 5.6. This is the same circuit as depicted by Talkhan *et al.* [95] when $R_e = R_0$.

(b) If we choose $R_a = 2R_e$, we get $R_b = R_c = 2R_e$.

The $T(s)$ varies from $1/H(s)$ to $H(s)$ when R_v varies from 0 to R_b. Thus, the whole range becomes $[0, R_b]$. A flat response is obtained when

$$x_1 = x_2 = 1 \tag{5.45}$$

$$\Rightarrow R_v = \frac{R_b R_e}{R_b + 2R_e}. \tag{5.46}$$

Depending upon R_e, flat response can be obtained for different values of R_v.

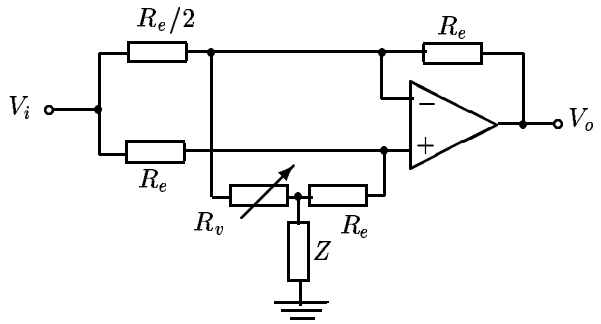


Fig. 5.6. Talkhan's AE for $R_e = R_0$.

5.2.3 Amplitude equalizers with specified $H(s)$

The block diagram realization of $T(s)$ given by

$$T(s) = \frac{x + H(s)}{1 + xH(s)} \tag{5.47}$$

where $x = R_v/R_0$ is given in Fig. 5.7(a) and the corresponding active RC realization is shown in Fig. 5.7(b) where

$$H(s) = \frac{R_0 + Z}{R_0 - Z}. \tag{5.48}$$

This is the corrected circuit proposed by Nowrouzian and Fuller [96] which requires, after including one inverter which is missing in their circuit, 5 OAs and 14 resistors. In the circuit of Fig. 5.7(b), one cannot isolate the block corresponding to $H(s)$. For this purpose, one can represent the circuit of Fig. 5.7(b) alternately as in Fig. 5.8(a). The realization of $H(s) = (R_0 + Z)/(R_0 - Z)$ is shown in Fig. 5.8(b). In the circuit of Fig. 5.8(a), if we realize $H(s)$ by $(R_0 - Z)/(R_0 + Z)$, then $T(s)$ becomes

$$T(s) = \frac{1 + \left(\frac{R_v}{R_0}\right)\frac{R_0 + Z}{R_0 - Z}}{\frac{R_v}{R_0} + \frac{R_0 + Z}{R_0 - Z}}. \tag{5.49}$$

Comparing (5.49) with (5.1), we get

$$x = \frac{R_v}{R_0} \tag{5.50}$$

and

$$H(s) = \frac{R_0 + Z}{R_0 - Z}. \tag{5.51}$$

The realization of $H(s) = (R_0 - Z)/(R_0 + Z)$ is shown in Fig. 5.8(c).

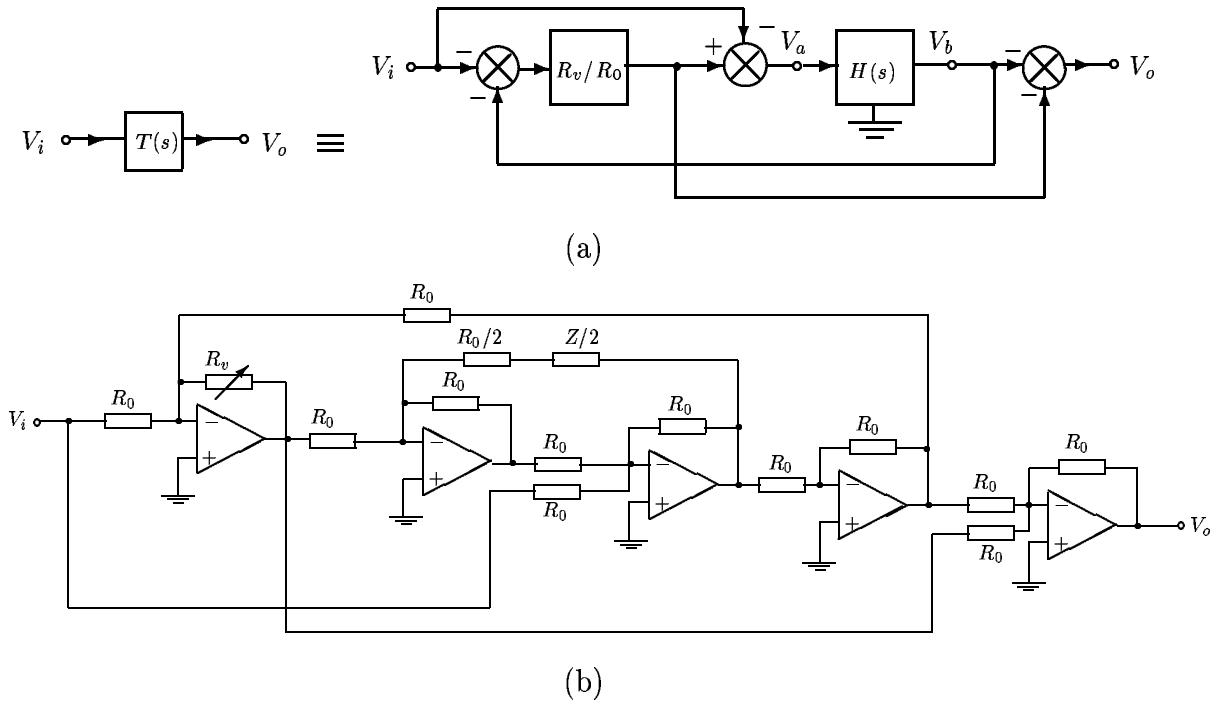


Fig. 5.7. Nowrouzian and Fuller's AE: (a) Realization of $T(s)$ and (b) active RC realization of the AE.

Alternate block diagrams of $T(s)$ given by (5.47) are shown in Fig. 5.9. The active RC realization of the AEs corresponding to Figs. 5.9(a)-(c) are same as in Fig. 5.7(b). The active RC realizations of an AE corresponding to Fig. 5.9(d) are given in Figs. 5.10(a)-(c) and the realization of $H(s) = (R_0 + Z)/(R_0 - Z)$ using OAs having their non inverting terminal grounded is shown in Fig. 5.10(d). The active RC realization of the AEs corresponding to Figs. 5.9(e)-(g) follows the same structures as shown in Fig. 5.10(a)-(c).

5.2.4 3-OA amplitude equalizers

A 3-OA AE proposed by Nowrouzian *et al.* [97] is shown in Fig. 5.11(a). The analysis of the circuit leads to

$$T(s) = -\frac{\dfrac{R_v}{R_0} + \dfrac{2Z}{2Z + R_0}}{1 + \left(\dfrac{R_v}{R_0}\right)\dfrac{2Z}{2Z + R_0}} = -\frac{x + H(s)}{1 + xH(s)} \tag{5.52}$$

where

$$x = \frac{R_v}{R_0} \tag{5.53}$$

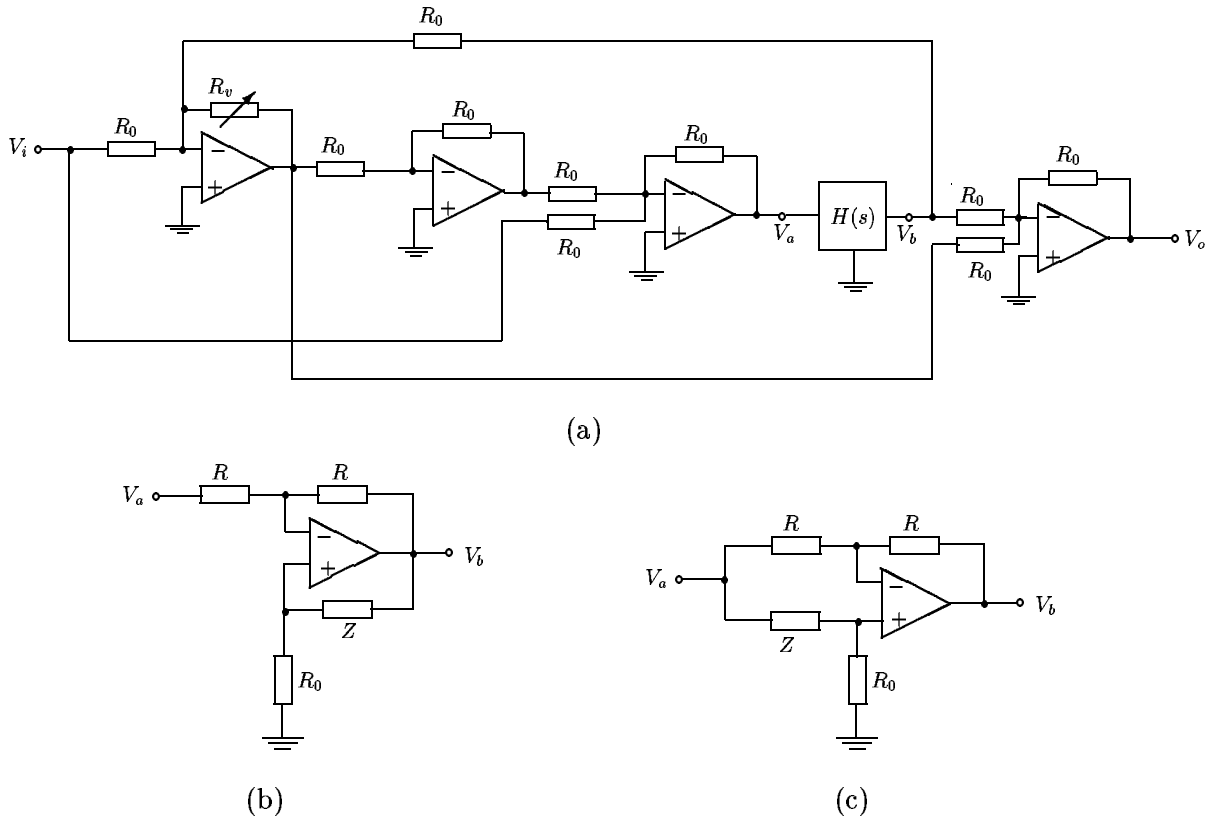


Fig. 5.8. (a) Alternate representation of the circuit in Fig. 5.7(b), (b) realization of $H(s) = (R_0 + Z)/(R_0 - Z)$, and (c) realization of $H(s) = (R_0 - Z)/(R_0 + Z)$.

and

$$H(s) = \frac{2Z}{2Z + R_0}. \tag{5.54}$$

The $T(s)$ is realized as a voltage transfer function from port 1 to port 2 of a three-port network N when its port 3 is terminated in the impedance Z as shown in Fig. 5.11(b).

Table 5.1 gives a comparative study of the various AEs. As can be seen, the Nowrouzian and Fuller's AE [96] requires a large number of active (5 OAs) and passive elements (14 resistors) whereas the Talkhan's AE [95] requires a single active element and a small number of passive elements. Further, the whole range produced by Talkhan's AE is less compared to that produced by all other AEs. Saraga and Zyoute's AE [91] requires an additional buffer to avoid the loading. The proposed AE given in Fig. 5.10(c) realizes the same $T(s)$, realized by Nowrouzian and Fuller, with only 4 OAs and 12 resistors. If both the whole range and the value of variable resistor at which the flat response is required are specified, it is not possible to realize the AEs using all the above methods. This drawback has been overcome by the method

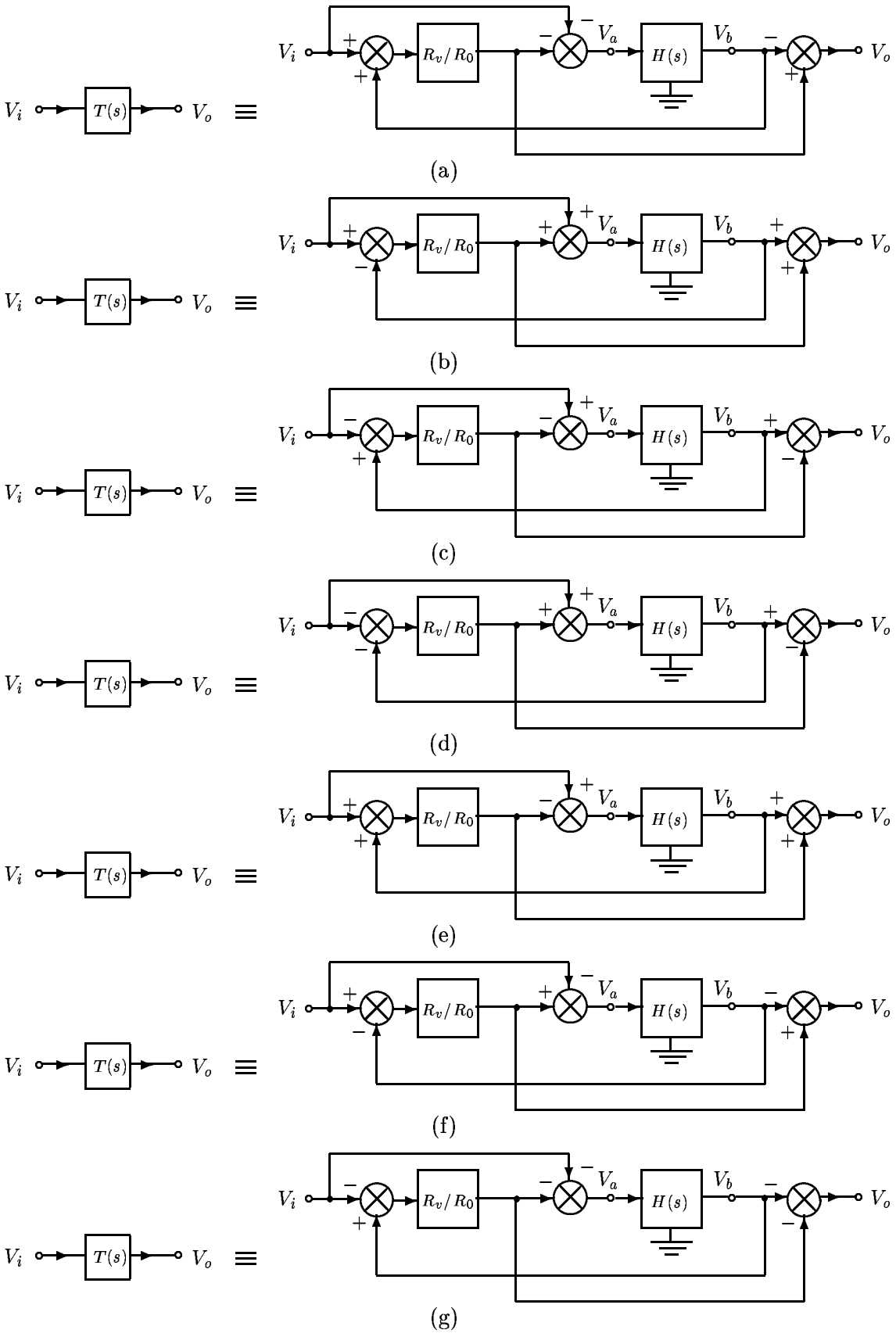


Fig. 5.9. Alternate realizations of $T(s)$ given by (5.47).

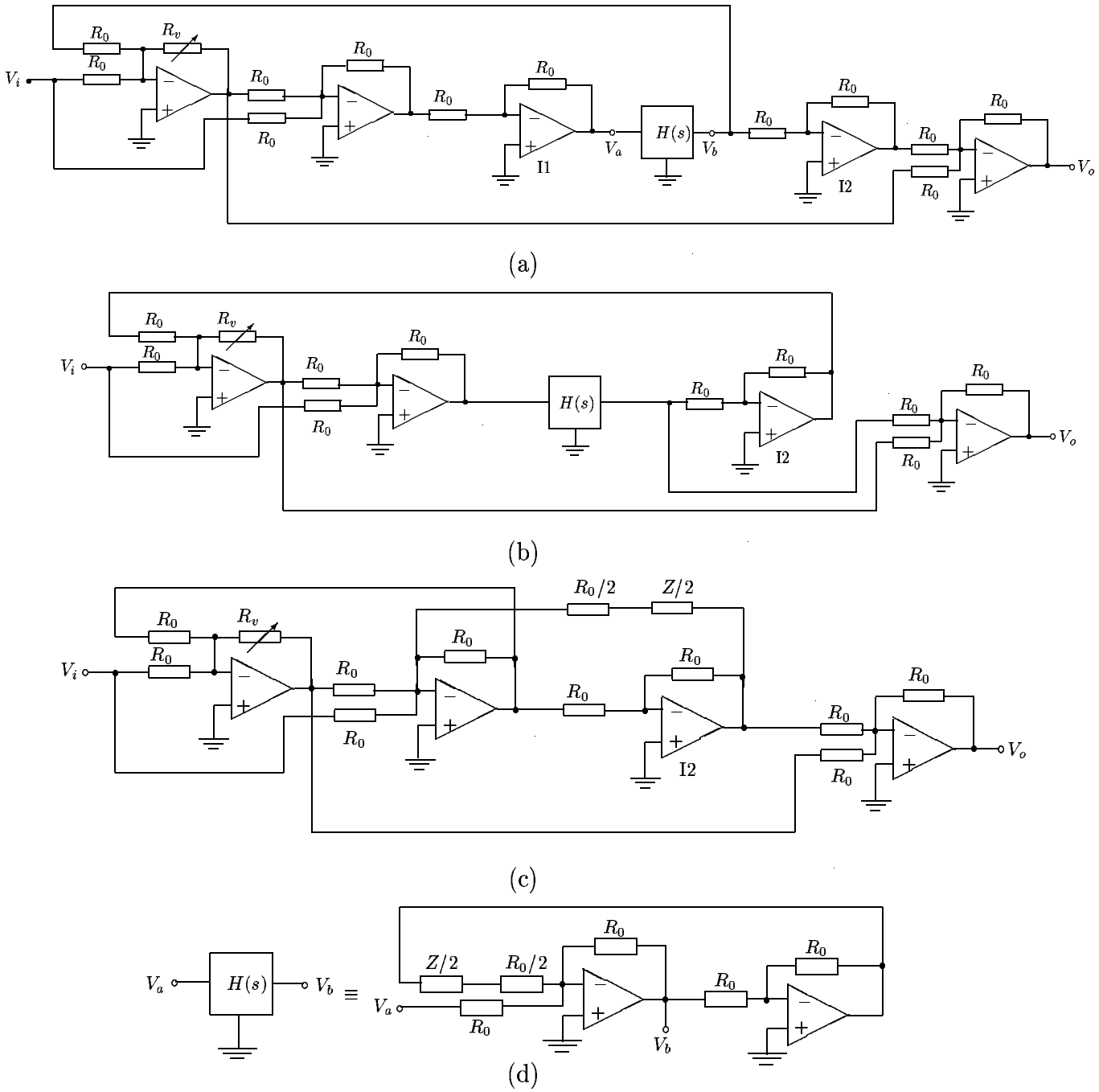


Fig. 5.10. (a) Active RC realization of $T(s)$ represented by the block diagram of Fig. 5.9(d) using 5 OA and block representation of $H(s)$, (b) realization of $T(s)$ using 4 OA and block representation of $H(s)$, (c) realization of $T(s)$ using 4 OA only, and (d) realization of $H(s)$.

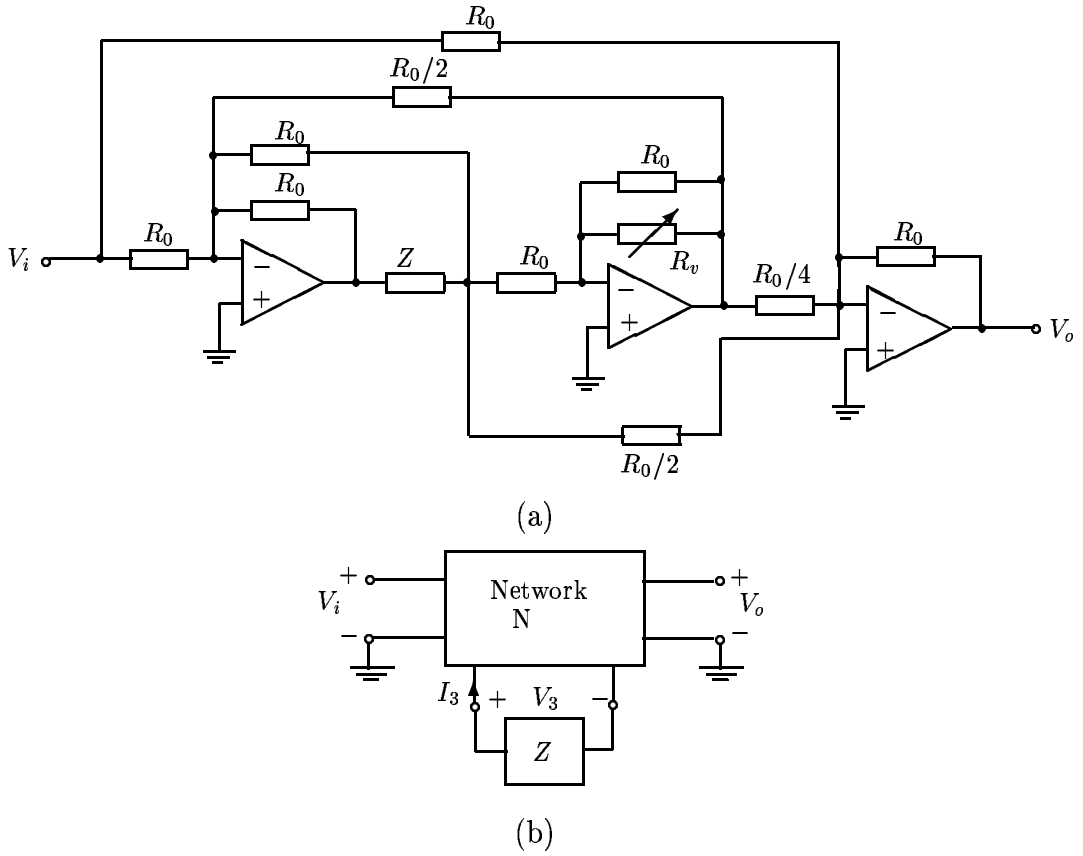


Fig. 5.11. Nowrouzian *et al.* AE: (a) Active RC realization of the AE and (b) realization of $T(s)$.

presented in the next section.

5.3 Design of amplitude equalizer with specified R_r and R_f

We shall consider the design of AEs which have only one RC impedance, only one variable resistor, and the rest all resistive elements. Let us consider the Zyoute's AE shown in Fig. 5.5(a). The analysis of the circuit leads to

$$T(s) = \frac{Z(R_v + R_e) + R_b R_e + R_v(R_e - \frac{R_b R_c}{R_a})}{Z(R_v + R_e) + R_v(R_e + R_c)}. \tag{5.55}$$

From (5.55),

$$T(s) = \frac{Z + R_b}{Z} = \frac{1}{H(s)} \quad \text{when} \quad R_v = 0, \tag{5.56}$$

Table 5.1. A comparision of various AEs.

Type	AEs	No. of OAs	No. of Resistors	Whole range	$H(s)$
Using NIC	Saraga and Zyoute's AE [91]	01	06	$[0, \infty]$	$Z/(Z+R_0)$
	Brglez's AE [92]	02	08	$[0, 2R_0]$	$R_0/(Z+R_0)$
Using 1 OA	Zyoute's AE [94]	01	05	$[0, \infty]$	$Z/(Z+2R_0)$
	Talkhan's AE [95]	01	05	$[0, R_0]$	$Z/(Z+R_0)$
With specified $H(s)$	Nowrouzian and Fuller's AE [96]	05	14	$[0, \infty]$	$(R_0+Z)/(R_0-Z)$
Using 3 OAs	Nowrouzian *et al.* AE [97]	03	11	$[0, \infty]$	$2Z/(2Z+R_0)$
Using 4 OAs	Proposed AE (Fig. 5.10(c))	04	12	$[0, \infty]$	$(R_0+Z)/(R_0-Z)$

$$T(s) = \frac{Z + \dfrac{R_aR_bR_e + R_r\,(R_aR_e - R_bR_c)}{R_a(R_r+R_e)}}{Z + \dfrac{R_r(R_e+R_c)}{(R_r+R_e)}} \quad \text{when} \quad R_v = R_r. \tag{5.57}$$

For $T(s)|_{R_v=R_r}$ to be the reciprocal of $T(s)|_{R_v=0}$, (5.56) and (5.57) demand

$$\frac{Z + \dfrac{R_aR_bR_e + R_r\,(R_aR_e - R_bR_c)}{R_a(R_r+R_e)}}{Z + \dfrac{R_r(R_e+R_c)}{(R_r+R_e)}} = \frac{Z}{Z+R_b}. \tag{5.58}$$

This is satisfied when

$$\frac{R_aR_bR_e + R_r\,(R_aR_e - R_bR_c)}{R_a(R_r+R_e)} = 0 \tag{5.59}$$

$$\Rightarrow \quad R_b = \frac{R_rR_eR_a}{R_rR_c - R_aR_e} \tag{5.60}$$

and

$$R_b = \frac{R_r(R_e+R_c)}{R_r+R_e}. \tag{5.61}$$

Equating R_b values from (5.60) and (5.61), we get

$$R_a = \frac{R_cR_r(R_e+R_c)}{R_e(R_r+2R_e+R_c)}. \tag{5.62}$$

Condition for flat response, from (5.55) when $R_v = R_f$, is

$$T(s) = \frac{Z(R_f+R_e) + R_bR_e + R_f(R_e - \dfrac{R_bR_c}{R_a})}{Z(R_f+R_e) + R_f(R_e+R_c)} = 1. \tag{5.63}$$

This requires

$$R_b R_e + R_f(R_e - \frac{R_b R_c}{R_a}) = R_f(R_e + R_c) \tag{5.64}$$

$$\Rightarrow R_e = \frac{R_f R_r}{R_r - 2R_f}. \tag{5.65}$$

For R_e to be non-negative real,

$$R_r \geq 2R_f. \tag{5.66}$$

However, when $R_r = 2R_f$, $R_e \to \infty$. Thus

$$T(s)|_{R_r=2R_f} = \frac{Z + R_b + R_f}{Z + R_f} > 1 \tag{5.67}$$

and (5.63) is not satisfied. Therefore

$$R_r > 2R_f. \tag{5.68}$$

Equations (5.61), (5.62) and (5.65) are the design equations with restrictions given by (5.68) and $H(s)$ given by (5.56). Note that Z does not appear in any of the design equations and hence can be chosen as the shaping element. One could interchange R_v and Z. However, this does not yield symmetrical gain-loss response about a flat response [94]. R_c can be assumed any arbitrary value. We choose R_c under the following three different cases for $H(s) = \frac{Z}{Z + R_0}$, i.e. when

$$R_b = R_0. \tag{5.69}$$

Design (i): $R_c = R_e$.

In this case, from (5.61), (5.62), and (5.69), we get

$$R_0 = \frac{2R_r R_e}{R_r + R_e}, \tag{5.70}$$

$$R_a = \frac{2R_r R_e}{R_r + 3R_e}. \tag{5.71}$$

Thus R_e can be chosen from (5.70) to accommodate any specified value of R_r. Then R_f gets fixed from (5.65) and cannot be chosen independently.

Design (ii): $R_c = R_0$.

From (5.61) and (5.62), we get, respectively

$$R_0 = R_r \tag{5.72}$$

and

$$R_a = \frac{R_r^2}{2R_e}. \tag{5.73}$$

Thus R_r gets fixed from (5.72) and cannot be chosen arbitrarily. R_e can, however, be chosen to accommodate any specified value of R_f from (5.65).

Thus, in the above designs (i) and (ii), we can accommodate specified value of either R_r or R_f but not both simultaneously. The following design (iii) overcomes this difficulty.

Design (iii): $R_c = R_0 + \frac{(1-n)}{n}R_e$ where n is a positive real.

In this case, from (5.61) and (5.69), we get

$$n = \frac{R_r}{R_0} \tag{5.74}$$

and from (5.62) and (5.74), we get

$$R_a = \frac{[nR_0 + (1-n)R_e]R_r}{n(n+1)R_e}. \tag{5.75}$$

Thus, specified values of both R_r and R_f can be accommodate by choosing n in (5.74) and R_e in (5.65), respectively. This is the distinct advantage of this design. Further, designs (i) and (ii) are the special cases of design (iii) when $R_e = \frac{R_0}{2}$ and $n = 1$, respectively.

Based on design (iii), we give five different equalizers with the specified values of R_r and R_f.

Equalizer 5.1

Let $R_r = \infty$ and $R_f = R_0/2$. Then from (5.74), $n = \infty$. From (5.65), $R_e = \frac{R_0}{2}$. Then $R_c = \frac{R_0}{2}$ and from (5.75), $R_a = R_0$. These are the values chosen by Zyoute [94].

Equalizer 5.2

Let $R_r = R_0$ and $R_f = R_0/3$. Then from (5.74), $n = 1$. From (5.65), $R_e = R_0$. Then $R_c = R_0$ and $R_a = \frac{R_0}{2}$. These are the values chosen by Talkhan *et al.* [95].

Equalizer 5.3

Let $R_r = R_0$ and $R_f = R_0/4$. Then, from (5.74) $n = 1$ and from (5.65), $R_e = \frac{R_0}{2}$. Then $R_c = R_0$, and from (5.75), $R_a = R_0$. These are the values chosen by Talkhan *et al.* [95]. Thus, Talkhan *et al.* have Equalizers 5.2 and 5.3 for different R_f but the same R_r.

Similarly, two more Equalizers 5.4 and 5.5 with different values of R_r and R_f have been given in Table 5.2. Equalizer 5.1 is the same as in [94]. Equalizers 5.2 and 5.3

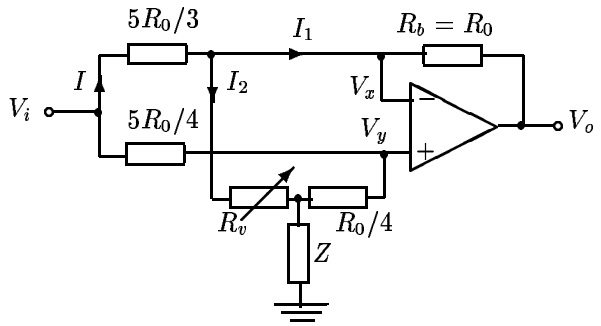


Fig. 5.12. Circuit for Equalizer 5.4.

Table 5.2. Design of the equalizers for few sets of R_r and R_f.

	n	R_r	R_f	R_a	R_b	R_c	R_e	x
Equalizer 5.1 [94]	∞	∞	$\frac{1}{2}R_0$	R_0	R_0	$\frac{1}{2}R_0$	$\frac{1}{2}R_0$	$\frac{2R_v}{R_0}$
Equalizer 5.2 [95]	1	R_0	$\frac{1}{3}R_0$	$\frac{1}{2}R_0$	R_0	R_0	R_0	$\frac{2R_v}{R_0-R_v}$
Equalizer 5.3 [95]	1	R_0	$\frac{1}{4}R_0$	R_0	R_0	R_0	$\frac{1}{2}R_0$	$\frac{3R_v}{R_0-R_v}$
Equalizer 5.4	$\frac{1}{2}$	$\frac{1}{2}R_0$	$\frac{1}{8}R_0$	$\frac{5}{3}R_0$	R_0	$\frac{5}{4}R_0$	$\frac{1}{4}R_0$	$\frac{6R_v}{R_0-2R_v}$
Equalizer 5.5	$\frac{1}{4}$	$\frac{1}{4}R_0$	$\frac{1}{10}R_0$	R_0	R_0	$\frac{5}{2}R_0$	$\frac{1}{2}R_0$	$\frac{6R_v}{R_0-4R_v}$

were considered in [95] where different values of R_e gives different R_f, but R_r remains the same. Thus we see that design (iii) can accommodate arbitrary values of R_r and R_f except for the constraint given by (5.68). The circuit for Equalizer 5.4 is shown in Fig. 5.12.

It may be noted that the design is applicable for both the fan and bump equalizers and also for the inverse networks [117]. The design procedure is applicable for all the AEs discussed in Section 5.2.

5.4 Amplitude equalizers employing CM building blocks

The OA circuit shown in Fig. 5.12 can be transformed into the circuits employing CM building blocks having terminal characteristics $V_x = V_y$, $I_z = I_x$ and $I_y = 0$ (such as CCII, CFA) as shown in Fig. 5.13 [47]. Such circuits can operate at high frequencies

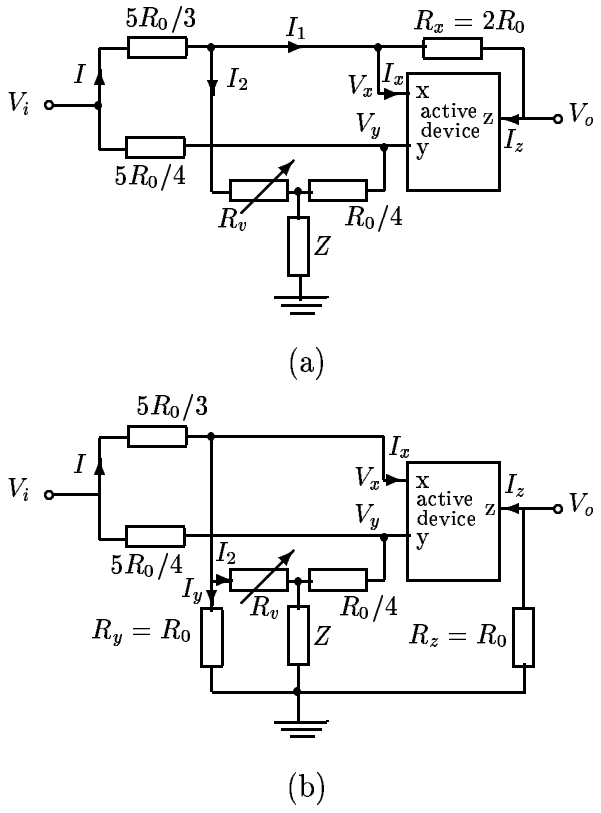


Fig. 5.13. Transformed equalizers employing CM building blocks such as CCII, CFA.

compared to OA based circuits. In the circuit shown in Fig. 5.12,

$$I = I_1 + I_2 = \frac{V_x - V_o}{R_b} + I_2. \tag{5.76}$$

From the circuit shown in Fig. 5.13(a),

$$I = I_1 + I_2 = (I_x + I_z) + I_2 = 2I_z + I_2 = 2\left(\frac{V_x - V_o}{R_x}\right) + I_2 \tag{5.77}$$

and from the circuit shown in Fig. 5.13(b),

$$I = I_y + I_x + I_2 = I_y + I_z + I_2 = \frac{V_x}{R_y} - \frac{V_o}{R_z} + I_2. \tag{5.78}$$

For the circuits shown in Figs. 5.13(a) and 5.13(b) to be equivalent to that shown in Fig. 5.12, from (5.76) and (5.77), we get

$$R_x = 2R_b \tag{5.79}$$

and from (5.76) and (5.78), we get

$$R_y = R_z = R_b. \tag{5.80}$$

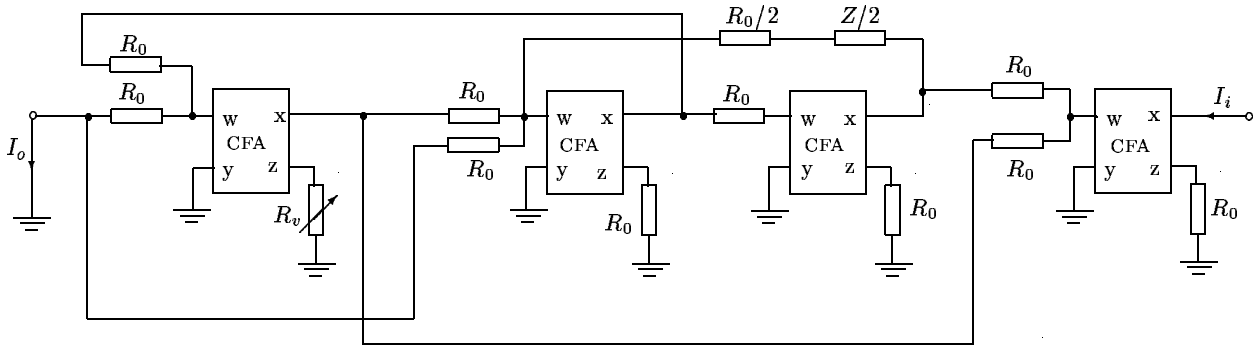


Fig. 5.14. CFA based CM AE obtained from the OA based VM AE of Fig. 5.10(c).

Although the circuit of Fig. 5.13(b) requires one extra resistor compared to the circuit of Fig. 5.13(a), the three resistors are getting grounded as well the total resistance remains the same. Such grounded topology is useful for IC technology.

Using VM-to-CM transformation method proposed in Chapter 2, one can convert the OA based VM AE of Fig. 5.10(c) into CFA based CM AE as shown in Fig. 5.14.

Now, consider the circuit using CDBA ($V_x = 0, V_y = 0, I_z = I_y - I_x, V_w = V_z$) as shown in Fig. 5.15(a). The analysis of the circuit leads to,

$$T(s) = \frac{I_o}{I_i} = \frac{\frac{R_v}{Z} - 1}{\frac{R_v}{Z} + 1}. \tag{5.81}$$

This $T(s)$ is in similar form as that of in (5.17) when $R_a = R_b$. Following the similar technique used for realizing Brglez's AE in Subsection 5.2.1(ii), we get

$$T(s) = \frac{1 + \left(\frac{R_p}{R_p - 2R_0}\right)\frac{R_0 - Z}{R_0 + Z}}{\frac{R_p}{R_p - 2R_0} + \frac{R_0 - Z}{R_0 + Z}} \tag{5.82}$$

where $R_v = R_p - R_0$. Comparing (5.82) with (5.1), we get

$$x = \frac{R_p}{R_p - 2R_0} \tag{5.83}$$

and

$$H(s) = \frac{R_0 - Z}{R_0 + Z}. \tag{5.84}$$

The complete CM AE is shown in Fig. 5.15(b). The whole range of the AE is [0, $2R_0$].

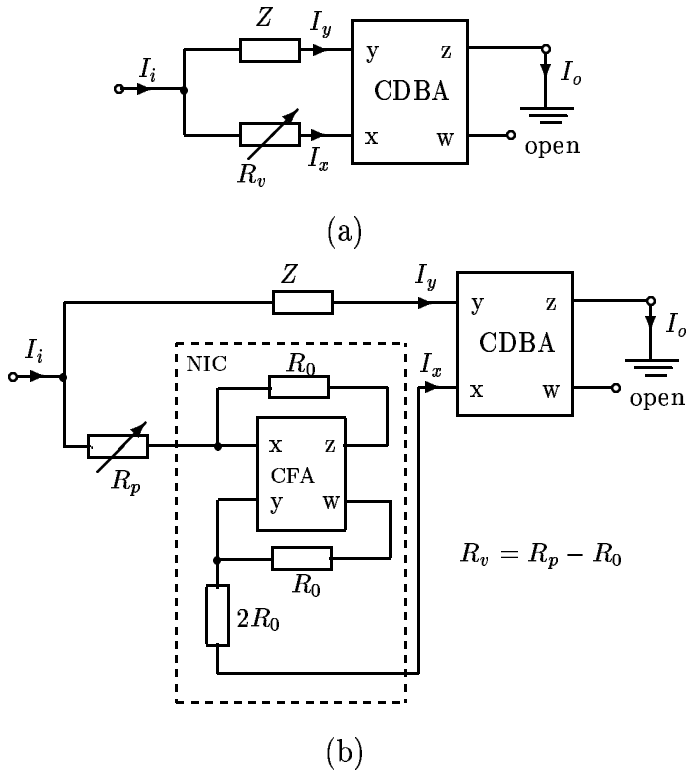
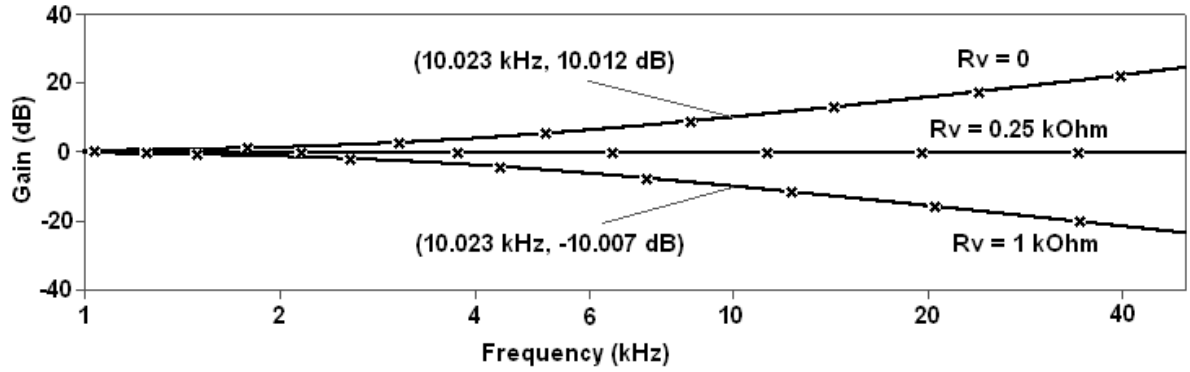


Fig. 5.15. (a) CDBA based circuit and (b) CDBA based CM AE.

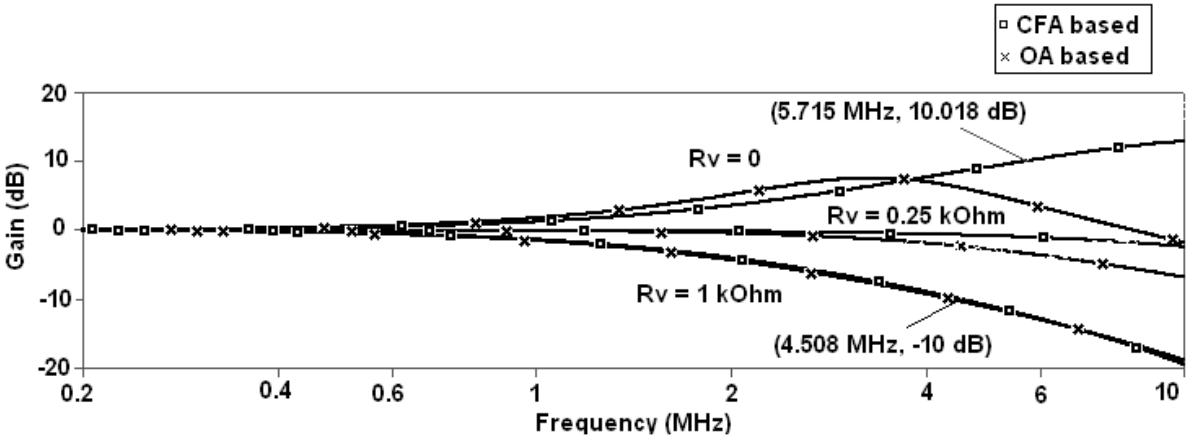
5.5 Simulation results

The circuit shown in Fig. 5.12 is designed for $R_r = R_0/2$ and $R_f = R_0/8$ and to provide ± 10 dB variation at a frequency of 10 kHz. The circuit is simulated using PSPICE [110] using high frequency OA such as AD817. Here, $Z = 1/j\omega C$. Taking $R_b = 2$ kΩ, we get $R_e = 0.5$ kΩ, $R_a = 3.33$ kΩ, $R_c = 2.5$ kΩ, $R_v = 1$ kΩ (potentiometer), $C = 23.87$ nF. The simulation results are given in Fig. 5.16(a).

The circuit shown in Fig. 5.13 is simulated for ± 10 dB variation at a frequency of 5 MHz with same R_r and R_f using CFA AD844. The only difference in the designed value is $C = 0.0477$ nF. For the same ± 10 dB variation at frequency 5 MHz, the OA based circuit is resimulated using OA AD817. The simulation results are given in Fig. 5.16(b). The simulation results show that the CFA based circuit works better at higher frequencies as compared to the OA based one. The simulation results are in good agreement with the theory.



(a)



(b)

Fig. 5.16. Frequency responces of the equalizers using (a) OA for ± 10 dB variation at 10 kHz frequency and (b) OA and CFA for ± 10 dB variation at 5 MHz frequency.

5.6 Concluding remarks

Some of the earlier reported AEs have been derived systematically and logically, and during this process, some new AEs have been derived. A set of new CM AEs employing CM building blocks have been proposed. A simple design procedure for realizing an AE with a single OA and single variable resistor has been proposed. It allows to control any specified values of R_r and R_f. The designs of AEs given by Zyoute [94] and Talkhan *et al.* [95] can be obtained as special cases from the proposed design procedure. The AEs employing CM building blocks operates better at higher frequencies as compared to the OA based ones. Simulation results are in good agreement with the theory.

Chapter 6

OSCILLATOR EMPLOYING CM BUILDING BLOCK

6.1 Introduction

Differential capacitive sensors are used to detect the changes of several physical variables like position, liquid level, angular speed, fluidic flow, force, pressure, etc. [118]. To extract such measurands, several techniques such as capacitance-to-voltage [119], capacitance-to-phase [120], capacitance-to-frequency [121], [122], and capacitance-to-current [123] conversions have been proposed. Of these, the direct sensor-to-digital conversion methods possess reduced complexity and provide increased reliability [124]. Recently, George *et al.* [125] have proposed a linear variable differential capacitive transducer for sensing planar angles by using capacitance-to-voltage conversion technique. Later, Madhu Mohan *et al.* [124] developed a digital converter for converting capacitance of differential-type capacitive sensor to a proportional digital value. In both the cases, they require a pair of precision dc reference voltages on which the output sensitivity depends. Pennisi [123] has proposed a differential-capacitance transducer in CM which converts capacitance to current. This transducer provides a linear relation between the displacement and the output current, but it requires a constant current source, increasing the circuit complexity.

A large number of oscillator circuits have been reported in the past and some of them can be used for sensor applications [98], [99]. These oscillator based sensor

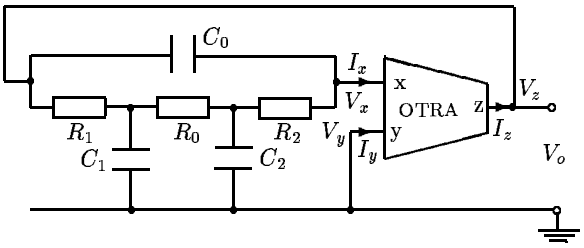


Fig. 6.1. BLO circuit.

circuits are used for sensing the change in velocity of the surface-acoustic-wave and for sensing the resistive unbalance of a Wheatstone bridge. For use as a differential capacitive sensor, a new high-frequency oscillator circuit that has independent control for condition of oscillation and frequency of oscillation and has a high linearity and sensitivity for measurement of displacement is developed.

6.2 Bridged-ladder oscillator

The proposed bridged-ladder oscillator (BLO) circuit is shown in Fig. 6.1 where OTRA has the terminal characteristics [31]:

$$\begin{bmatrix} V_x \\ V_y \\ V_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ -R_m & R_m & 0 \end{bmatrix} \begin{bmatrix} I_x \\ I_y \\ I_z \end{bmatrix}. \tag{6.1}$$

Assuming ideal OTRA ($R_m = \infty$), application of Barkhausen's criterion [126] leads to the condition for sinusoidal oscillation as

$$\frac{1}{C_0} = (R_0 + R_1 + R_2) \times \left[\frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} + \frac{1}{R_0}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\right] \tag{6.2}$$

and the frequency of oscillation

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2}\left[\frac{1}{R_1 R_2} + \frac{1}{R_0}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)\right]}. \tag{6.3}$$

Choosing $R_1 = R_2 = R$ and $R_0 = kR$, from (6.2) and (6.3) we get the condition for oscillation

$$\frac{1}{C_0} = \frac{(1+k)(2+k)}{k}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \tag{6.4}$$

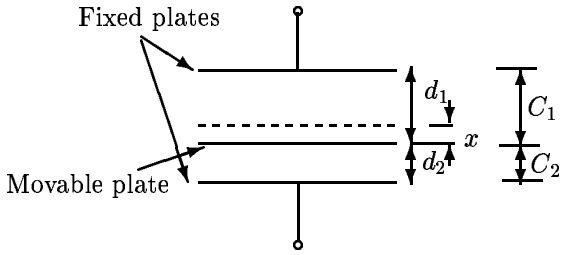


Fig. 6.2. Push-pull type variable displacement capacitor.

and the frequency of oscillation

$$\omega_0 = \frac{1}{R}\sqrt{\frac{1}{C_1 C_2}\left(\frac{2+k}{k}\right)}. \tag{6.5}$$

Although the condition for oscillation can be satisfied by adjusting C_0, the frequency of oscillation cannot be adjusted independently. To achieve independent adjustments of both, we have two alternatives.

6.2.1 Capacitor-tuned oscillator

In (6.4) and (6.5), adjusting C_1, C_2 keeping $\left(\frac{1}{C_1}+\frac{1}{C_2}\right)$ constant, ω_0 can be tuned without disturbing the condition for oscillation and C_0 can be adjusted to satisfy the condition for oscillation without affecting ω_0. However, it is practically inconvenient to change C_1 and C_2 keeping $\left(\frac{1}{C_1}+\frac{1}{C_2}\right)$ constant. But, if C_1 and C_2 represent the push-pull arrangement as shown in Fig. 6.2 such that $C_{1,2} = \frac{\epsilon A}{d_{1,2}}$ where ϵ is the dielectric constant, A $(= b \times 2l)$ is the area of the capacitor plate, $2l$ is the length and b is the breadth of the plates, $2d$ is the total distance between the fixed plates, $d_1 = d + x$ and $d_2 = d - x$, x is the displacement, the condition of oscillation becomes

$$\frac{1}{C_0} = \frac{(1+k)(2+k)}{\epsilon 2lbk}(2d) \tag{6.6}$$

and the frquency of oscillation is given by

$$\omega_0 = \frac{1}{\epsilon 2lbR}\sqrt{(d^2 - x^2)\left(\frac{2+k}{k}\right)}. \tag{6.7}$$

The two can now be adjusted independently if C_0 and x are chosen as the variables.

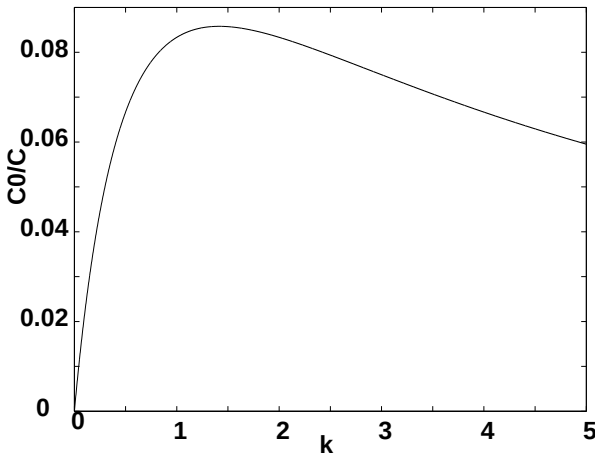


Fig. 6.3. Plot of C_0/C versus k.

6.2.2 Resistor-tuned oscillator

Let $C_1 = C_2 = C$. Then from (6.4) and (6.5) we get the condition for oscillation as

$$\frac{C_0}{C} = \frac{1}{2}\left[\frac{k}{(1+k)(2+k)}\right] \tag{6.8}$$

and the frequency of oscillation as

$$\omega_0 = \frac{1}{CR}\sqrt{\frac{2+k}{k}}. \tag{6.9}$$

Case (i): Choosing $k = 1$ so as to have equal-valued resistors, we get the condition for oscillation as

$$C_0 = 0.0833C \tag{6.10}$$

and the corresponding

$$\omega_0 = \frac{\sqrt{3}}{RC}. \tag{6.11}$$

Thus, both the condition for oscillation and ω_0 can be adjusted independently by varying C_0 and R, respectively. However, a three ganged resistor arrangement is required for this purpose.

Case (ii): The plot of C_0/C versus k as given by (6.8) is shown in Fig. 6.3. It may be noted that C_0 is always less than C for any value of k. Therefore, the three capacitors cannot be of equal value. However, C_o is closest to C when $k = \sqrt{2}$ and the corresponding C_0 and ω_0 are,

$$C_0 = 0.0858C, \tag{6.12}$$

$$\omega_0 = \left(\frac{1.5537}{CR}\right). \tag{6.13}$$

Although the condition for oscillation and ω_0 can be adjusted independently by varying C_0 and R, respectively, it is practically inconvenient to change R_0 and R keeping $R_0 = \sqrt{2}R$. Moreover, the value of C_0 is not significantly different from that when $k = 1$. Hence the capacitor-tuned oscillator is preferable from the practical point of view.

6.3 Displacement sensor and its design

Equation (6.7) shows that ω_0 is a function of x. Hence, the oscillator circuit shown in Fig. 6.1 can be used as a displacement sensor when the capacitors C_1 and C_2 are arranged as shown in Fig. 6.2. The circuit can be designed for specified maximum value of $x = x_m$ and the desired maximum and minimum values of ω_0 at $x = 0$ and $x = x_m$, respectively. As mentioned above, we choose $k = 1$. Then from (6.7) we get

$$\omega_0|_{x=0} = \frac{1}{\epsilon AR} d\sqrt{3} \tag{6.14}$$

and

$$\omega_0|_{x=x_m} = \frac{1}{\epsilon AR}\sqrt{3(d^2 - x_m^2)}. \tag{6.15}$$

From (6.14) and (6.15), we get

$$d = \sqrt{\left(\frac{n^2}{n^2 - 1}\right)} x_{\mathrm{m}} \tag{6.16}$$

where

$$n = \frac{\omega_0|_{x=0}}{\omega_0|_{x=x_m}}. \tag{6.17}$$

Now R can be calculated from (6.14). From (6.7)

$$\omega_0 = \frac{d\sqrt{3}}{\epsilon AR}\sqrt{1 - \left(\frac{x}{d}\right)^2}. \tag{6.18}$$

Therefore,

$$\omega_n = \frac{\omega_0}{\omega_0|_{x=0}} = \sqrt{1 - (x_n)^2}, \quad x_n = \frac{x}{d} \tag{6.19}$$

$$\omega_n = \frac{\omega_0}{\omega_0|_{x=0}} \cong 1 - \frac{1}{2}x_n^2, \quad \text{if } x_n << 1. \tag{6.20}$$

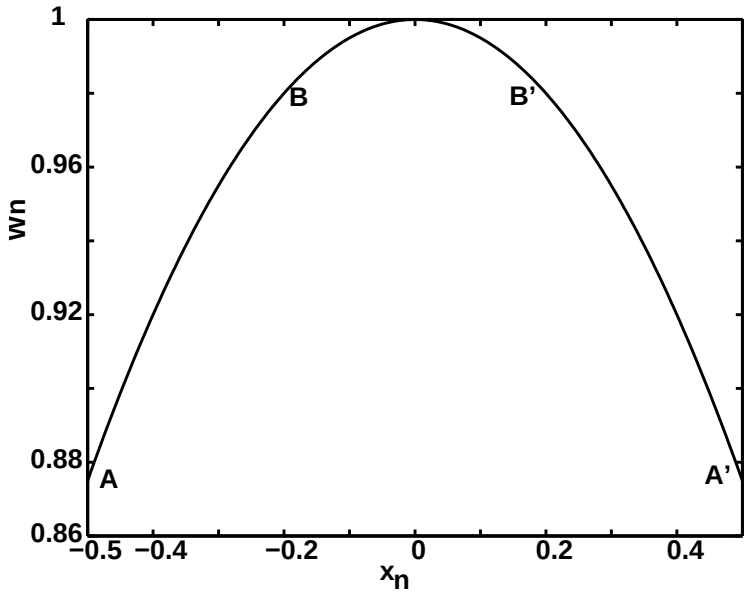


Fig. 6.4. Plot of normalized ω_n versus normalized x_n.

The plot of normalized frequency ω_n versus x_n is shown in Fig. 6.4. It can be seen that ω_n varies approximately linear in the range AB, A'B'. Hence, the sensor should be operated in these ranges.

The sensor circuit is initially designed for $x_m = \pm\ 5\ \mu m$, $d = 10\ \mu$m. Choosing the frequency corresponding to x at the middle point of AB (x=$-3.5\ \mu$m) $\omega_0|_{x=-3.5\ \mu m} =$ 10 Mrad/sec, air as the dielectric media ($\epsilon = 8.854 \times 10^{-12}$ F/m), $A = 25 \times 25$ mm^2, and $k = 1$, R obtained is 293.2 Ω. The corresponding C and C_0 are 0.5534 nF and 0.0461 nF, respectively. The theoretical plot of ω_0 versus x for the designed sensor is shown in Fig. 6.5. Since the linear region is confined to range AB as discussed earlier, the displacement is offset by $-3.5\ \mu$m so that $x = 0$ is shifted to C in Fig. 6.6. The circuit is therefore suitable for measurement in the range $x = \pm 1.5\ \mu$m. The straight line (best curve fit) is drawn using the method of least squares from the obtained simulation data and is shown in Fig. 6.6. The linearity is a measure of maximum deviation of the simulated point from this straight line. The displacement is positive (negative) for ω_0 greater (smaller) than 10 Mrad/sec. Since the output is a frequency, it can be used for a direct digital readout without the need for analog-to-digital conversion [127].

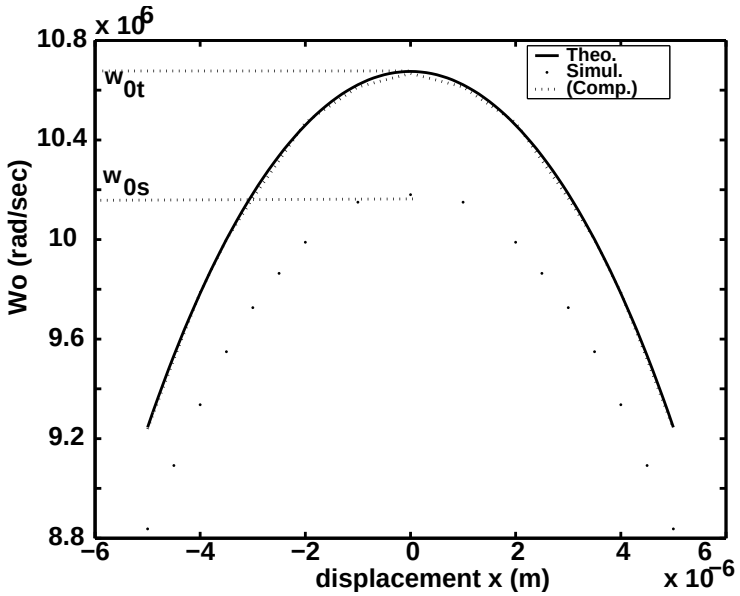


Fig. 6.5. Plot of frequency of oscillation (ω_0) versus displacement (x).

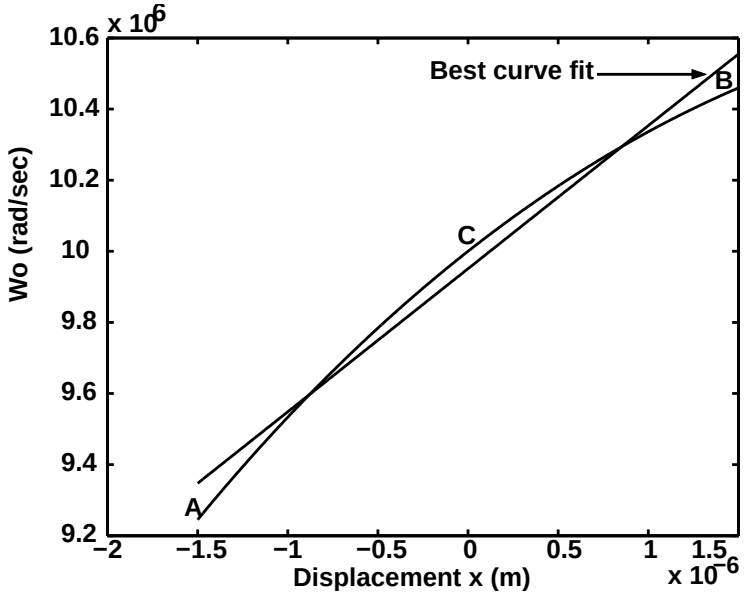


Fig. 6.6. Plot of ω_0 versus x with displacement offset in BLO based sensor.

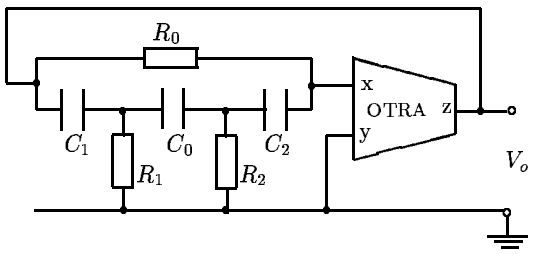


Fig. 6.7. RC:CR transformed BLO circuit.

6.4 Bridged-ladder oscillator versus twin-T oscillator based sensor circuit

For comparison purpose, we analyze two other ($3C$, $3R$) sensors: one derived from the above sensor using RC:CR transformation and the other based on twin-T oscillator (TTO).

The RC:CR transformation on the circuit of Fig. 6.1 gives a circuit shown in Fig. 6.7. Choosing $C_1 = C_2 = C_0 = C$, analysis yields the condition of oscillation as

$$R_0 = 6(R_1 + R_2) \tag{6.21}$$

and the frequency of oscillation

$$\omega_0 = \frac{1}{C}\sqrt{\frac{1}{3R_1R_2}}. \tag{6.22}$$

Thus, adjusting R_1 and R_2 keeping $(R_1 + R_2)$ constant, both the condition of oscillation and the frequency of oscillation can be adjusted independently. To achieve this, one possible arrangement is shown in Fig. 6.8 where $R_{1,2} = \frac{\rho\, l_{1,2}}{A}$, ρ is the resistivity of the material used, A is the cross-sectional area of the resistor, l is the length, $l_1 = l + x$ and $l_2 = l - x$, and x is the displacement, then the condition of oscillation becomes

$$R_0 = 6\frac{\rho}{A}(l_1 + l_2) \tag{6.23}$$

and the frequency of oscillation becomes

$$\omega_0 = \frac{A}{\rho\, C}\sqrt{\frac{1}{3(l^2 - x^2)}}. \tag{6.24}$$

The two can now be adjusted independently if R_0 and x are chosen as the variables.

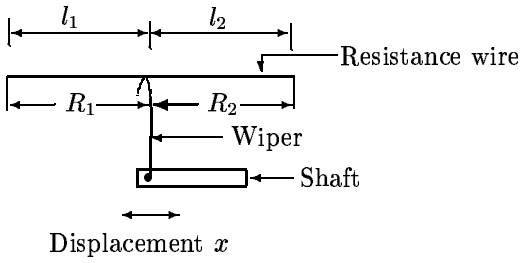


Fig. 6.8. Resistor arrangement.

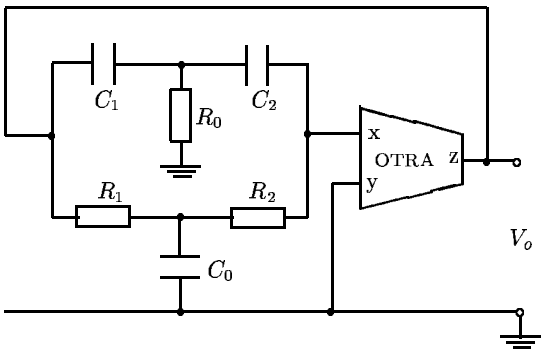


Fig. 6.9. TTO based sensor circuit.

Thus, RC:CR transformed BLO circuit can also be used as a resistive displacement sensor. However, the friction between the wiper and the resistance track results in resolution limitation and less life expectancy [128]. Hence, the original capacitive displacement sensor should be preferred.

Let us consider another sensor based on TTO shown in Fig. 6.9. Choosing $R_1 = R_2 = R_0 = R$, analysis gives the condition of oscillation as

$$\frac{1}{C_0} = \frac{1}{2(C_1 + C_2)} \tag{6.25}$$

and the frequency of oscillation as

$$\omega_0 = \frac{1}{R}\sqrt{\frac{1}{2C_1C_2}}. \tag{6.26}$$

Thus, adjusting C_1 and C_2 keeping (C_1+C_2) constant, both the condition of oscillation and the frequency of oscillation can be adjusted independently. To adopt the oscillator as a displacement sensor, let C_1 and C_2 be arranged as shown in Fig. 6.10 where $C_{1,2} = \frac{\epsilon A_{1,2}}{d}$, ϵ is the dielectric constant, d is the distance between the fixed and movable plates, $A_{1,2} = l_{1,2} \times b$, $l_1 = l + x$, $l_2 = l - x$ where $2l$ is the length and b

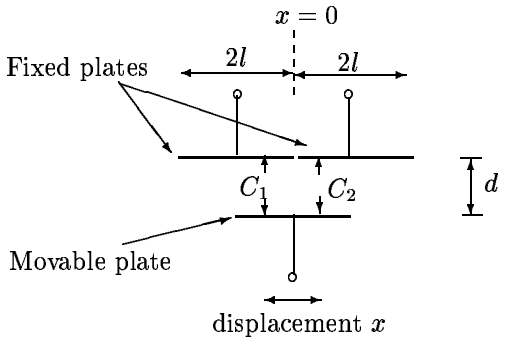


Fig. 6.10. Capacitor arrangement in TTO based displacement sensor.

is the bredth of the plates, x is the displacement and $x < l$, then the condition of oscillation becomes

$$\frac{1}{C_0} = \frac{d}{2\epsilon b}\left(\frac{1}{2l}\right) \tag{6.27}$$

and the frequency of oscillation is given as

$$\omega_0 = \frac{d}{\epsilon R b}\sqrt{\frac{1}{2(l^2 - x^2)}}. \tag{6.28}$$

Thus, the condition of oscillation and the frequency of oscillation can be adjusted independently if C_0 and x are chosen as the variables. Thus, TTO based sensor circuit can also be used as a capacitive displacement sensor.

6.5 Simulation results

The designed BLO based sensor circuit is simulated using ORCAD PSPICE [110]. OTRA is realized using commercially available CFAs, AD844s [115]. The displacement x is simulated using various pairs of capacitors (C_1, C_2) such that $\left(\frac{1}{C_1} + \frac{1}{C_2}\right)$ is constant. The simulation plot of ω_0 versus x is also shown in Fig. 6.5. The simulated values are lower than the theoretical values. This may be due to the OTRA nonidealities. The error has been componensated by reducing R to a value $\left(\frac{\omega_{0s}}{\omega_{0t}}\right)$ times R. After compensating the effect of OTRA nonidealities, the plot from the simulator has excellent match with the theoretical plot as can be seen from Fig. 6.5. The $R-$tuned oscillator circuit is also simulated. The theoretical and simulated plots of ω_0 versus R are shown in Fig. 6.11. In both the tunings, once the condition of oscillation is satisfied, sinusoidal oscillations are obtained over the entire range of x

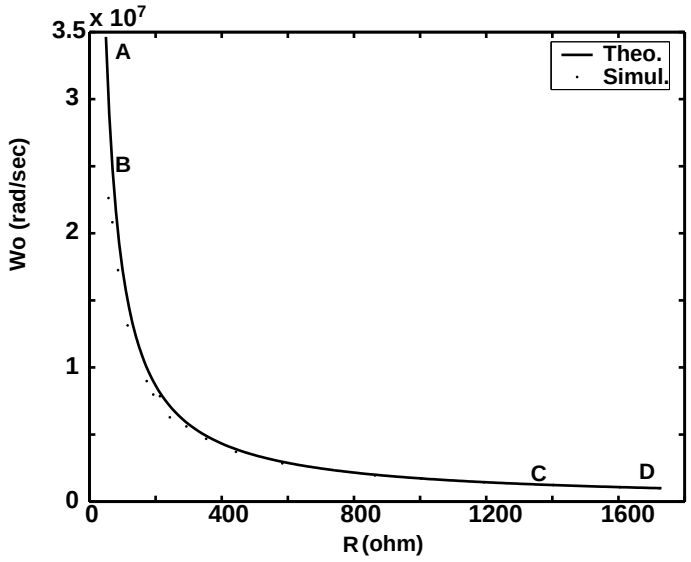


Fig. 6.11. Plot of ω_0 versus R.

or R without any further tuning, i.e., the change in C_0. The oscillator circuits does not have a separate amplitude stabilizer and the oscillation levels are limited by the supply voltages. The simulation resulted in peak-to-peak amplitudes of 4 V and 21 V for ± 6 V and ± 15 V supply voltages, respectively.

The TTO based sensor is designed with the following specifications: $x_m = \pm 1.5$ mm, $d = 10$ μm, $\omega_0|_{x=0} = 10$ Mrad/sec, air as the dielectric media, $l_1 = l_2 = 25$ mm, $b = 25$ mm, $R = 127.78$ Ω, $C = 0.553$ nF, and $C_0 = 2.212$ nF. The theoretical plot of ω_0 versus x after the displacement offset is shown in Fig. 6.12. Note that, in both the (6.24) and (6.28), the term $(l^2 - x^2)$ appears in the denominator. Hence the nature of the plot of ω_0 versus x in both the cases will be the same.

Table 6.1 gives a comparison of the total capacitance C_t required by the two capacitive sensors based on BLO and TTO for the same ω_0 $(=\frac{1}{\sqrt{6}RC})$, and the same total resistance R_t $(=3R)$. BLO based displacement sensor requires less total capacitance C_t. This will lead to less area and higher speed of operation in integrated circuits [129]. Table 6.1 also shows the sensitivity, span, resolution, non-linearity observed for the same ω_0 =10 Mrad/sec at x=0. It can be seen that the BLO based displacement sensor is superior to the TTO one as the former sensor can measure smaller displacements with better resolution and higher linearity. The BLO based displacement sensor measures the displacement in the direction perpendicular to length of

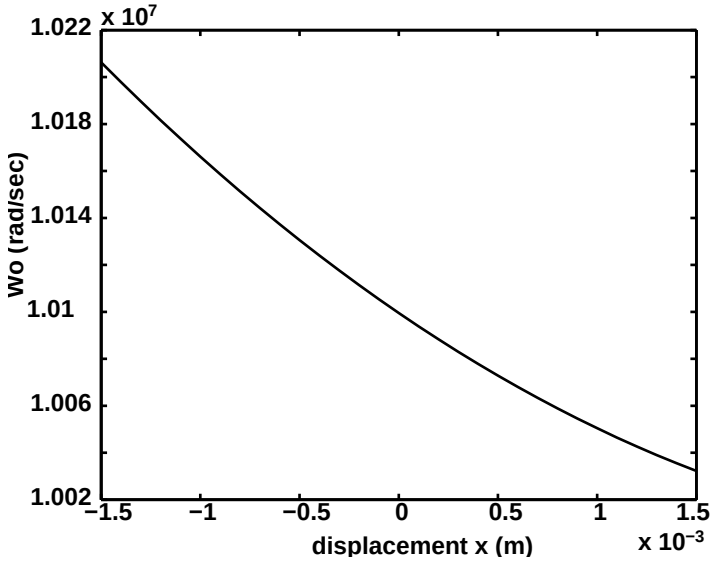


Fig. 6.12. Plot of ω_0 versus x with displacement offset in TTO based sensor.

Table 6.1. Comparison of total capacitance C_t and various quality parameters.

Parameters	**BLO based**	**TTO based**
Total capacitance (C_t)	8.84 C	10.39 C
Sensitivity (Hz/m)	4.0×10^{11}	5.8×10^{6}
Span	-1.5 to $+1.5$ μm	-1.5 to $+1.5$ mm
Resolution	15 nm	1 mm
Non-linearity (% of F. S.)	8.419	6.896

the plate whereas the TTO based displacement sensor measures it along the length of the plate.

6.6 Concluding remarks

A new high frequency oscillator circuit has been developed which can be used as a micrometer displacement sensor. Although both C-tuned and R-tuned oscillators give independent control of the condition of oscillation and frequency of oscillation, the former is more practicable and ideally suited for the displacement sensor. The

sensor can measure displacements of the order of few microns accurately with higher sensitivity and linearity. The effect of OTRA nonidealities has been compensated. An offset in the displacement has been introduced so that the sensor operates in the linear region for its entire range. The BLO based displacement sensor has been compared with two alternatives: one derived using RC:CR transformation on it and the other based on TTO. It has been found that it can measure extremely small displacements with better resolution and higher linearity. Moreover, it requires less total capacitance and hence should be preferred in IC technology. The simulation results are found to be in close agreement with the theoretical ones.

Chapter 7

SUMMARY AND CONCLUSIONS

The thesis deals with various synthesis techniques used for realizing analog circuits like filters, equalizers, oscillators employing CM building blocks such as CC, CFA, FTFN, CDBA, and OTRA. The CM building blocks are attaractive because of their wider bandwidth, higher slew rate, and lower power consumption compared to the VM counterparts. The analog circuits using these devices have simple topologies and are suitable for integration in CMOS technology. As a large number of OA based circuits with elegant realization procedures are already available, it is worthwhile to convert them into the circuits based on CM building blocks. Therefore, the initial contribution of the thesis deals with the transformation technique for converting VM circuits to CM circuits. A transformation technique for converting OA, CC, FTFN, and CFA based VM circuits into corresponding CM circuits without requiring any additional circuit elements and any change in the circuit topology has been proposed in Chapter 2. Later, the transformation technique is extended to convert OA based VM/CM circuits into VM/CM circuits employing CM building blocks and vice versa. The use of CM building blocks in analog circuits help in performance enhancement. The sensitivities to nonidealities of these CM building blocks have been found not more than unity in magnitude.

In IC technology, it is desirable to have circuit topologies with equal-valued grounded capacitors. Therefore the next main thrust of the work reported has been

on developing the novel synthesis techniques for realizing analog circuits like filters, equalizers, oscillators employing CM devices such as CC, CFA, FTFN, OTRA, using (i) equal-valued grounded capacitors (EVGCs) and (ii) minimal number of active and passive elements. Most of the synthesis procedures for analog circuits already available require a large number of active devices and do not lead to EVGC realizations. Three synthesis procedures for realizing a class of transfer functions of any order with negative real poles using only one active device have been proposed in Chapter 3. These procedures lead to circuit design with minimum number of passive elements. Since, synthesis procedures are restricted to the transfer functions with distinct negative real poles only, they are restricted to low Q values. To overcome this drawback, another procedure that can realize any stable voltage/current transfer function of any order has also been developed. It has been elaborated with the design of nth order all-pass transfer function. These synthesis procedures lead to the grounded capacitor realizations but may not lead to equal-valued capacitor realizations. Later, an EVGC realization of a low-pass filter is also proposed which is capable of realizing any desired gain constant and accommodating any specified source conductance and have extremely low passive sensitivities. Such realizations allow easy compensation for the parasitic capacitors.

In Chapter 4, a procedure for realizing a ladder filter from passive RLC to active all equal-valued grounded capacitors has been proposed. The ladder filters have been simulated by simulating the functional relations for various node voltages and branch currents. The realization procedure has been illustrated with the simulation of nth order band-pass filter. All other generic filter functions except the all-pass one have been derived from the band-pass filter. The realization procedure allows the simulations of all these filters with all the capacitors grounded and that too of equal value. Although these ladder filters can be simulated using OA, CC, and FTFN, none of them can yield an all grounded-capacitor simulation. Therefore, only CFA based ladder filter realizations have been discussed in detail. They work satisfactorily at higher frequencies. These novel grounded-capacitor realizations allow easy compensation for the parasitic capacitors, latter being in parallel with the grounded capacitors.

A simple design procedure for realizing an amplitude equalizer with a single OA and single variable resistor has been developed in Chapter 5. It gives flexibility in

choosing the range of variable resistor and the value of the same variable resistor at which a flat response can be achieved. The design procedure has been further applied to the transformed variable equalizers with CM devices which operates better at higher frequencies as compared to the OA based ones.

Finally, a novel high-frequency bridged-ladder oscillator (BLO) based micrometer displacement sensor employing CM building block has been proposed in Chapter 6. The sensor can measure very small displacements of the order of few microns with higher sensitivity, better resolution, and higher linearity. Moreover, because of the displacement offset technique used, there are two distinct output frequencies for equal displacements in either direction of the capacitor plate from its null position. Compared to twin-T oscillator based, BLO based displacement sensor requires less total capacitance, and can sense the displacement in micron span with sensitivity as high as 4×10^{11} Hz/m and the resolution as low as 15 nm.

The advantages of the proposed techniques are:

- The CM building blocks can operate with low voltages and hence the circuits employing CM building blocks are suitable for IC technology.
- Grounded-capacitors allow easy compensation for the parasitic capacitors, latter being in parallel with the grounded capacitors. For thin film fabrication, the use of grounded capacitors eliminates the etching process and reduces the number of gold contacts, thereby improving the circuit reliability.
- Equal-valued grounded capacitors help saving silicon area and easy processing in IC technology. For low frequency applications, EVGC realization would facilitate time-multiplexing of all the capacitors and thereby reducing the area on the silicon wafer.

The disadvantages of the proposed techniques are:

- The proposed VM to CM transformation without change in circuit elements requires active devices with virtual ground.
- The proposed synthesis technique in Chapter 3 requires minimum 4 passive elements to realize first order all-pass filter and hence Higashimura's filter given in reference [27] should be preferred.

To summarize:

- A novel procedure for converting VM circuits to the CM circuits without requiring any additional circuit elements and any change in the circuit topology has been developed.
- Three synthesis procedures (Synthesis I, II, III) for realizing a class of transfer functions of any order with negative real poles using only one active device have been proposed which can lead to the circuit design with minimum passive elements. The synthesis procedures are restricted to the transfer functions with distinct negative real poles only and hence are restricted to low Q values. One of the procedures (Synthesis III) is extended further (as Synthesis IV) to realize any stable voltage/current transfer function of any order.
- A synthesis procedure for realizing a ladder filter from passive RLC to active all equal-valued grounded capacitors has been proposed.
- A simple design procedure for realizing an amplitude equalizer with a single OA and single variable resistor has been developed.
- A novel high-frequency BLO based micrometer displacement sensor which can measure very small displacement of the order of few microns with higher sensitivity, better resolution, and higher linearity has been developed.

Although a number of synthesis techniques have been presented in this thesis, there is ample scope of discovering new additional circuit topologies suitable for integrated technology. Some suggestions for future work are as the following:

- The EVGC realization would facilitate time-multiplexing of all the capacitors and thereby reducing the area on the silicon wafer. This can be exploited and experimented.
- In BLO based micrometer displacement sensor, the error compensation between simulated and theoretical plots of frequency ω_0 versus displacement x may be investigated further.
- The noise analysis of the proposed circuits needs to be explored and can be compared with those of the circuits derived by the conventional methods.

APPENDIX

1. Derivation of (2.1)

From Fig. 2.1(a), we get

$$\begin{aligned} I_z &= I_i - I_x \\ (V_x - V_o)Y_2 &= (V_i - V_x)Y_1 - I_x. \end{aligned} \tag{7.1}$$

From (7.1), we get

$$\frac{V_o}{V_i} = -\frac{Y_1}{Y_2} + \frac{V_x}{V_i}\left(1 + \frac{Y_1}{Y_2}\right) + \frac{I_x}{V_i Y_2}. \tag{7.2}$$

2. Derivation of (2.2)

From Fig. 2.1(b), we get

$$I_i - \overline{I}_x = (\overline{V}_x - \frac{I_o}{Y_1})Y_2. \tag{7.3}$$

This gives

$$\frac{I_o}{I_i} = -\frac{Y_1}{Y_2} + \frac{\overline{V}_x Y_1}{I_i} + \frac{\overline{I}_x Y_1}{I_i Y_2}. \tag{7.4}$$

3. Derivation of (3.1)

For the sake of convenience, Fig. 3.1 is redrawn in Fig. 7.1.

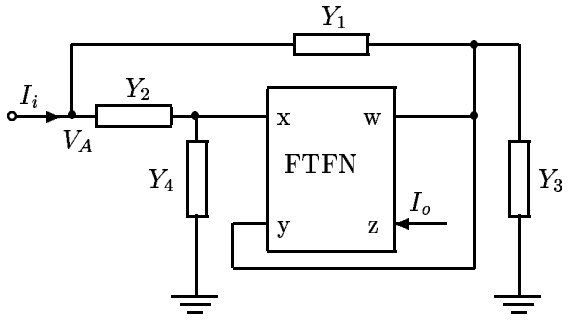


Fig. 7.1. The FTFN circuit.

From Fig. 7.1, we get

$$V_x = V_y = V_w, \tag{7.5}$$

$$V_A = \frac{V_x(Y_2 + Y_4)}{Y_2}, \tag{7.6}$$

$$V_x = \frac{I_i - (V_A - V_w)Y_1}{Y_4} \tag{7.7}$$

and

$$I_o = I_w = (V_A - V_w)Y_1 - V_w Y_3. \tag{7.8}$$

From (7.5), (7.6), and (7.7), we get

$$V_w = \frac{I_i Y_2}{Y_1 Y_4 + Y_2 Y_4} \tag{7.9}$$

and from (7.5), (7.6), (7.8), we get

$$V_w = \frac{I_o Y_2}{Y_1 Y_4 - Y_2 Y_3}. \tag{7.10}$$

Equating (7.9) and (7.10), we get

$$\frac{I_o}{I_i} = \frac{Y_1 Y_4 - Y_2 Y_3}{Y_4(Y_1 + Y_2)}. \tag{7.11}$$

4. Derivation of (3.20)

From Fig. 3.2,

$$V_o = \frac{V_i Y_1 + V_z Y_2}{Y_1 + Y_2}, \tag{7.12}$$

$$V_x = \frac{V_i Y_3 + V_z Y_4}{Y_3 + Y_4}. \tag{7.13}$$

Since $V_x = 0$, from (7.13), we get

$$V_z = -V_i \frac{Y_3}{Y_4}. \tag{7.14}$$

Substituting (7.14) in (7.12), we get

$$\frac{V_o}{V_i} = \frac{Y_1 - \mu Y_2}{Y_1 + Y_2} \tag{7.15}$$

where $\mu = \frac{Y_3}{Y_4}$.

5. Derivation of (5.3)

For the sake of convenience, Fig. 5.1 is redrawn in Fig. 7.2.

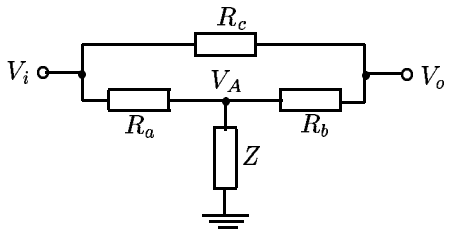


Fig. 7.2. The passive AE circuit.

From Fig. 7.2, we get

$$V_A = \frac{Z(V_i R_b + V_o R_a)}{R_a R_b + R_b Z + R_a Z} \tag{7.16}$$

and

$$\frac{V_i - V_o}{R_c} = \frac{V_o - V_A}{R_b}. \tag{7.17}$$

From (7.17), we get

$$V_A = V_o - \frac{(V_i - V_o)R_b}{R_c}. \tag{7.18}$$

Equating (7.16) and (7.18), we get

$$\frac{Z(V_i R_b + V_o R_a)}{R_a R_b + R_b Z + R_a Z} = V_o - \frac{(V_i - V_o)R_b}{R_c}. \tag{7.19}$$

This gives

$$\frac{V_o}{V_i} = \frac{(R_a + R_b + R_c)Z + R_a R_b}{(R_a + R_b + R_c)Z + R_a(R_b + R_c)}. \tag{7.20}$$

Equation (7.20) can be rearranged as

$$\frac{V_o}{V_i} = \frac{(R_a + R_b)Z + R_a R_b + Z R_c}{(R_a + R_b)Z + R_a R_b + R_c(Z + R_a)} \tag{7.21}$$

$$\frac{V_o}{V_i} = \frac{[Z(R_a + R_b) + R_a R_b]\left[1 + \dfrac{Z R_c}{Z(R_a + R_b) + R_a R_b}\right]}{(Z + R_a)\left[R_c + \dfrac{Z(R_a + R_b) + R_a R_b}{Z + R_a}\right]} \tag{7.22}$$

$$\frac{V_o}{V_i} = \left[\frac{Z(R_a + R_b) + R_a R_b}{(Z + R_a)R_a}\right] \frac{\left[1 + \left(\dfrac{R_c}{R_a}\right)\dfrac{Z R_a}{Z(R_a + R_b) + R_a R_b}\right]}{\left[\dfrac{R_c}{R_a} + \dfrac{Z(R_a + R_b) + R_a R_b}{(Z + R_a)R_a}\right]}. \tag{7.23}$$

6. Derivation of (5.15)

From Fig. 5.3(a), we get

$$V^- = \frac{V_i R_b + V_o R_a}{R_a + R_b} \tag{7.24}$$

and

$$V^+ = \frac{V_i R_c}{R_c + Z_c}. \tag{7.25}$$

Equating (7.24) and (7.25), we get

$$\frac{V_i R_b + V_o R_a}{R_a + R_b} = \frac{V_i R_c}{R_c + Z_c}. \tag{7.26}$$

This gives

$$\frac{V_o}{V_i} = \frac{\frac{R_b}{R_a}\left[\left(\frac{R_a}{R_b}\right)\frac{R_c}{Z_c} - 1\right]}{\frac{R_c}{Z_c} + 1}. \tag{7.27}$$

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RESUME

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