Department of Electrical Engineering, IIT Bombay

EE206 Digital Circuits: Tutorial Sheet II

Implementation of Digital Circuits; Karnaugh Maps

1. For TTL circuits, voltage ringing is caused by lead inductance resonating with shunt capacitance. One often finds (in textbooks and logic data books) the presence of a diode at each input of a multi-emitter transistor (the shaded block in Figure 1(a)). What is their purpose ?

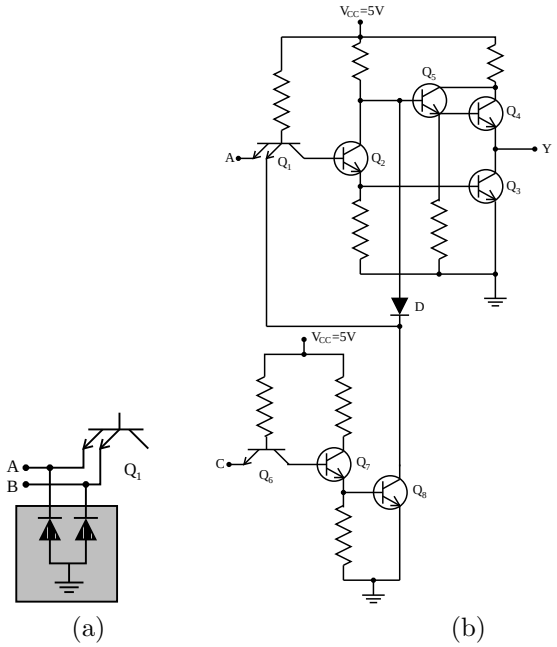

Figure 1: (a) Diodes at the input of a TTL NAND gate, and (b) a TTL NAND Gate in the tristate output configuration

2. (*Hill and Peterson*, Question 4-1) Assume that a simple NAND gate (Figure 2) is to be used in a network composed only of NAND gates of the same type. Why is this situation plausible ? Now, assume that $R_1 = 2K\Omega$, $R_L = 1K\Omega$, and $\beta = 200$. Also assume that the base current of a transistor is $0.5mA$ when it is turned on.

   (a) Determine a steady-state fan-out limit for the gate

   (b) Considering delay, why might a lower nominal fan-out be set for the gate ?

3. (*Hill and Peterson*, Question 4-2) Suppose two gates with specification in the previous question are connected as shown in Figure 2(b). Here, gate 1 drives only gate 2, and the low-current lamp. What is the maximum dc resistance allowed for the lamp, if the circuit is to function properly ? [Hint: the lamp will be lighted and $Z = 1$, when $A = B = C = 1$.]

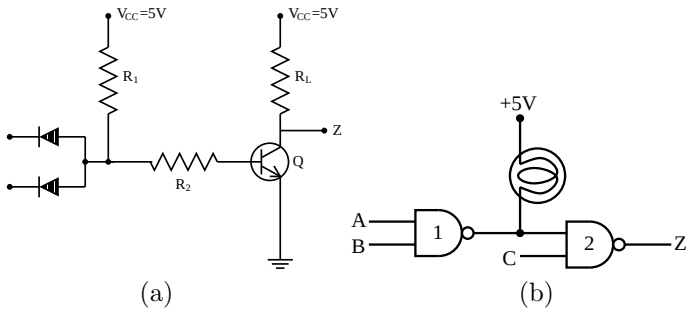

Figure 2: (a) A simple NAND gate, and (b) the circuit for the 'lamp' question

4. *TTL NAND Gate in Tristate Logic Configuration:* Assume that you know the 'normal' functioning of a TTL NAND gate. Now, consider the special case of a TTL NAND gate in a tristate output configuration. Explain the function of the control input C, and how it affects the functioning of the entire circuit, given in Figure 1(b).

5. (Based on *Kohavi*, Question 3-19) *Majority Circuit:* Using a Karnaugh Map, design a minimal logic function of 4 variables w, x, y and z such that the output is 1 whenever a majority of the inputs is 1, and 0, otherwise.