Department of Electrical Engineering, IIT Bombay

EE206 Digital Circuits: Tutorial Sheet III

Combinational Logic: MSI and LSI

1. **Priority Encoder** Given an Octal-to-Binary Encoder Chip with all input and output lines as shown in Figure 1(a). Using this chip, and only NOT, AND and OR gates, design an *Octal-to-Binary Priority Encoder*, whose required input and output lines are shown in Figure 1(b). Assume the

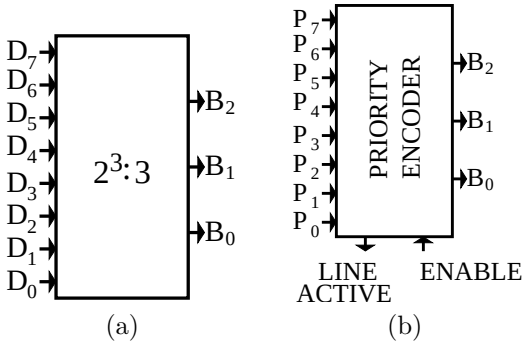

Figure 1: (a) The given Octal-to-Binary Chip, and (b) Input and Output lines for the desired Priority Encoder

availability of suitable multi-input AND and OR gates. Write down *all* boolean expressions, and show only important connections in the circuit. A $LINE\ ACTIVE$ output is 1 when any of the inputs P_7 - P_0 is 1, 0 otherwise. An $ENABLE$ input causes the system to operate according to the desired functionality when $ENABLE = 1$, else is disabled when $ENABLE = 0$. A Priority Encoder operates on the principle that *more than one input* P_i, $0 \leq i \leq 7$ could be 1 at a time, unlike a normal Encoder. For a Priority Encoder, the output is a binary number, corresponding to the "highest" P_i that is 1 *i.e.*, the output corresponds to i such that $P_i = 1$, $P_j = 0\ \forall\ i < j \leq 7$.

2. **Combinational Circuit Design with Multiplexers** The input to a digital circuit are three signals A, B and C (Note that $\overline{A}$, $\overline{B}$ and $\overline{C}$ are NOT available). Logic 1 and 0 are available (*e.g.*, as V_{CC} and GND). The output of the circuit is given to be $f = \overline{A}\ B\ +\ \overline{A}\ \overline{B}\ \overline{C}$. Implement the circuit using *only TWO* $2:1$ *Multiplexer Modules* of the form shown in Figure 2(b) - do not use any other hardware. s is the select line. Data lines D_0 and D_1 are selected (*i.e.* , made the output Y) when $s = 0$ and 1, respectively.

3. **Decoders** Design a $8:256$ decoder using $2:4$ decoders, and SSI hardware chips (if required), both in a tree configuration, as well as in the coincident configuration. How would you compare the hardware requirements in the two cases ?

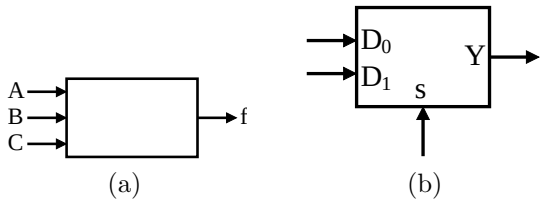

Figure 2: (a) The 3-input combinational circuit to be designed, and (b) A 2:1 Multiplexer Module.

4. **BCD-to-Decimal Decoder** Design a BCD-to-Decimal Decoder. The circuit should also handle the case when an invalid input combination occurs - all outputs should be made zero in this case.

5. **Circuit Design using Decoders** *(Drill Problem), Mano, Problem 5-18*
   A combinational circuit is defined by the following two functions:

   (a) $F_1(x, y) = \sum(0, 3)$
   (b) $F_2(x, y) = \sum(1, 2, 3)$

   - Implement the circuit with a $2:4$ decoder with an $ENABLE$ input, and external NAND gates.
   - Now, implement this with $4:1$ multiplexers, and OR gate, and an inverter.

6. **Circuit Design using Decoders and Multiplexers** *(Drill Problem), Mano, Problems 5-17 and 5-24*
   A combinational circuit is defined by the following three functions:

   (a) $F_1 = x'y' + xyz'$
   (b) $F_2 = x' + y$
   (c) $F_3 = xy + x'y'$

   Design the circuit with a decoder and external gates.

7. **Circuit Design using Multiplexers** *(Drill Problem), Mano, Problem 5-26*
   Implement a Full Adder circuit using multiplexers.

8. **ROM** *Mano, Problem 5-28*
   Prove (using the representation of a number in a number system as a linear combination of powers of the base) that a 32×8 ROM can be used to implement a circuit that generates the binary square of an input 5-bit number with $B_0 = A_0$, and $B_1 = 0$. Draw a block diagram of the circuit and list the first four and last four entries of the ROM truth table.