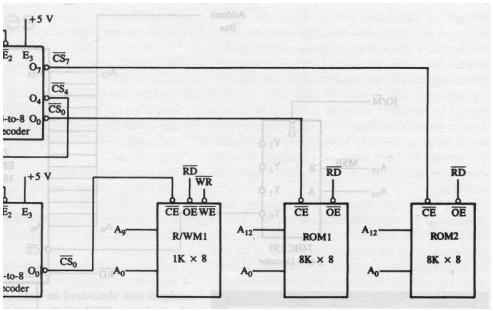
Department of Electrical Engineering, IIT Bombay

EE309 Computer Organization, Architecture and Microprocessors: Tutorial Sheet II

The 8085: Hardware and Interfacing

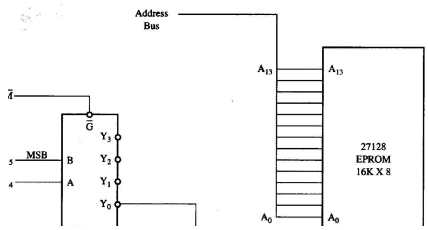
1. Consider Figure 1 (*Gaonkar*, Chapter 3). $\overline{CS}$ and $\overline{CE}$ denote 'Chip Select' and 'Chip Enable'. $\overline{OE}$ and $\overline{WE}$ enable the output buffer of a memory chip for a read operation, and enable a write, respectively.



   (a) Specify the memory addresses of ROM1, ROM2 and R/WM1.

   (b) Eliminate the second decoder and connect $\overline{CS_4}$ to $\overline{CE}$ of the R/WM1, and identify its memory map and foldback memory. Normally, one considers a memory range by considering all 'don't care' lines as 0s. The rest of the memory space is the foldback memory.

2. Consider Figure 2 (*Gaonkar*, Chapter 3).



   (a) Identify the address range of the memory chip.

   (b) Connect Y_1 to the $\overline{CE}$ of the memory chip in place of Y_0, and identify the address range of the memory chip.

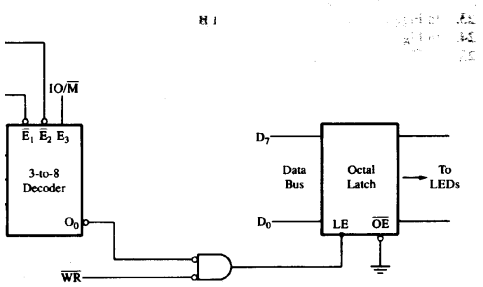
3. (*Gaonkar*, Chapter 4)

   (a) Explain why a latch is used for an output port, and a tristate buffer is used for an input port.

   (b) What 8085 control signals are needed for memory-mapped I/O ?

   (c) Can the μP differentiate between the cases when it is reading from a memory-mapped input port, or reading from memory ?

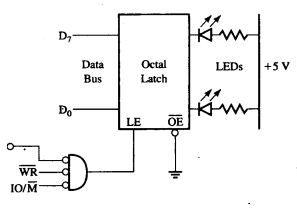
4. Consider Figure (*Gaonkar*, Chapter 4).



   (a) Identify the port addresses.

   (b) If $\overline{OE}$ is connected directly to the $\overline{WR}$ signal and the output of the decoder is connected to the latch enable (through an inverter), can you display a byte at the output port ? Explain your answer.

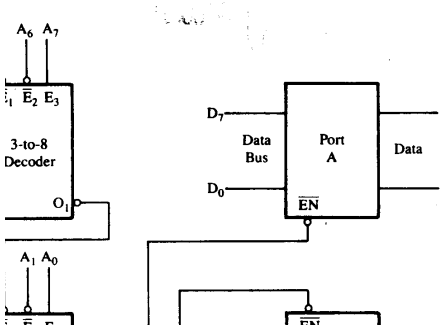
5. Consider Figure (*Gaonkar*, Chapter 4).



   (a) Justify that the arrangement shown represents peripheral-mapped (Isolated) I/O.

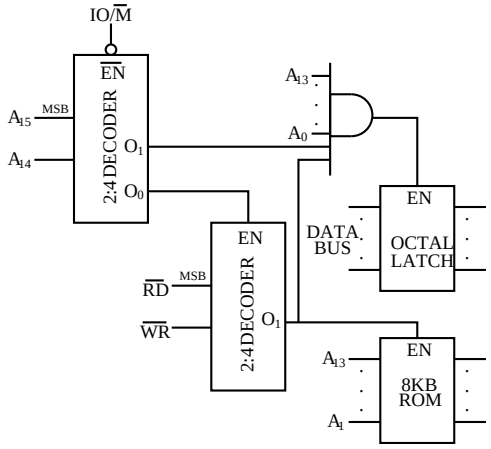
   (b) What is the port address if all the don't care address lines are assumed to be at logic 0 ?

6. Consider Figure (*Gaonkar*, Chapter 4). Identify ports A and B as input



or output ports. What are the addresses of ports A and B ?

7. **Mem(I/)Orable Question**



(a) Identify the memory map of the ROM chip, and its foldback memory.

(b) Identify the port as an Input port or an Output Port. Is this I/O Isolated (Peripheral-mapped), or Memory-mapped ?