Parallelization of DC-Analyzer

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Abstract

Physical problems offer scope for macro level parallelization of solution by their essential structure. For parallelization of electrical network simulation, the most natural structure based method is that of *Multiport Decomposition*. In this paper this method is used for the simulation of electrical networks consisting of resistors, independent and controlled sources using a distributed cluster of weakly coupled processors. Results are presented for the cases where the number of processors are 1,2,4,8 and for circuit sizes upto 700,000 nodes and 1.4 million edges. We use a cluster of Pentium IV processors linked through a 10/100MBPS ethernet switch.

Keywords: Multiport Decomposition, Parallel processor, simulation.

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