Parallelization of DC-Analyzer

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ABSTRACT

Physical problems offer scope for macro level parallelization of solution by their essential structure. For parallelization of electrical network simulation, the most natural structure based method is that of *Multiport Decomposition*. In this paper this method is used for the simulation of electrical networks consisting of resistors, independent and controlled sources using a distributed cluster of weakly coupled processors. Results are presented for the cases where the number of processors are 1,2,4,8 and for circuit sizes upto $700,000$ nodes and 1.4 million edges. We use a cluster of Pentium IV processors linked through a 10/100 Mbps ethernet switch.
Keywords: Multiport Decomposition, Parallel processor, simulation.

INTRODUCTION

It is becoming increasingly necessary to solve very large circuits accurately because of higher chip densities and also because of the incorporation of high frequency effects. Usually such circuits are too large to be solved on a single processor and some form of distributed computing [3] has to be resorted to. We have chosen the model of cluster computing in which all the processors are connected through weak media. This level of resources is easy to obtain in almost any computational laboratory or software house.

The general approach used by us to parallel process a circuit simulator is to decompose the circuit into k 'multiports'. These decomposed k multiports are solved independently. After obtaining the port behaviour we use the connection constraints between multiports for computing the port voltages and currents. It is necessary therefore that decomposed blocks should have minimum interconnection between themselves. Every general purpose circuit simulator has a *DC-Analyzer* at its core. In any iteration of non-linear circuit analysis a circuit simulator solves a circuit consisting only of elements: resistors (R),controlled sources (CS), voltage sources (V) and Current sources (J). Thus, We can exploit parallelism, first, by parallelizing each iteration of the non-linear analysis [4] and second, by parallelizing the *DC-Analyzer* [6, 2, 9] itself.

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MULTIPORT DECOMPOSITION AND METHOD USED

A electrical circuit is divided into k parts by using *Multiport Decomposition* [7] in such a way that there is no interaction between the k parts. The decomposed parts may be large but the number of ports should be minimum.

A network N, which is to be decomposed into two multiports, is given in figure 1. N_A and N_B are the subnetworks of N. Assume that the devices in both of the network are decoupled. It can be seen that the currents in N_B can affect the currents in N_A or vice-versa according to the KCE constraint at n_1, n_2. Simultaneously voltages in $N_A(N_B)$ can affect the voltages in $N_B(N_A)$ because voltage $v_1 = v_{n_1} - v_{n_2}$. Thus the constraint on all currents and voltages of N remain the same if we replace the network by the decomposed network. Both the original and decomposed networks are shown in figure 1. The conditions $v_P = v_{P'}, i_P = -i_{P'}$, are imposed by the *port connection diagram* which is shown by two dotted lines in parallel in figure 1.

The method used for circuit decomposition is *Multiport Decomposition*. The analysis is performed by *DC-Analyzer* [1] which uses the *Two-Graph Method* [1]. An elementary partitioner was used to obtain the graph of the network into subgraphs of approximately equal size with very few common nodes. *PVM* [5, 8] is used for communicating among processors. Implementation details are given in [6, 2, 9].

RESULTS

Parallelization of DC-Analyzer was implemented using the network of PIV 1.6 GHz processors each having

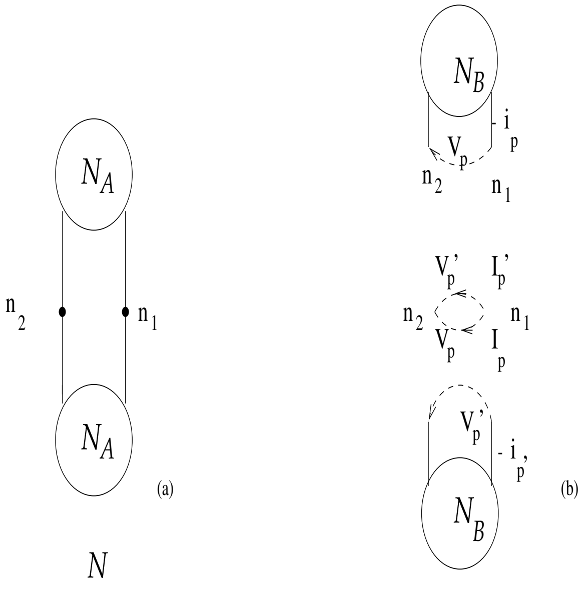

Figure 1: Multiport Decomposition Technique

256MB RAM. Processors used were connected through a 10/100 Mbps Switch. Results are given for different circuit sizes. In each circuit voltage and current sources are kept constant at 14% and 7% of the circuit size respectively. Results are presented for the 8 block partitions. For comparison, we have given the results for a 10 block partition with 2 slave processors. Here, t_1, t_2, t_4 and t_8 is the total time (in seconds) taken by $1, 2, 4$ and 8 slave processors.

Circuit	8-block Partition				10-block Partition
	t_1	t_2	t_4	t_8	t_2
g60k	17	10	6	4	11
g105k	36	21	11	7	23
g200k	82	43	25	14	52
g300k	125	64	36	21	84
g400k	222	126	66	38	131
g500k	282	145	85	49	178
g600k	417	237	129	76	281
g700k	905	504	319	220	490

CONCLUSION

In this paper a method of parallelization of circuit simulation is outlined which is based on the structure (topology) of the network viz. *Multiport Decomposition*. We use this method to parallelize the DC-Analyzer noting that since a DC-Analyzer lies at the core of every general purpose simulator, this would amount to parallelizing the circuit simulator. Our results show speedups proportional to the number of processors provided the blocks into which the network is broken up do not have many ports in between (number of ports $< 1\%$). We find it interesting that a method which uses no sparsity exploiting technique except the simple structural one of multiport decomposition does as well as can be hoped for with the best kind of parallelization. We note that circuits of sizes up to $700,000$ nodes and 1.4 million edges have been solved by this technique in a few minutes using facilities easy to obtain in any computational laboratory or software house.

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