Random Access Scan

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EE 709: Testing & Verification of VLSI Circuits
Lecture – 23 (Feb 27, 2012)
Should Serial Scan Continue?

- **Three Problems with serial-scan**
  - Test power
  - Test application time
  - Test data volume

- **Efforts and limitations**
  - ATPG for low test power consumption
    - Test power $\downarrow$ Test length $\uparrow$
  - Reducing scan clock frequency
    - Test power $\downarrow$ Test application time $\uparrow$
  - Scan-chain re-ordering (with additional logic insertion)
    - Test power/time $\downarrow$ Design time $\uparrow$
  - Test Compression
    - Test time/data size $\downarrow$ Has limited capability for Compacted test

- **Orthogonal attack**
  - **Random access scan** instead of **Serial-scan**
  - Hardware overhead? Silicon cost $\ll$ Testing cost
Random Access Scan

First proposed by Ando in 1980

It was considered impractical due to large area overhead.

Baik at al. revisited it in 2004 [ITC’04]

Proposed as a simultaneous solution to test power, test time, and test data volume

Baik, 2005, proposed PRAS which showed around 3x speed up, reduction in test data volume with only minor increase in area compared to Serial Scan, thus making RAS practical
Random Access Scan: Architecture

A solution to test power, test time and test data volume

- Architecture
  - Each FF has unique address
  - Address shift register
  - X-Y Decoder
  - Select FF to write/read

Saluja et al [ITC’04]
Scan Operation Example

- Test vector

<table>
<thead>
<tr>
<th>Test</th>
<th>PPI($i_i$)</th>
<th>PPO($o_i$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>t1</td>
<td>00101</td>
<td>00110</td>
</tr>
<tr>
<td>t2</td>
<td>00100</td>
<td>00101</td>
</tr>
<tr>
<td>t3</td>
<td>11010</td>
<td>11010</td>
</tr>
<tr>
<td>t4</td>
<td>00111</td>
<td>01011</td>
</tr>
</tbody>
</table>

- Scan operation for $t_2$

- Complete test application

  Total number of scan operation = 15
Test Vector Ordering

- Test data volume and Test application time is proportional to the random access scan operation
- Goal: Reduce # scan operation

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<tbody>
<tr>
<td>t₁</td>
<td>00101</td>
<td>00110</td>
</tr>
<tr>
<td>t₂</td>
<td>00100</td>
<td>00101</td>
</tr>
<tr>
<td>t₃</td>
<td>11010</td>
<td>11010</td>
</tr>
<tr>
<td>t₄</td>
<td>00111</td>
<td>01011</td>
</tr>
</tbody>
</table>

# Scan operation = 8
Optimizing Address Scan

- The cost of address shifting
  - # of scan operation x ASR width
  - Example address set = \{ 1, 5, 6, 11 \} for 4-bit ASR
  - $4 \times 4 = 16$

- Proper ordering of address can minimize shifting cost
  - Apply 11(1011) after 5(0101) → needs only 1 left-shift

- Minimizing address shifting cost
  - Construct Address Shifting Distance Graph (ASD-graph)
  - Find min-cost Hamiltonian path using ATSP algorithm (Result: 5 shifts)

$G = < V, E >$
$V = A_{ij} = \{1, 5, 6, 11\}$
$E = \{ e_{ij} | e_{ij} \text{ is an edge between } v_i \text{ and } v_j \}$

$w(e_{ij}) = \text{The number of minimum left-shift operation for the transition from } v_i \text{ to } v_j.$
Thank You