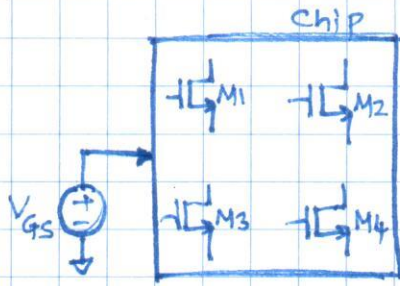


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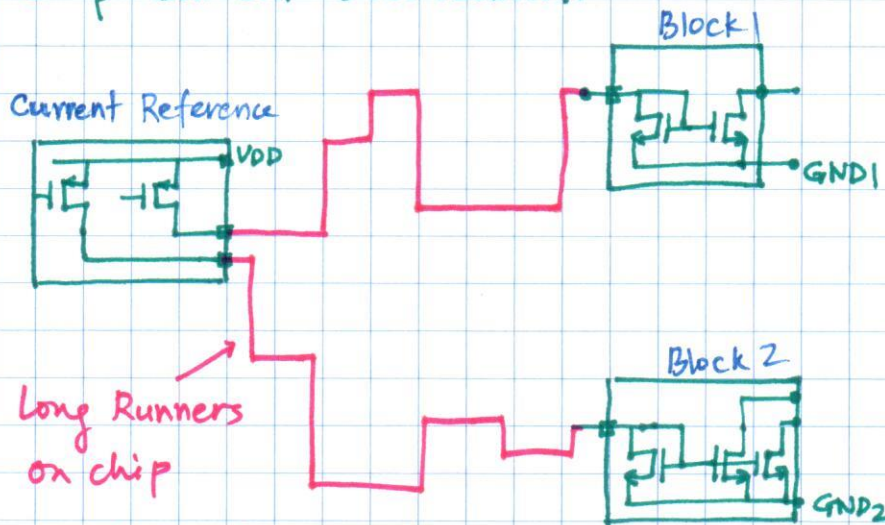
Current Mirrors / Sources



Voltage biasing → Bad idea

- PROCESS VARIATIONS M_1, M_2, M_3, \dots
- GND, VDD potentials could be different across chip (IR drops)
- Transistor properties across chip change.

On chip current distribution.



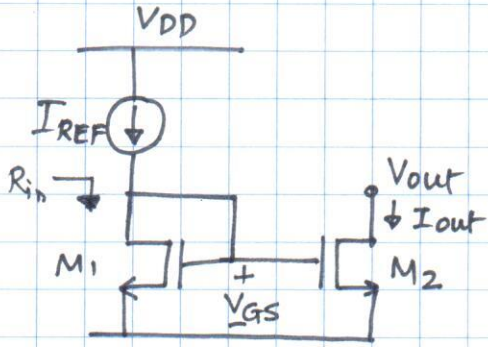
Long Runners
on chip

- can have large R .
- current is faithfully replicated all over chip.

Current Sources used for DC biasing

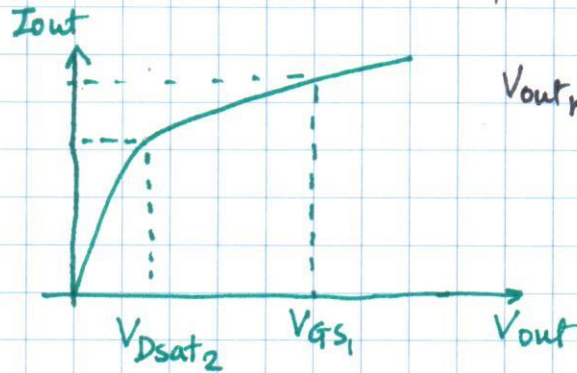
- Speeds → O/p resistance
 - voltage compliance (min - max voltage)
 - Accuracy & process independance
 - DC balance
 - i/p Resistance
- } for current mirrors

Simple Current Mirror



$$R_{in} = \frac{1}{g_{m1} + g_{ds1}}$$

$$g_{ds1} = \frac{1}{V_{o1}}$$



$$I_{REF} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH1})^2 (1 + \lambda_1 V_{GS1})$$

$$I_{OUT} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH2})^2 (1 + \lambda_2 V_{OUT})$$

Assume $V_{TH1} = V_{TH2}$

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \frac{(1 + \lambda_2 V_{OUT})}{(1 + \lambda_1 V_{GS})}$$

For accurate mirroring

keep $L_1 = L_2$

$\Rightarrow \lambda_1 = \lambda_2 = \lambda$

$$\frac{I_{OUT}}{I_{REF}} = \frac{W_2}{W_1} (1 + \lambda (V_{OUT} - V_{GS}))$$

To keep λ small \rightarrow use long channel devices

$L \gg L_{min}$.

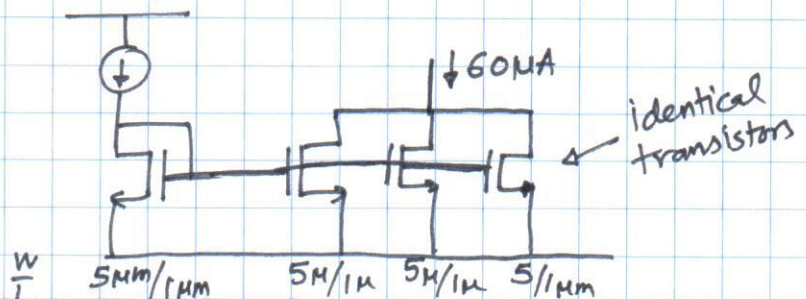
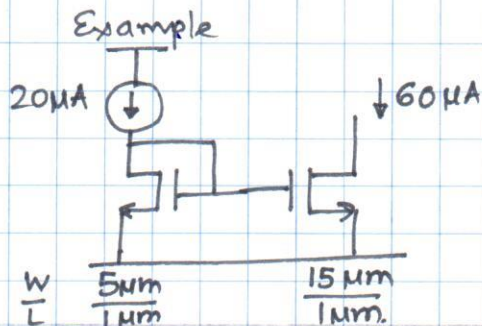
$$\frac{I_{OUT}}{I_{REF}} \approx \frac{W_2}{W_1}$$



For accurate mirroring

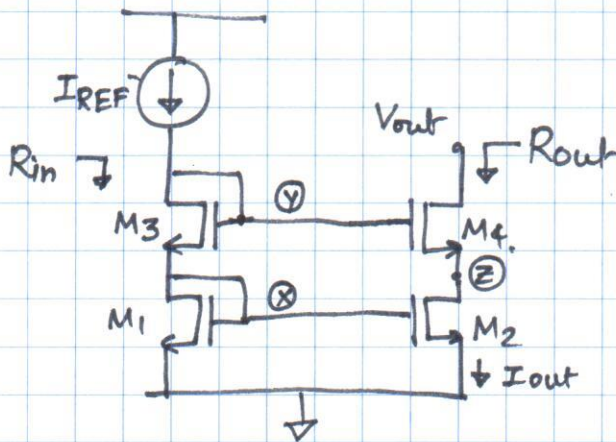
keep $W_2 = N W_1$ N integer

Replicate transistors - Don't stretch W



How to scale currents/transistor sizes?

Cascode Current Mirror



$$R_{in} = \frac{1}{g_{m1}} + \frac{1}{g_{m3}} = \frac{2}{g_m}$$

$$R_{out} \approx (g_{m4} r_{o4}) r_{o2}$$

$$V_Y = V_{GS3} + V_{GS1}$$

$$V_Z = V_{GS3} + V_{GS1} - V_{GS4} = V_{GS1}$$

$$V_{out_{min}} = V_Z + V_{dsat4}$$

$$\approx V_{GS1} + V_{dsat4}$$

$$\approx V_T + V_{dsat1} + V_{dsat4}$$

$$\approx V_T + 2V_{dsat}$$

$$\approx 0.5V + 2(0.2) = 0.9V$$

Not suitable for low voltage operation
 $V_{DD} = 1.2V$.

