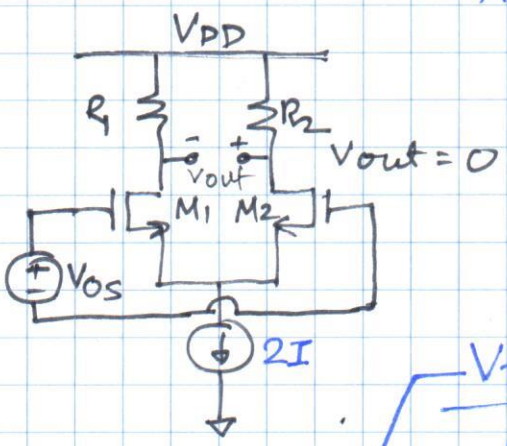
DC offset

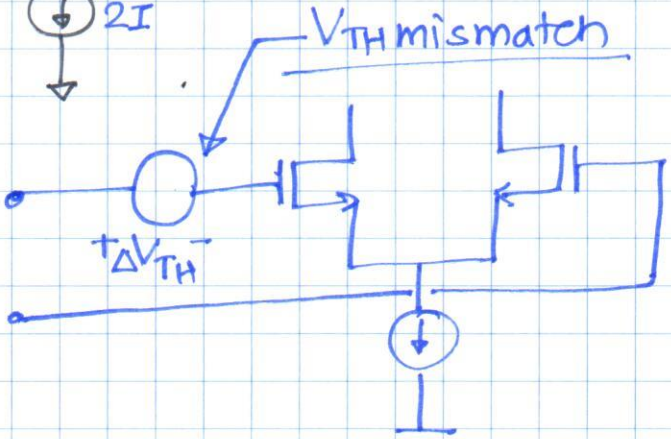
Input Referred Offset Voltage V_{os}

= i/p DC voltage required to make $V_{out} = 0$

- Systematic offset - Bad design practice, V_{DS} mismatched
- Random offsets - process variations.



- R mismatches
- W/L mismatches for M_1, M_2
- V_{TH} mismatches for M_1 & M_2



$\rightarrow V_{os} = \Delta V_{TH}$

R mismatch $\Rightarrow$ V_{out} due to R mismatch $= I \Delta R_D$

$$V_{os \text{ due to R mismatch}} = \frac{V_{out}}{A_{DM}} = \frac{I \Delta R_D}{g_m R_D}$$

To calculate input referred V_{os}

Similarly you can prove that

$$V_{os \text{ due to K mismatch}} = \frac{I}{g_m} \frac{\Delta K}{K}$$

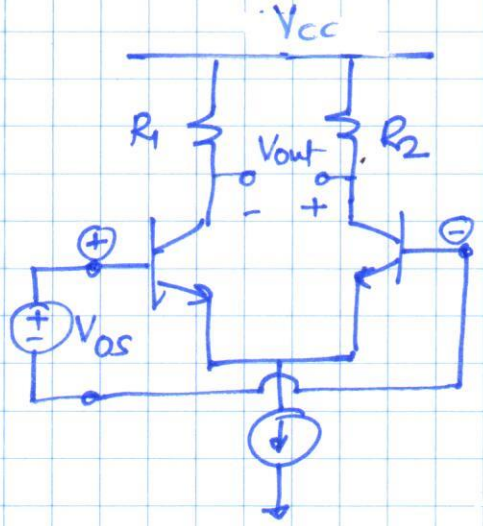
$K = \mu_n C_{ox} \frac{W}{L}$

Since each mismatch is randomly varying quantity, we take rms addition for final effect

$$V_{OS_{overall}}^2 = \Delta V_{TH}^2 + \frac{I^2}{g_m^2}\left(\left(\frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{\Delta K}{K}\right)^2\right)$$

I, g_m, R_D, K are average quantities.

FOR BJT amplifier



o/p offset

Rmismatch $\rightarrow I\Delta R_D$

$$V_{OS_{Rm}} = \frac{I\Delta R_D}{g_m R_D} = V_T \cdot \frac{\Delta R_D}{R_D}$$

$g_m = \frac{I}{V_T} \rightarrow \frac{KT}{q}$

I_S mismatch

$= V_{BE_1} = V_{BE_2}$

$$V_T \ln\frac{I_1}{I_{S_1}} = V_T \ln\frac{I_2}{I_{S_2}}$$

$$\Rightarrow \frac{I_1}{I_{S_1}} = \frac{I_2}{I_{S_2}} \Rightarrow \frac{\Delta I}{I} = \frac{\Delta I_S}{I_S}$$

$$V_{OS}\ @\ o/p = \Delta I R = \frac{\Delta I_S}{I_S} \cdot I R$$

$$V_{OS_{i/p\,ref}} = \frac{\Delta I_S}{I_S}\cdot\frac{I R}{\boxed{g_m R}} = V_T\frac{\Delta I_S}{I_S}$$

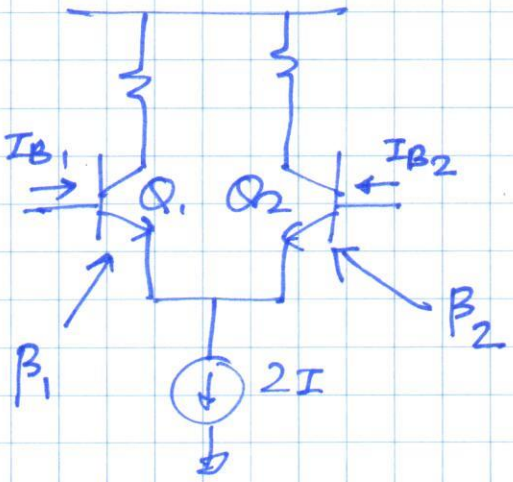
Adm gain

$$V_{OS_{overall}}^2 = V_T^2\left(\frac{\Delta R_D}{R_D}\right)^2 + V_T^2\left(\frac{\Delta I_S}{I_S}\right)^2$$

{ RMS addition

Input Offset Current (for BJT amplifier)

↳ due to β mismatch



$$I_{OS} = |I_{B_1} - I_{B_2}|$$

$$= \left| \frac{I}{\beta_1 + 1} - \frac{I}{\beta_2 + 1} \right|$$

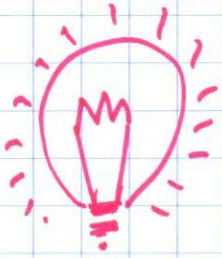
$$\cong I \left(\frac{\Delta\beta}{\beta^2} \right)$$

β avg. value

$$\cong \frac{I}{\beta} \left(\frac{\Delta\beta}{\beta} \right)$$

$$\cong I_B \left(\frac{\Delta\beta}{\beta} \right)$$

Avg. Base current — avg. β.



MOSFET

$$V_{OS_{overall}}^2 = \Delta V_{TH}^2 + \frac{I^2}{g_m^2} \left(\left(\frac{\Delta R_D}{R_D} \right)^2 + \left(\frac{\Delta k}{k} \right)^2 \right)$$

BJT

$$V_{OS_{overall}}^2 = V_T^2 \left(\frac{\Delta R_D}{R_D} \right)^2 + V_T^2 \left(\frac{\Delta I}{I_S} \right)^2$$

compare MOS $\frac{I}{g_m} \Rightarrow \frac{V_{dsat}}{2} \sim 100mV$

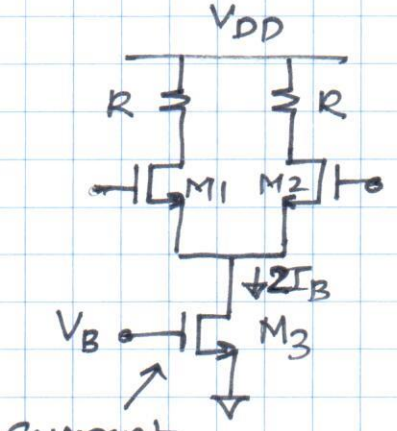
compare to V_T 26mV.

MOS – relatively high offset voltage comp to BJT
(~10mV) (~1mV)

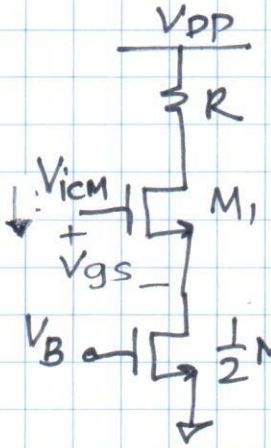
NO i/p offset current (MOS advantage)

Input Common-Mode Range (CMR)

→ Range of common-mode i/p voltage for which all devices are → in saturation (MOSFET)
↳ in active region (BJT)



Since we are analysing common-mode i/p → half ckt



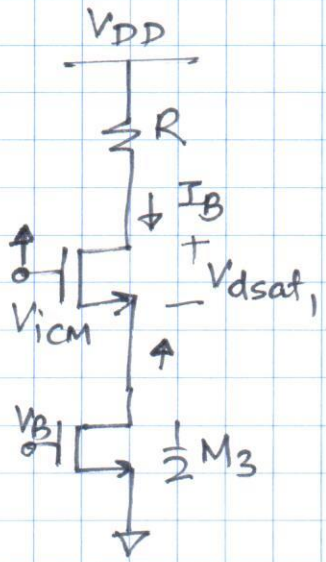
$V_{icM(min)}$ – M_3 @ sat-edge

$V_{icM(min)} = V_{gs_1} + V_{dsat_3}$

$\approx V_{TH} + V_{dsat} + V_{dsat}$

$\approx V_{TH} + 2V_{dsat}$

(assuming similar V_{dsat})



$V_{icM(max)}$ = when M_1 enters non-sat. (sat-edge)

$V_{icM(max)} - V_{gs_1} = V_{DD} - I_B R - V_{dsat_1}$

$V_{icM(max)} = V_{TH_1} + V_{dsat_1} + V_{DD} - I_B R - V_{dsat_1}$

$= V_{DD} + V_{TH_1} - I_B R$

$I_B R$: Drop across R

Can be larger than V_{DD}

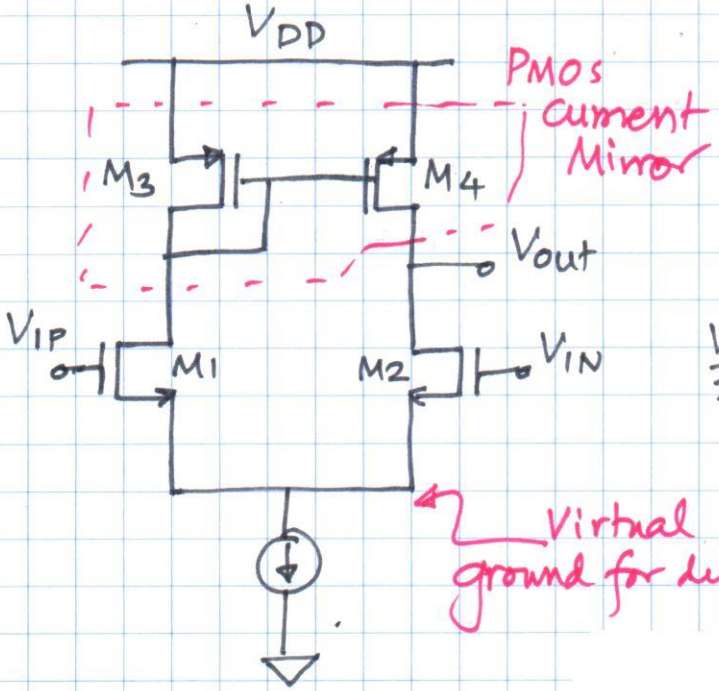
Similar analysis for BJT

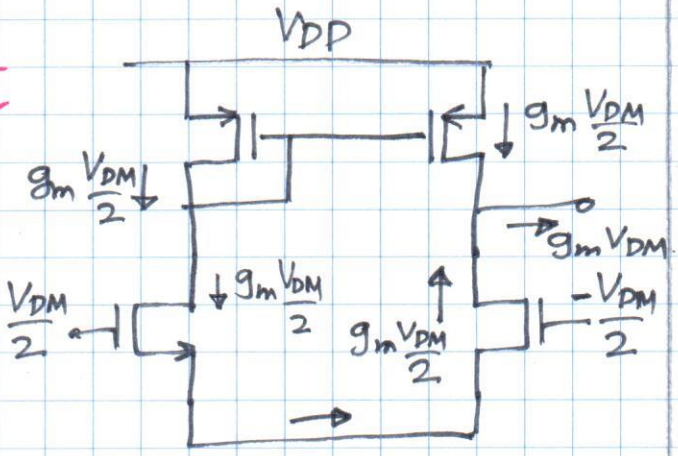
$V_{icm\,max} = V_{CC} + V_{BE} - V_{CEsat} - IR \approx V_{CC} + 0.4 - IR$

$V_{icm\,min} = V_{BE} + V_{CEsat} \approx 0.7 + 0.3 \approx 1V$

Diff Pair with Current Mirror Load.

* Increase gain of amplifier
* Diff-2-Single Ended conversion.





Trick to figure out gain (single Stage)

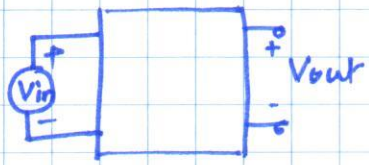
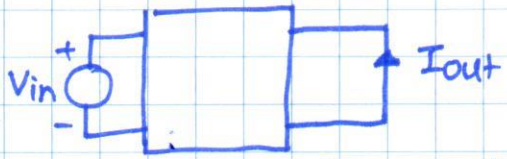


Figure out voltage gain

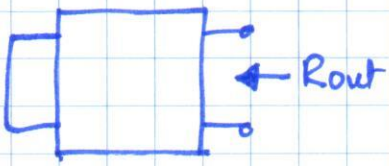
$$A_V = \frac{V_{out}}{V_{in}}$$

Step 1. Short Circuit Gm



$$G_m = \frac{I_{out}}{V_{in}}$$

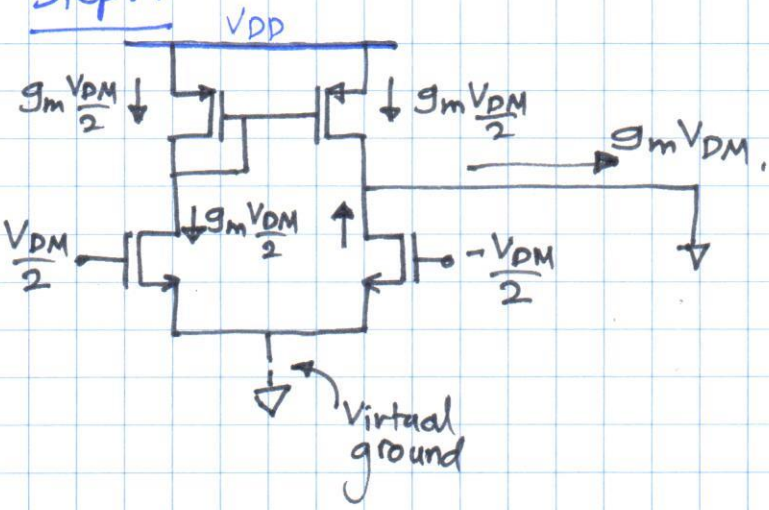
Step 2: Rout calculation (Vin=0)



Voltage Gain

$$\Rightarrow A_V = -G_m R_{out}$$

Step. 1

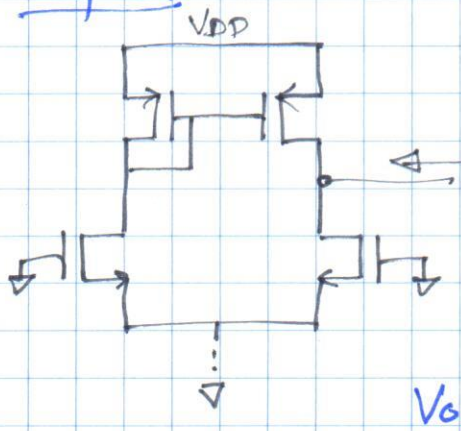


$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_m V_{DM}}{V_{DM}}$$

$$= g_m$$

← for each Diff. pair transistor

Step 2.



R_o transistor o/p resistance

Voltage gain $A_V = g_m (r_{on} \| r_{op})$

or $= \frac{g_m}{g_{dsn} + g_{dsp}}$

$g_{dsn} = \frac{1}{r_{on}}$; $g_{dsp} = \frac{1}{r_{op}}$

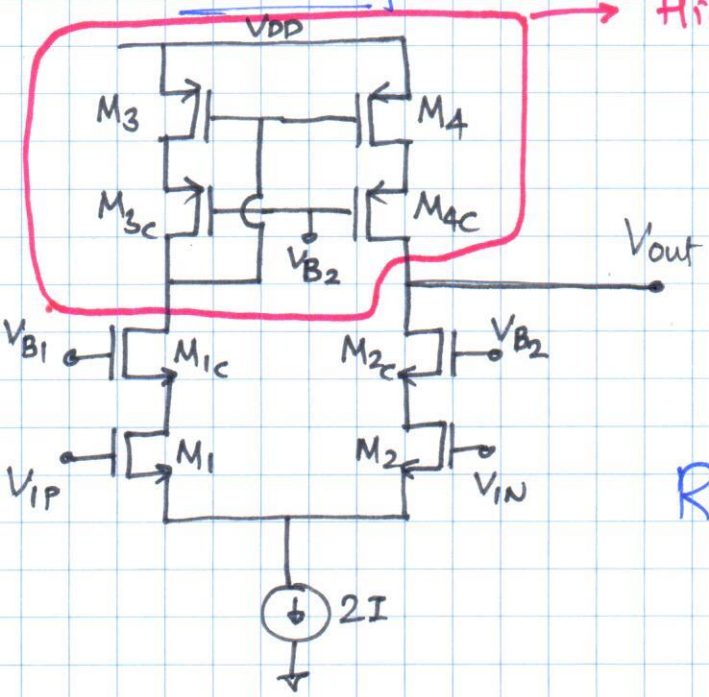
Increase A_V (Remember opamp $A_V \to \infty$)

→ Increase g_m → high I, W/L

→ Increase r_o → cascoding

→ Add another gain stage (cascading)

Cascoding



→ High Swg. Cascode Current Mirror

Cascode Transistors
$M_{1c}, M_{2c}, M_{3c}, M_{4c}$

$G_m = g_{m_{1,2}} = g_m$ ↑ i/p diff pair

$R_{out} = (g_{m_{2c}} r_{o_{2c}}) r_{o_2} \,\|\, (g_{m_{4c}} r_{o_{4c}}) r_{o_4}$

$A_V = G_m R_{out} = g_m \left[(g_{m_{2c}} r_{o_{2c}}) r_{o_2} \| (g_{m_{4c}} r_{o_{4c}}) r_{o_4} \right]$

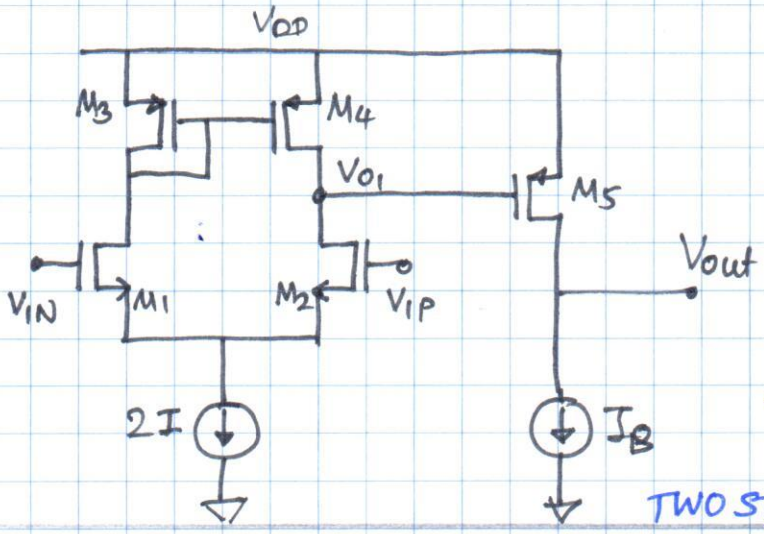
If all g_m & r_o equal (for each transistor)

$A_V \cong \frac{1}{2} g_m [g_m r_o \cdot r_o]$

$= \frac{1}{2}(g_m r_o)^2$ ← gain squared.

Adding Second Stage

(we will study this in detail later.)



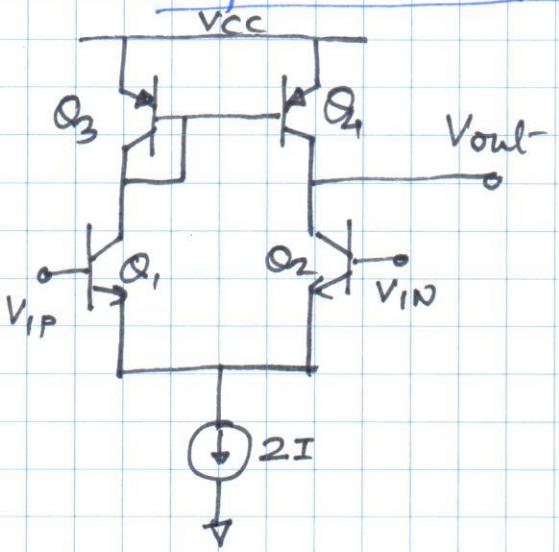
$\frac{V_{o1}}{V_{input}} = -g_{m_1} \cdot (r_{o_2} \| r_{o_4})$

$\frac{V_{out}}{V_{o1}} = -g_{m_5} \cdot r_{o_5}$

$\frac{V_{out}}{V_{input}} = g_{m_1} (r_{o_2} \| r_{o_4}) \cdot g_{m_5} r_{o_5}$

TWO STAGE OTA

Bipolar Examples

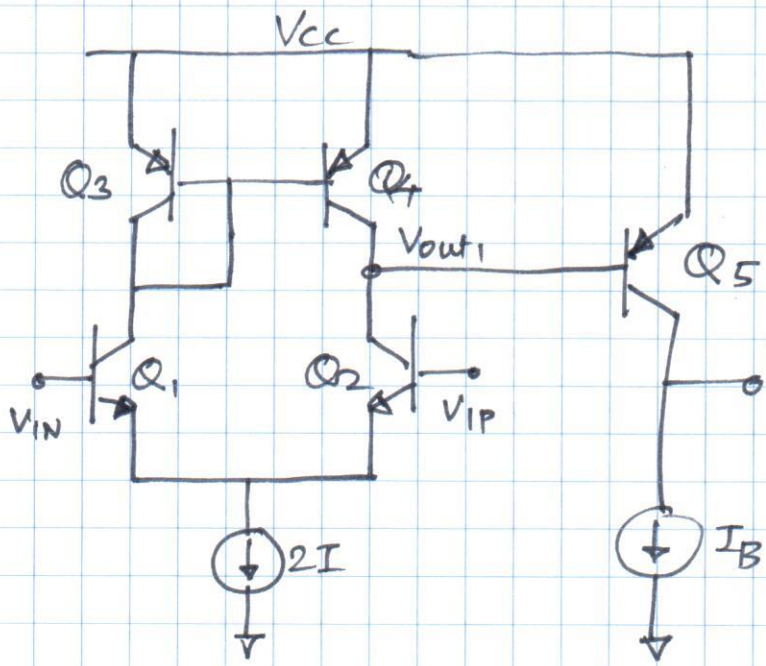


$$A_V = \frac{V_{out}}{V_{IP}-V_{IN}} = g_m\left(r_{o_2} \| r_{o_4}\right)$$

if $r_{o_2} = r_{o_4}$

$$\approx \frac{g_m r_o}{2}$$

Two Stage OTA



$$\frac{V_{out1}}{V_{input}} = -g_{m_1}\left(r_{o_2} \| r_{o_4} \| r_{\pi_5}\right)$$

$$\frac{V_{out}}{V_{out_1}} = -g_{m_5} r_{o_5}$$

$$A_V = g_{m_1}\left(r_{o_2} \| r_{o_4} \| r_{\pi_5}\right) g_{m_5} r_{o_5}$$

Bipolar i/p resistance

(Output Resistance of I_B is ignored here)